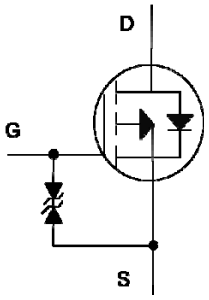
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DSON\ (MAX.)}$	44mΩ
I_D	-4A



Pb-Free Lead Plating & Halogen Free

ESD Protection – up to 2KV HBM

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A = 25 °C	I_D	-4	A
	T_A = 70 °C		-3.5	
Pulsed Drain Current[1]		I_{DM}	-16	
Power Dissipation	T_A = 25 °C	P_D	1.25	W
	T_A = 70 °C		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3]	$R_{\theta JA}$		100	°C / W
Junction-to-Lead[4]	$R_{\theta JL}$		55	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]100°C / W when mounted on a 1 in^2 pad of 2 oz copper.

[4] $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

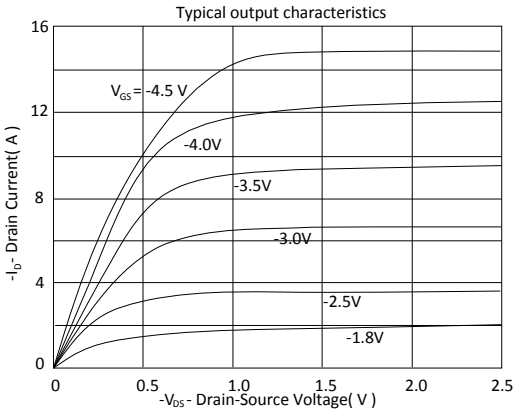
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.3	-0.65	-1.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±10	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -16V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-4			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -4A		37	44	mΩ
		V_{GS} = -2.5V, I_D = -3A		55	70	
		V_{GS} = -1.8V, I_D = -1A		65	90	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -4A		14		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		1059		pF
Output Capacitance	C_{oss}			132		
Reverse Transfer Capacitance	C_{rss}			127		
Total Gate Charge[1,2]	Q_g	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -4A		12.9		nC
Gate-Source Charge[1,2]	Q_{gs}			1.8		
Gate-Drain Charge[1,2]	Q_{gd}			3.2		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω		15		nS
Rise Time[1,2]	t_r			30		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			35		
Fall Time[1,2]	t_f			35		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-3	A
Pulsed Current[3]	I_{SM}				-12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

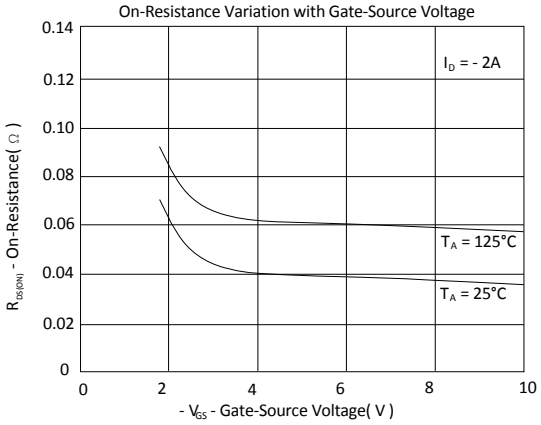
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

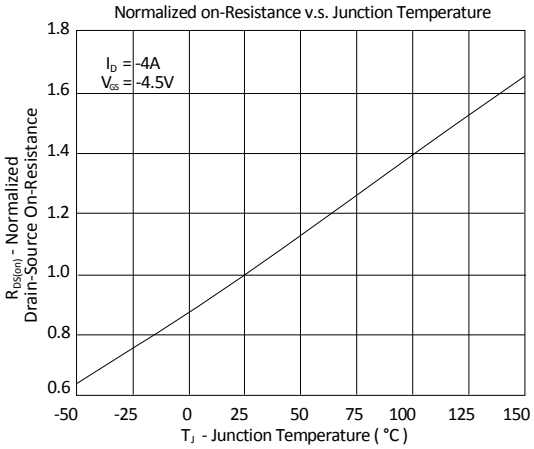
[2]Independent of operating temperature.

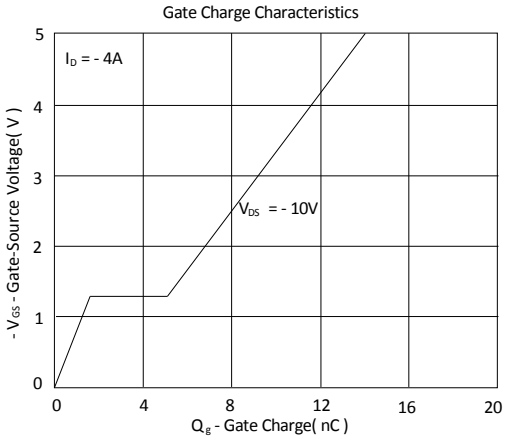
[3]Pulse width limited by maximum junction temperature.

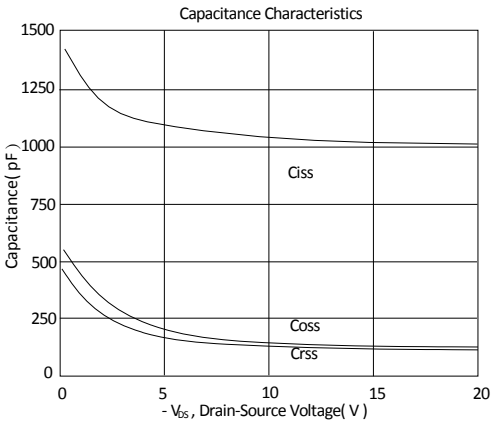
TYPICAL CHARACTERISTICS

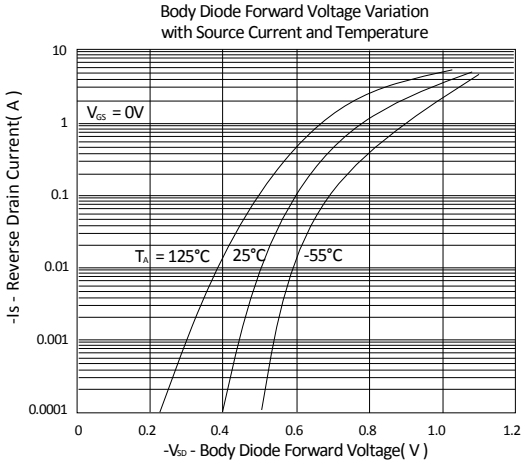




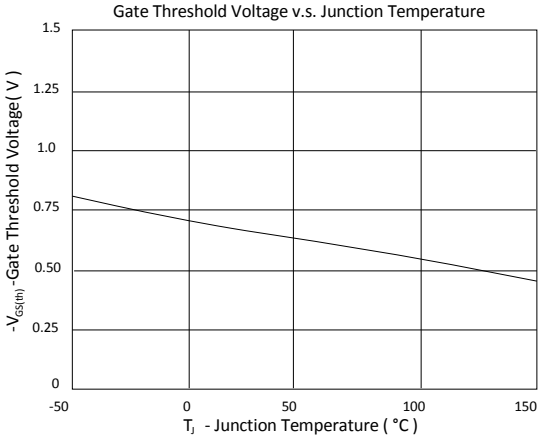




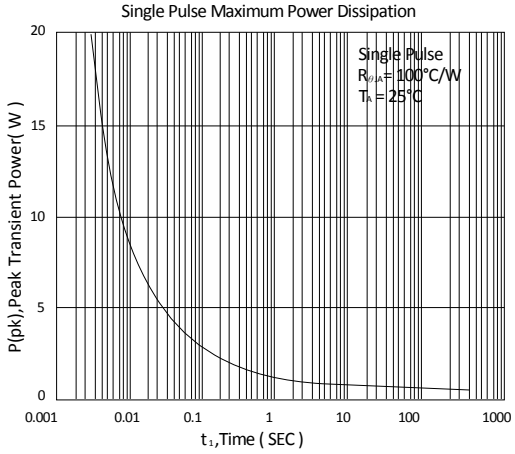




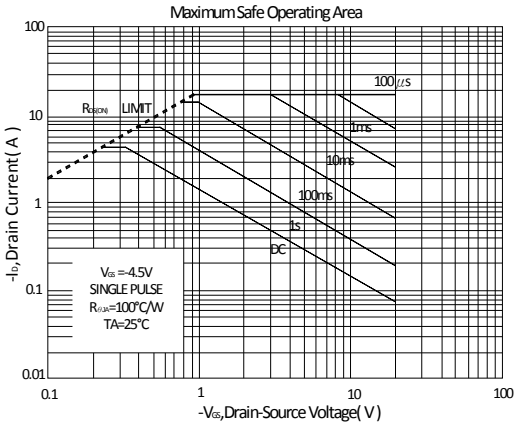
Gate Threshold Voltage v.s. Junction Temperature



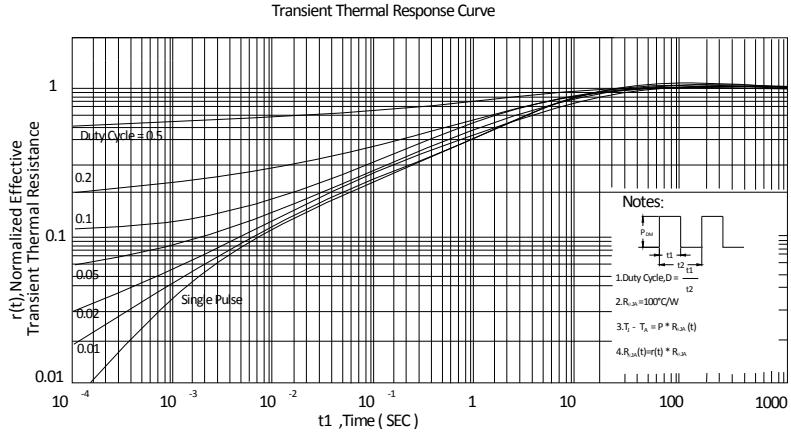
Single Pulse Maximum Power Dissipation



Maximum Safe Operating Area

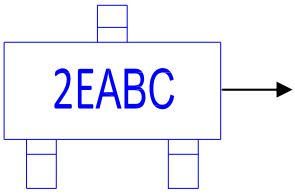


Transient Thermal Response Curve



Ordering & Marking Information:

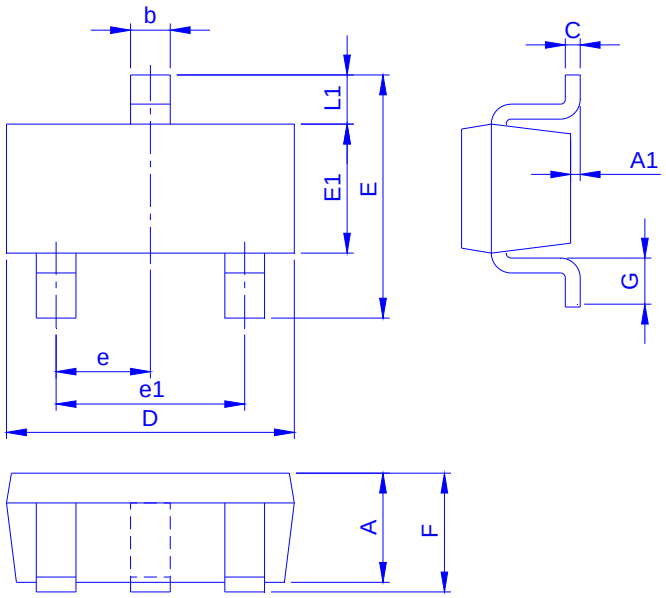
Device Name: EMZF50P02J for SOT-23



2E: Device Code, 2E for EMZF50P02J

ABC: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	A2	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.7	0		0.35	0.1	2.8	2.6	1.5	0.9		0.8	0.3	0.55
Typ.						2.9	2.8	1.6	0.95	1.9			
Max.	1.12	0.1		0.5	0.2	3	3	1.7	1		1.2	0.6	0.65

Footprint