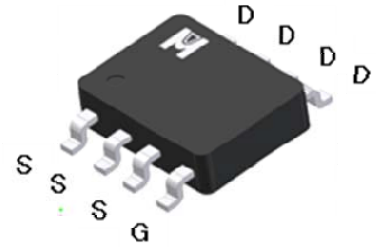


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	100V
$R_{DS(on)}$ (MAX.)	30m $\Omega$
$I_D$	9A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	9	A
	$T_A = 100\text{ }^\circ\text{C}$		6.4	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	36	
Avalanche Current		$I_{AS}$	9	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 9\text{A}, R_G = 25\text{ }\Omega$	$E_{AS}$	4	mJ
Repetitive Avalanche Energy <sup>2</sup>	$L = 0.05\text{mH}$	$E_{AR}$	2	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.5	W
	$T_A = 100\text{ }^\circ\text{C}$		1	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

**ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.0	1.7	3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 70V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	9			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 9A		26	30	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5A		28	35	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 9A		38		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 50V, f = 1MHz		2725		pF
Output Capacitance	C <sub>oss</sub>			209		
Reverse Transfer Capacitance	C <sub>rss</sub>			57		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz		1.5		Ω
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 9A		38		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			6.8		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			9.1		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 50V, I <sub>D</sub> = 1A, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 6Ω		25		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			110		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			100		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			120		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				2.3	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				9.2	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.3	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 9A, dI <sub>F</sub> /dt = 100A / μS		120		nS
Reverse Recovery Charge	Q <sub>rr</sub>			380		nC

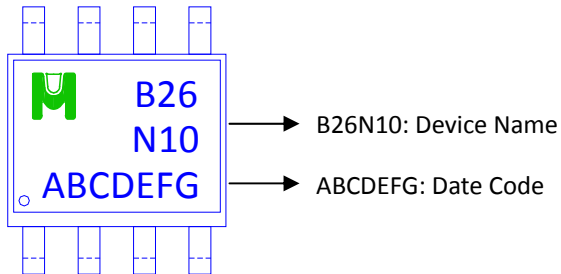
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

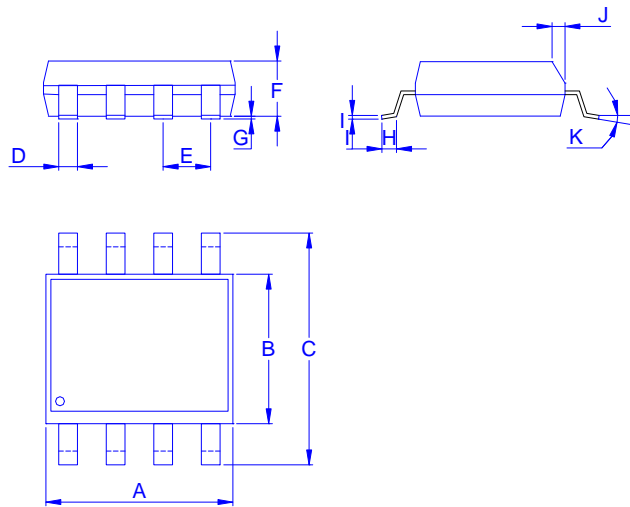
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB26N10G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



TYPICAL CHARACTERISTICS

