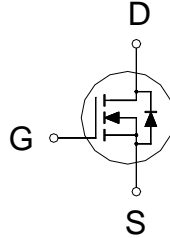


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	200V
$R_{DS(on) (MAX.)}$	$1 \Omega$
$I_D$	0.5A



Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	$I_D$	0.5	A
	$T_A = 100^\circ\text{C}$		0.3	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	2	
Power Dissipation	$T_A = 25^\circ\text{C}$	$P_D$	125	W
	$T_A = 70^\circ\text{C}$		0.8	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to- Ambient	$R_{\theta JA}$		100	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$



ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	200			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	4.0	5.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±30V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 130V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 5V, V <sub>GS</sub> = 10V	0.5			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.25A		0.9	1	Ω
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 0.25A		2		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1MHz		180		pF
Output Capacitance	C <sub>oss</sub>			38		
Reverse Transfer Capacitance	C <sub>rss</sub>			13		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz		3.5		Ω
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 0.25A		3.1		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			1.0		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			0.7		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = 100V, I <sub>D</sub> = 0.25A, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 6Ω		10		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			20		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			15		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				0.5	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				2	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.3	V

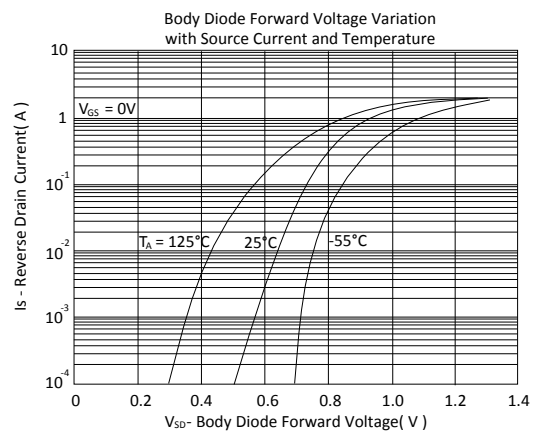
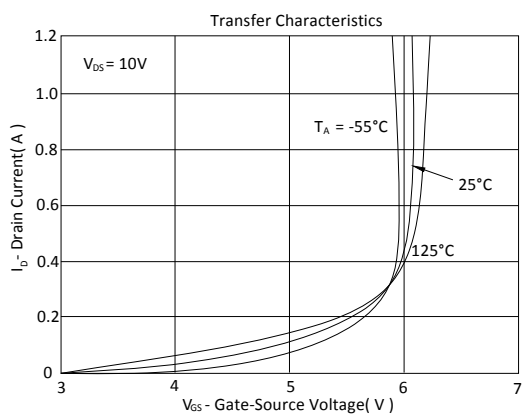
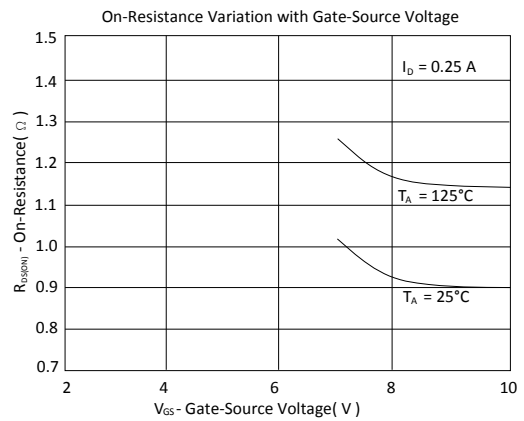
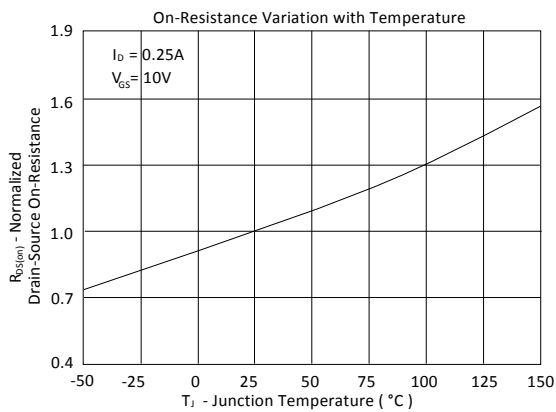
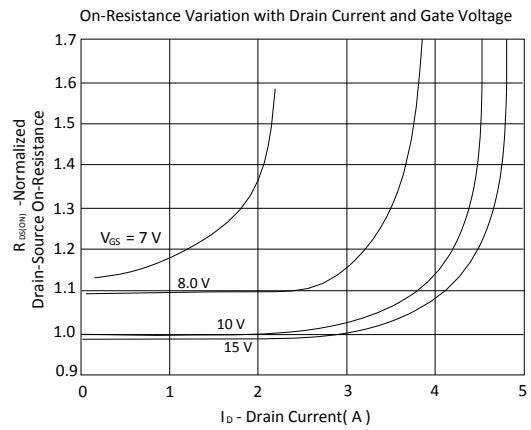
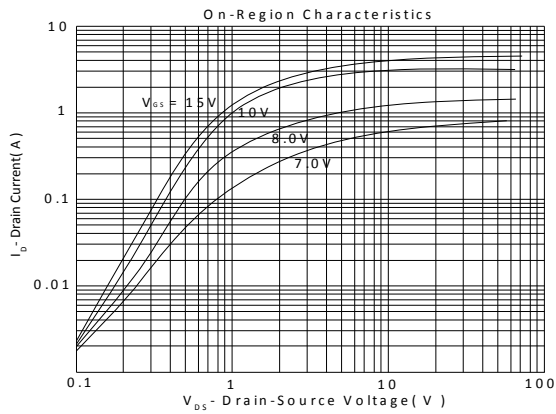
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

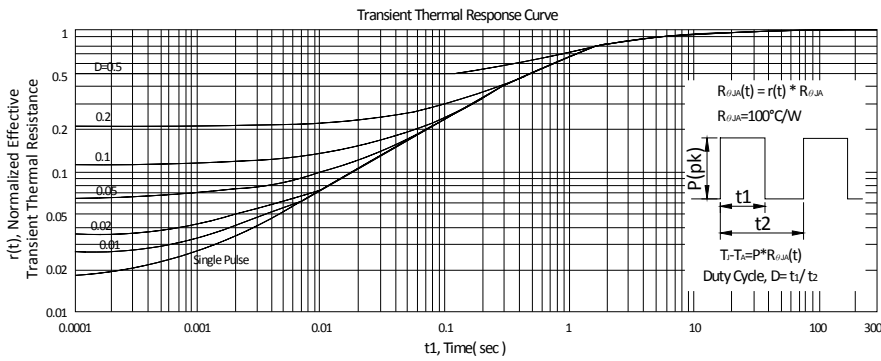
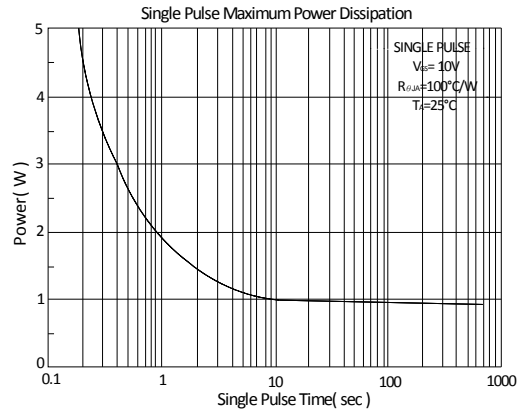
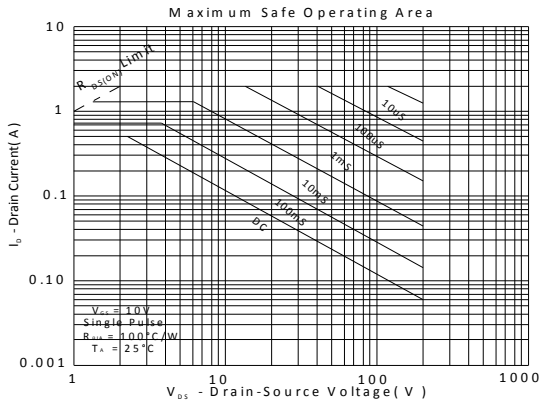
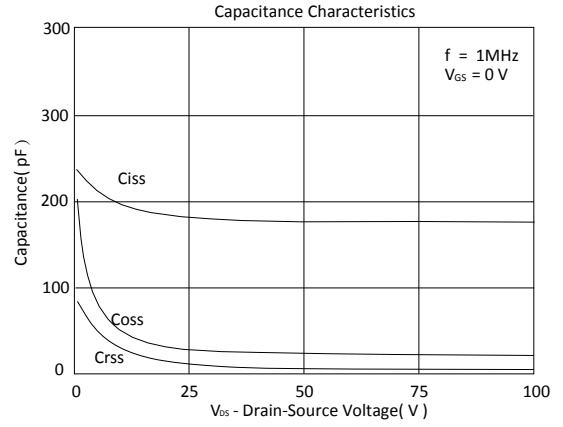
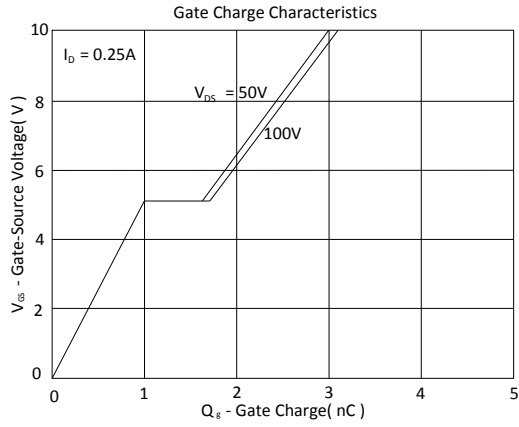
<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.



TYPICAL CHARACTERISTICS

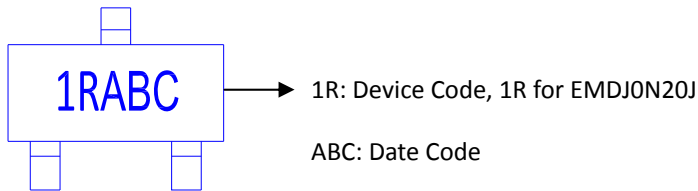




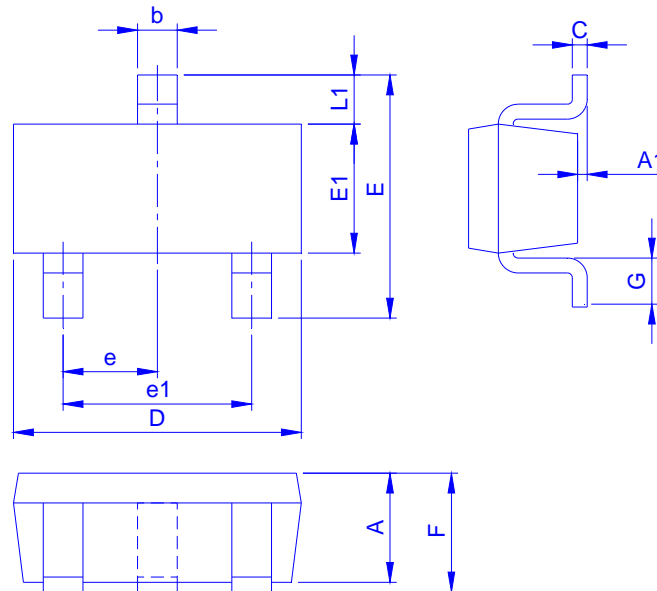


Ordering & Marking Information:

Device Name: EMDJ0N20J for SOT-23



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.7	0		0.35	0.1	2.8	2.6	1.5	0.9		0.8	0.3	0.55
Typ.						2.9	2.8	1.6	0.95	1.9			
Max.	1.12	0.1		0.5	0.2	3	3	1.7	1		1.2	0.6	0.65

Footprint

