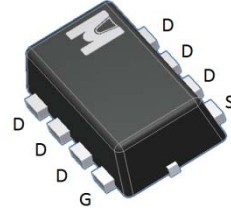
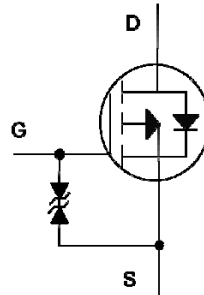


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-30V
R _{DS(on) (MAX.)}	24mΩ
I _D	-8A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free

ESD Protection



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±25	V
Continuous Drain Current	T _A = 25 °C	I _D	-8	A
	T _A = 70 °C		-6	
Pulsed Drain Current ¹		I _{DM}	-32	
Avalanche Current		I _{AS}	-10	
Avalanche Energy	L = 0.1mH, I _D = -10A, R _G = 25Ω	E _{AS}	5	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	2.5	
Power Dissipation ³	T _A = 25 °C	P _D	2.5	W
	T _A = 70 °C		1	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Lead	Steady-State	R _{θJL}		30	°C / W
Junction-to-Ambient ⁴	t ≤ 10s	R _{θJA}		50	
	Steady-State			90	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³The power dissipation P_D is based on T_{J(MAX)} = 150°C, using ≤ 10s junction-to-ambient thermal resistance.



⁴The value of $R_{\theta JA}$ is measured with mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 30	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-8			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -8A$		20	24	$m\Omega$
		$V_{GS} = -4.5V, I_D = -7A$		29	38	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -8A$		24		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		1407		pF
Output Capacitance	C_{oss}			208		
Reverse Transfer Capacitance	C_{rss}			164		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		4.5		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -8A$		20.3		nC
	$Q_g(V_{GS}=4.5V)$			10		
Gate-Source Charge ^{1,2}	Q_{gs}			3.2		
Gate-Drain Charge ^{1,2}	Q_{gd}			4.9		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		$V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 2.7\Omega$		10	
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			25		
Fall Time ^{1,2}	t_f			6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				-3	A
Pulsed Current ³	I_{SM}				-12	
Forward Voltage ¹	V_{SD}	$I_F = I_S A, V_{GS} = 0V$			-1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		32		nS
Reverse Recovery Charge	Q_{rr}			26		nC

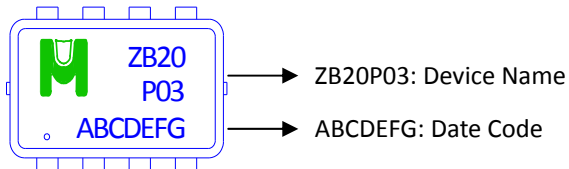
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

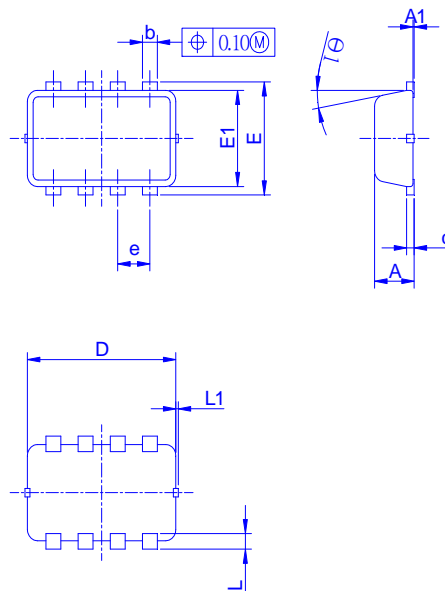
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMZB20P03L for DFN 3 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	E	E1	e	L	L1	θ
Min.	0.70	0.00	0.24	0.08					0.20	0.00	0°
Typ.					3.00	2.00	1.70	0.65			
Max.	0.90	0.05	0.35	0.25					0.40	0.10	12°

Recommended minimum pads

