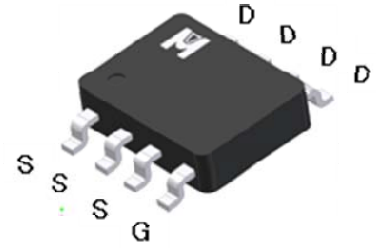
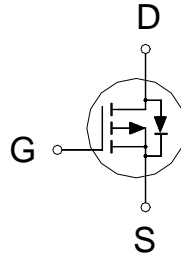


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

$BV_{DSS}$	-100V
$R_{DS(on)}$ (MAX.)	120m $\Omega$
$I_D$	-3.4A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	-3.4	A
	$T_A = 70\text{ }^\circ\text{C}$		-2.7	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-13.6	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.5	W
	$T_A = 70\text{ }^\circ\text{C}$		1.6	
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>50 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-2.0	-3.0	-4.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V			-1	μA
		V <sub>DS</sub> = -70V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			-10	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	-3.4			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -3.4A		105	120	mΩ
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -3.4A		8		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V, f = 1MHz		3520		pF
Output Capacitance	C <sub>oss</sub>			132		
Reverse Transfer Capacitance	C <sub>rss</sub>			115		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz		5.5		Ω
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -80V, V <sub>GS</sub> = 10V, I <sub>D</sub> = -3.4A		59		nC
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			14		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			11		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -1A, V <sub>GS</sub> = -10V, R <sub>GS</sub> = 6Ω		15		nS
Rise Time <sup>1,2</sup>	t <sub>r</sub>			45		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			50		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			50		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				-2.3	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				-9.2	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			-1.3	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / μS		150		nS
Reverse Recovery Charge	Q <sub>rr</sub>			830		nC

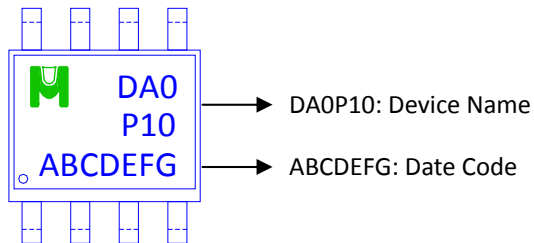
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

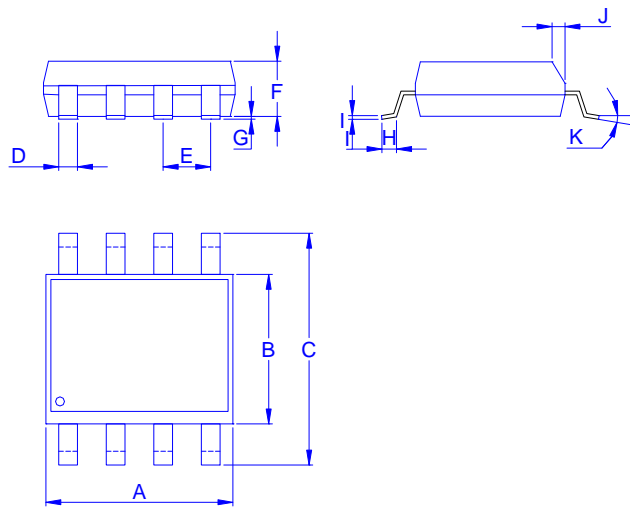
<sup>3</sup>Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMDA0P10G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

