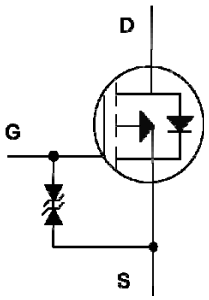
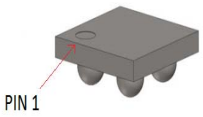
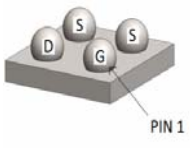
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-16V
$R_{DSON\ (MAX.)}$	100mΩ
I_D	-2.6A







Pb-Free Lead Plating & Halogen Free

ESD Protection

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_A = 25 °C	I_D	-2.6	A
	T_A = 70 °C		-2.0	
Pulsed Drain Current[1]		I_{DM}	-10	
Power Dissipation	T_A = 25 °C	P_D	1.3	W
	T_A = 70 °C		0.84	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3]	$R_{\theta JA}$		95	°C / W

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]95°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-16			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.35	-0.6	-0.85	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±30	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -12.8V, V_{GS} = 0V			-1	μA
		V_{DS} = -12.8V, V_{GS} = 0V, T_J = 125 °C			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-2.6			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -2A		80	100	mΩ
		V_{GS} = -2.5V, I_D = -1.5A		90	140	
		V_{GS} = -1.8V, I_D = -1A		105	190	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -2A		7		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -8V, f = 1MHz		535		pF
Output Capacitance	C_{oss}			98		
Reverse Transfer Capacitance	C_{rss}			84		
Total Gate Charge[1,2]	Q_g	V_{DS} = -8V, V_{GS} = -4.5V, I_D = -2A		8.1		nC
Gate-Source Charge[1,2]	Q_{gs}			0.9		
Gate-Drain Charge[1,2]	Q_{gd}			2.7		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -8V, I_D = -1A, V_{GS} = -4.5V, R_{GEN} = 6Ω		5		nS
Rise Time[1,2]	t_r			7		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			70		
Fall Time[1,2]	t_f			35		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				-2.6	A
Pulsed Current[3]	I_{SM}				-10	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

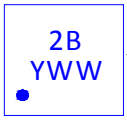
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

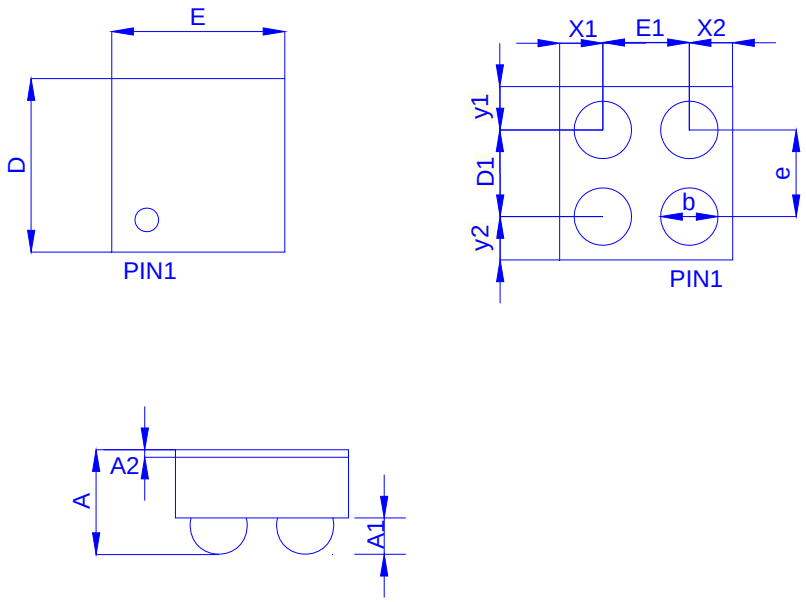
Device Name: EMZEA0P02Z for WLCSP



2B: Device Code, 2B for EMZEA0P02Z

YWW: Date Code

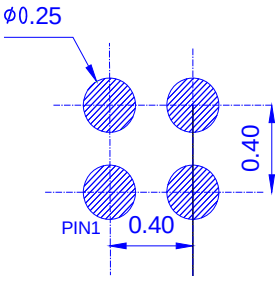
Outline Drawing



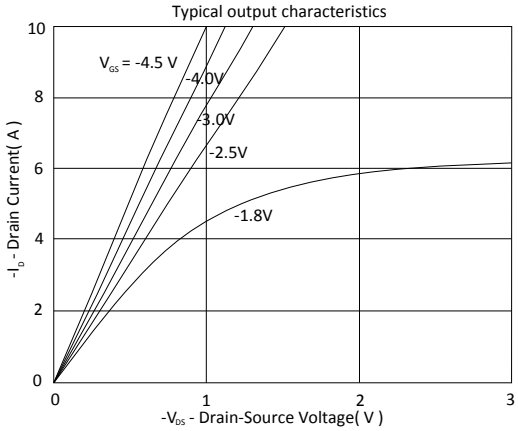
Dimension in mm

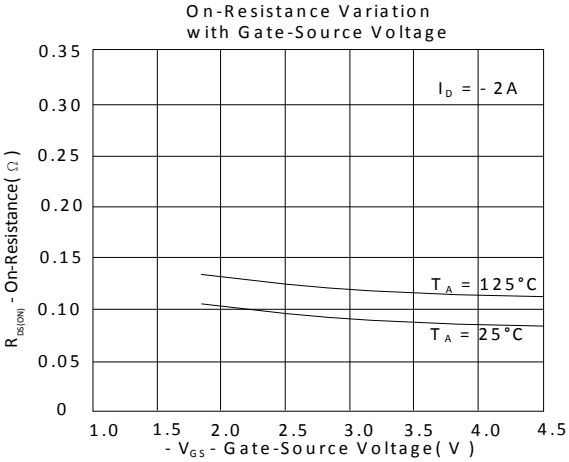
Dimension	A	A1	A2	D	D1	E	E1	b	e	X1	X2	y1	y2
Min.	0.463	0.168	0.020	0.770	0.400 (BSC)	0.770	0.400 (BSC)	0.265	0.400 (BSC)	0.200 (REF)	0.200 (REF)	0.200 (REF)	0.200 (REF)
Max.	0.503	0.228	0.050	0.830		0.830							

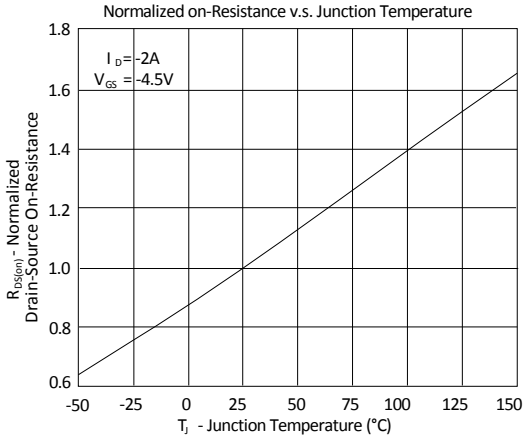
Footprint

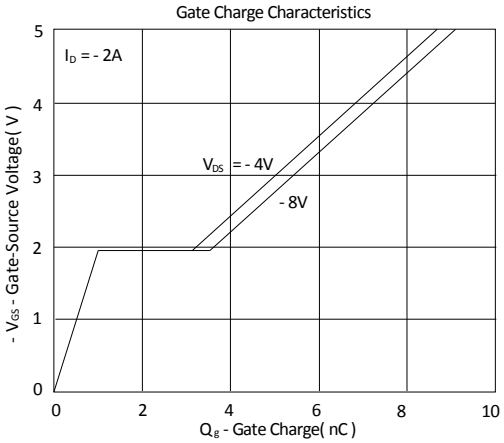


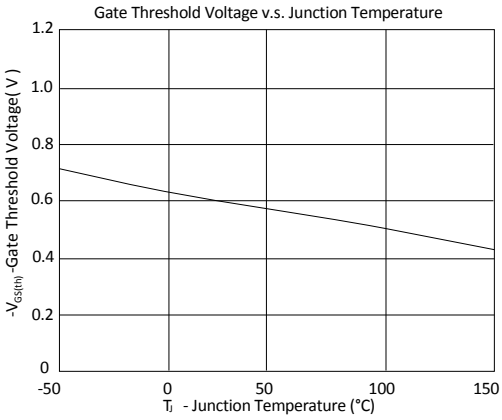
TYPICAL CHARACTERISTICS

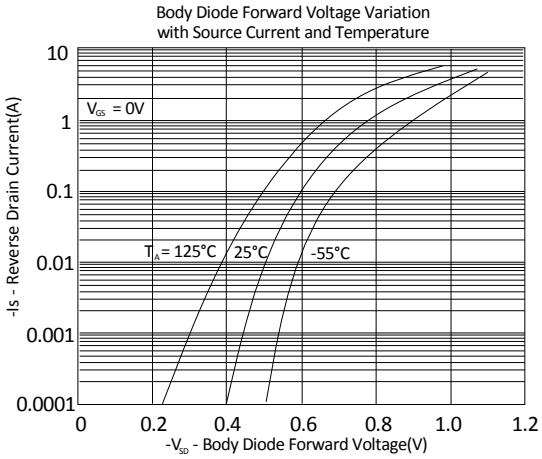


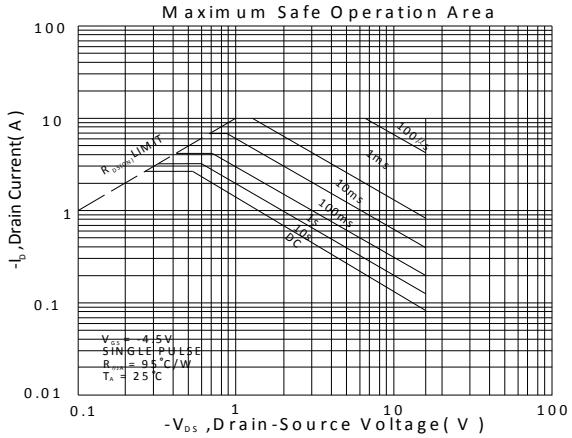


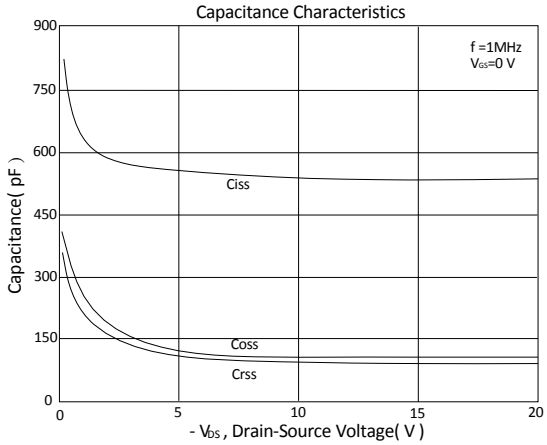


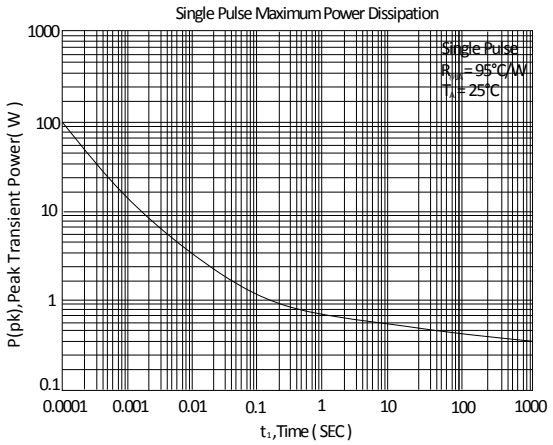


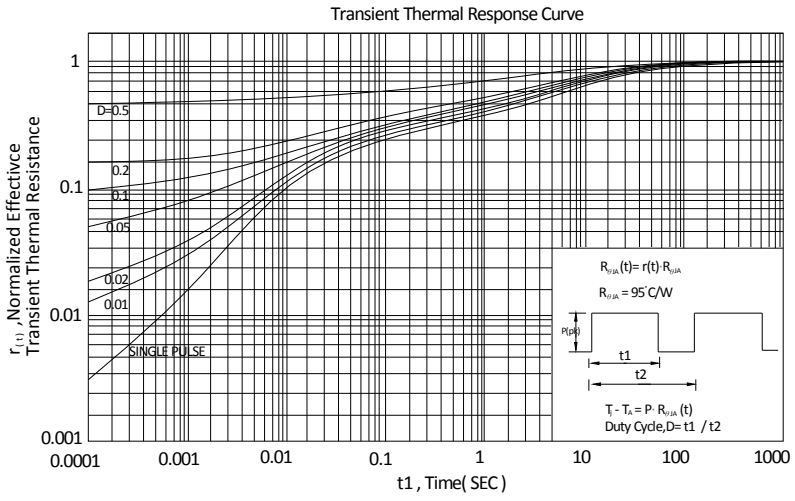





Maximum Safe Operation Area
-I_D ,Drain Current(A)
-V_DS ,Drain-Source Voltage(V)
100
10
1
0.1
0.01
0.1
1
10
100
R_DS(on) LIMIT
100μs
1ms
10ms
100ms
1s
10s
DC
V_GS = -4.5V
SINGLE PULSE
R_θJA = 95°C/W
T_A = 25°C


Capacitance Characteristics
Capacitance(pF)
- V_DS , Drain-Source Voltage(V)
f =1MHz
V_GS=0 V
900
750
600
450
300
150
0
0
5
10
15
20
Ciss
Coss
Crss


Single Pulse Maximum Power Dissipation
P(pk),Peak Transient Power(W)
t1,Time (SEC)
1000
100
10
1
0.1
0.0001
0.001
0.01
0.1
1
10
100
1000
Single Pulse
R_θJA = 95°C/W
T_A = 25°C


Transient Thermal Response Curve
r(t) ,Normalized Effectivce
Transient Thermal Resistance
t1 , Time(SEC)
1
0.1
0.01
0.001
0.0001
0.001
0.01
0.1
1
10
100
1000
D=0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE
R_θJA(t)= r(t)·R_θJA
R_θJA = 95°C/W
P(pk)
t1
t2
T_j - T_A = P· R_θJA (t)
Duty Cycle,D= t1 / t2