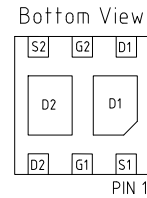
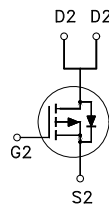
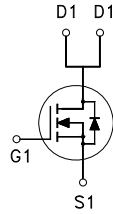


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
$BV_{DSS}$	20V	-20V
$R_{DS(on) (MAX.)}$	45m $\Omega$	100m $\Omega$
$I_D$	4.8A	-3.4A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		$V_{GS}$	N-CH	P-CH	V
			$\pm 12$	$\pm 12$	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	4.8	-3.4	A
	$T_A = 70\text{ }^\circ\text{C}$		3.8	-2.7	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	19.2	-13.6	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	1.9		W
	$T_A = 70\text{ }^\circ\text{C}$		1.2		
Operating Junction & Storage Temperature Range		$T_{j}, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		15	$^\circ\text{C} / \text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		65	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>65 $^\circ\text{C} / \text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$ $V_{GS} = 0V, I_D = -250\mu A$	N-CH	20		V
			P-CH	-20		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$ $V_{DS} = V_{GS}, I_D = -250\mu A$	N-CH	0.4	0.75	1.2
			P-CH	-0.3	-0.75	-1.2
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$ $V_{DS} = 0V, V_{GS} = \pm 12V$	N-CH			$\pm 100$
			P-CH			$\pm 100$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16V, V_{GS} = 0V$ $V_{DS} = -16V, V_{GS} = 0V$	N-CH			1
			P-CH			-1
			N-CH			10
			P-CH			-10
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 4.5V$ $V_{DS} = -5V, V_{GS} = -4.5V$	N-CH	4.8		A
			P-CH	-3.4		
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 3.5A$ $V_{GS} = -4.5V, I_D = -3A$ $V_{GS} = 2.5V, I_D = 2A$ $V_{GS} = -2.5V, I_D = -2A$	N-CH		36	45
			P-CH		83	100
			N-CH		43	60
			P-CH		110	135
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 3.5A$ $V_{DS} = -5V, I_D = -3A$	N-CH		5	S
			P-CH		4.5	
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	N-CH $V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$	N-CH		355	pF
			P-CH		420	
Output Capacitance	$C_{oss}$	P-CH $V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	N-CH		56	pF
			P-CH		56	
Reverse Transfer Capacitance	$C_{rss}$		N-CH		40	pF
			P-CH		42	



Total Gate Charge <sup>1,2</sup>	$Q_g$	N-CH $V_{DS} = 10V, V_{GS} = 4.5V,$ $I_D = 5A$ P-CH $V_{DS} = -10V, V_{GS} = -4.5V,$ $I_D = -3A$	N-CH		4.6		nC	
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$		P-CH		5.4			
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$		N-CH		0.66			
			P-CH		0.75			
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$		N-CH		8			nS
			P-CH		10			
Rise Time <sup>1,2</sup>	$t_r$	$I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$	N-CH		10			
			P-CH		20			
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$		P-CH $V_{DS} = -10V,$ $I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$	N-CH		20		
				P-CH		15		
Fall Time <sup>1,2</sup>	$t_f$	N-CH			15			
		P-CH			12			
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25^\circ C</math>)</b>								
Continuous Current	$I_S$		N-CH			2	A	
			P-CH			-2		
Pulsed Current <sup>3</sup>	$I_{SM}$		N-CH			8		
			P-CH			-8		
Forward Voltage <sup>1</sup>	$V_{SD}$		$I_F = I_S, V_{GS} = 0V$	N-CH			1.3	V
				P-CH			-1.3	

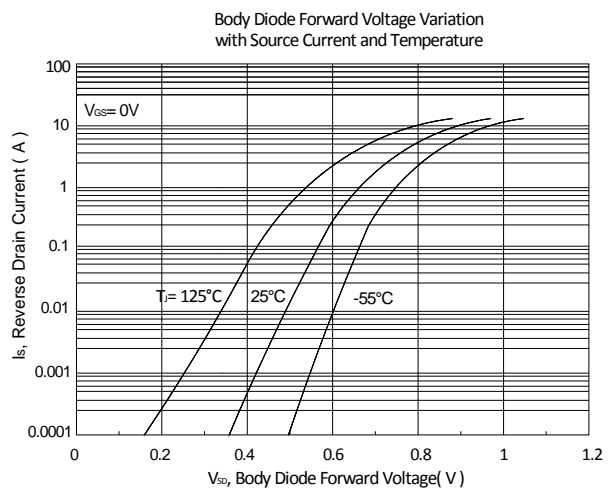
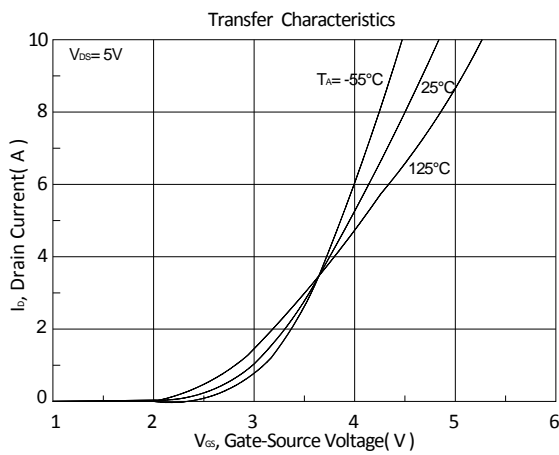
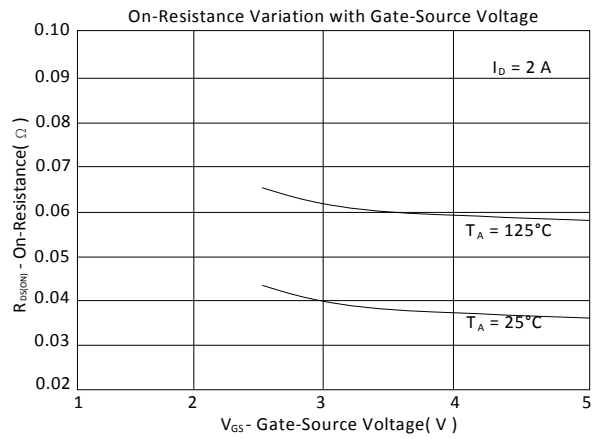
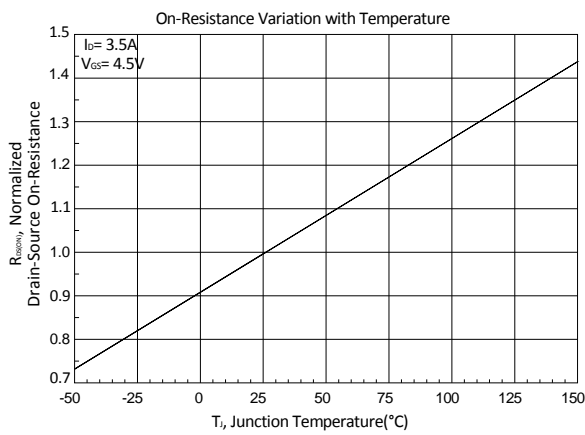
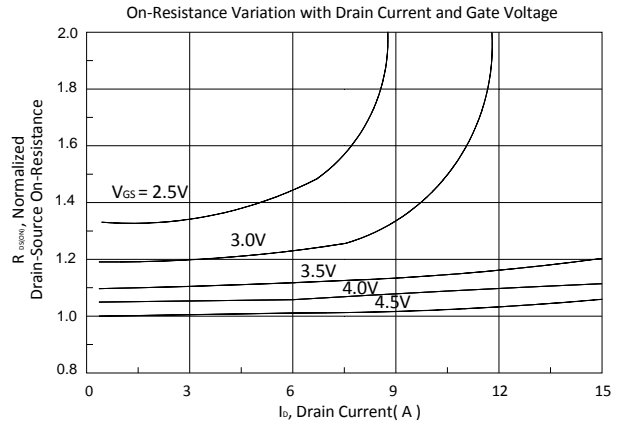
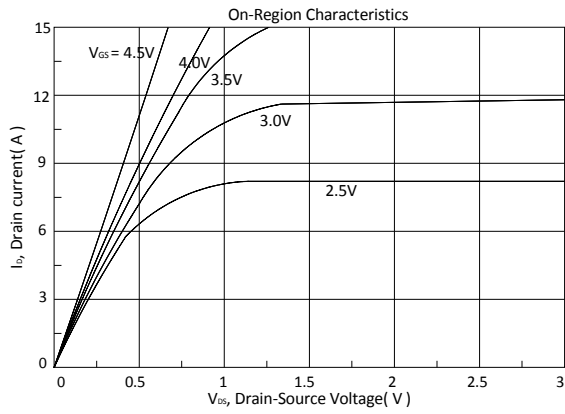
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

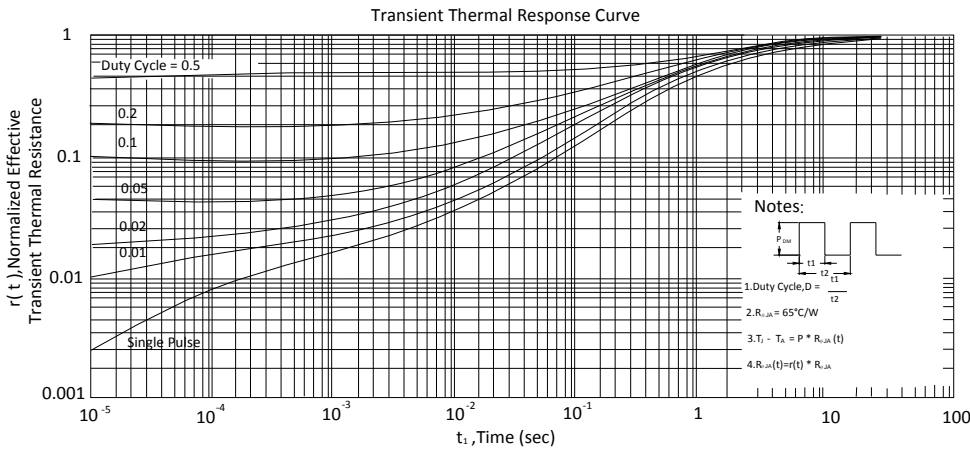
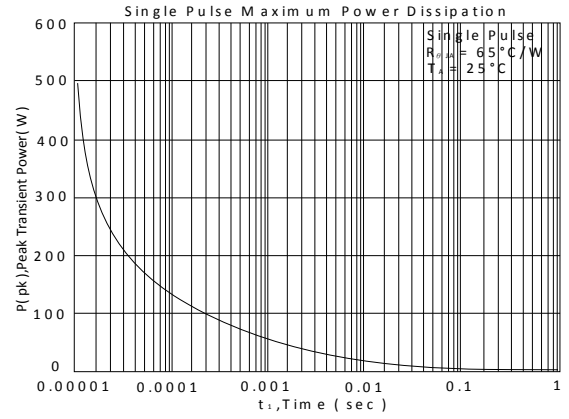
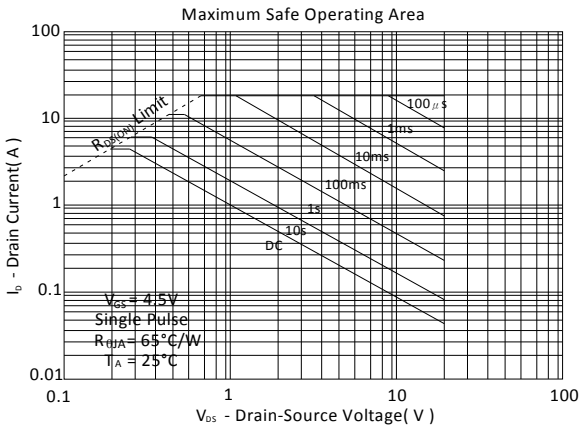
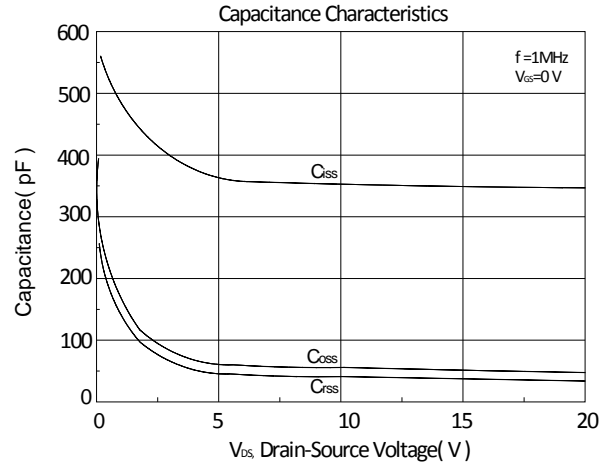
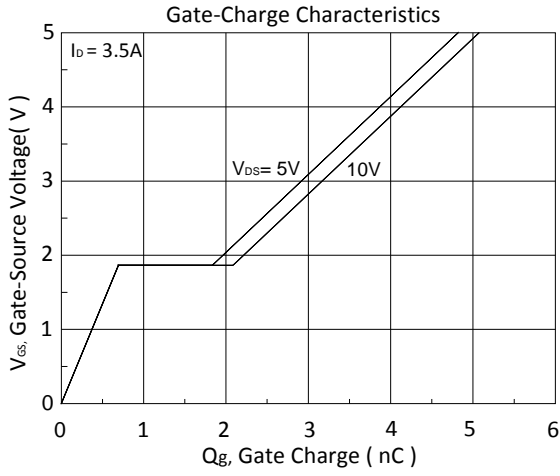
<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.



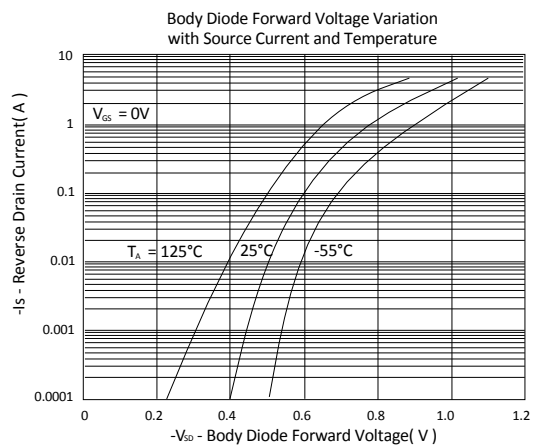
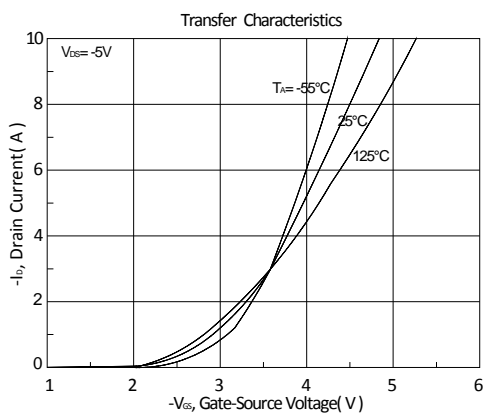
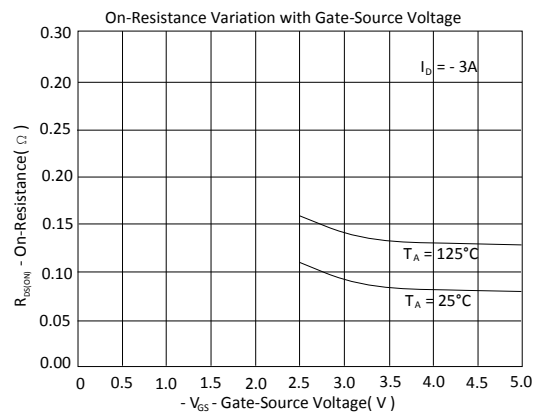
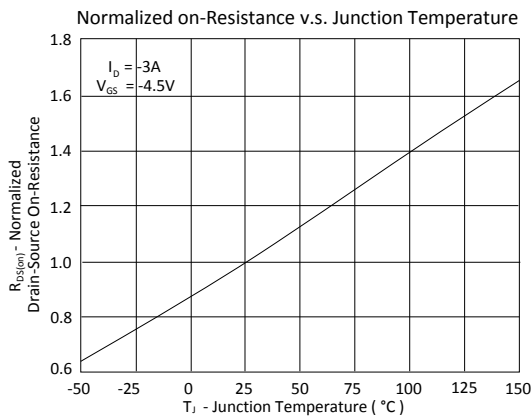
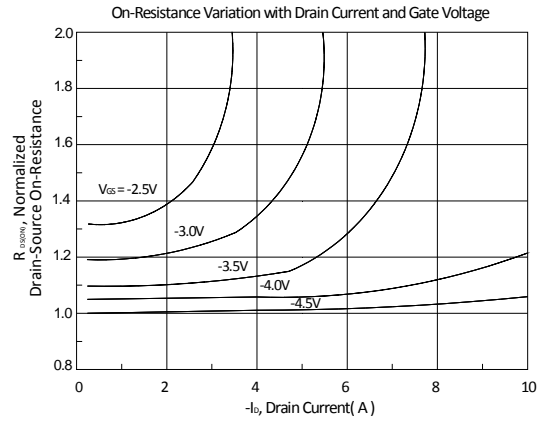
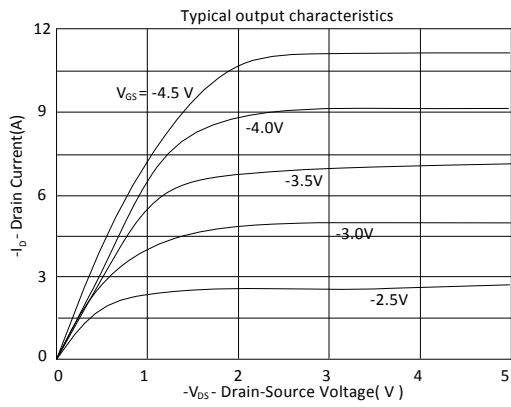
N-Channel

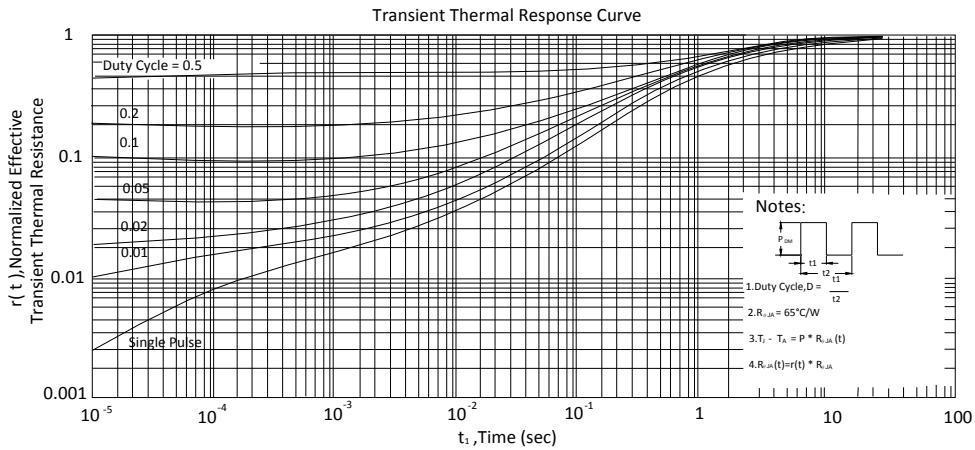
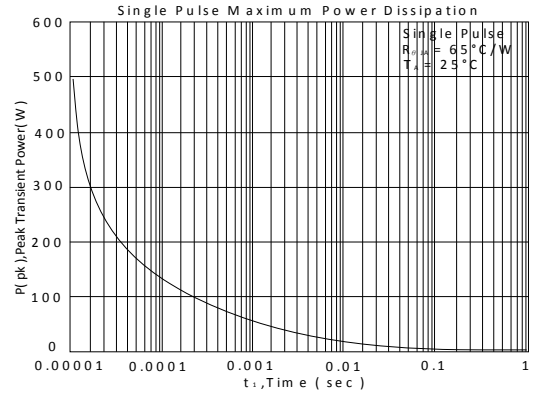
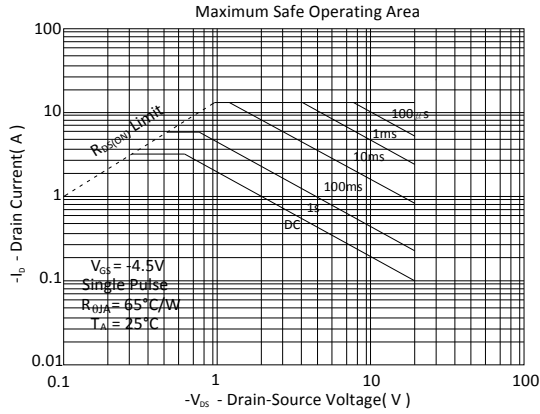
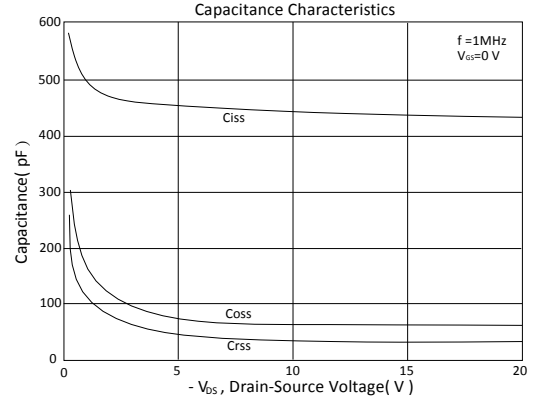
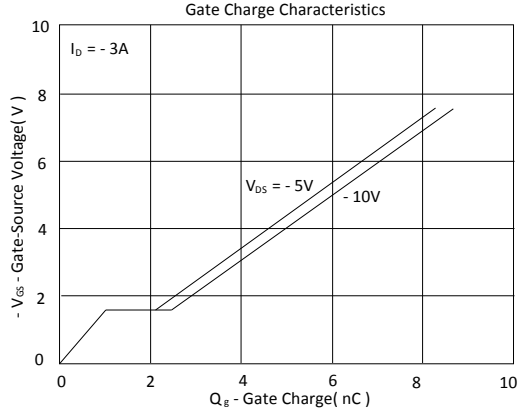






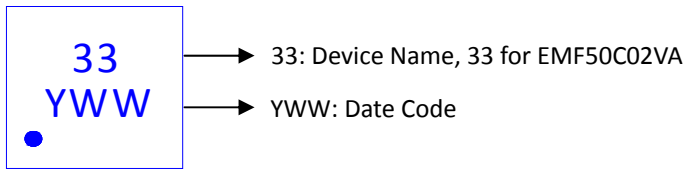
P-Channel



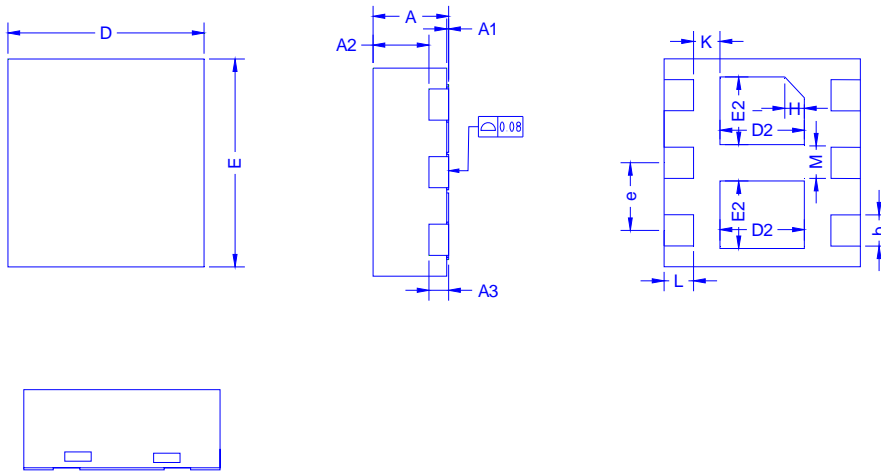


Ordering & Marking Information:

Device Name: EMF50C02VA for EDFN 2 x 2



Outline Drawing



Dimension in mm

Dimension	A	A1	A2	A3	b	D	E	D2	E2	e	H	K	L	M
Min.	0.70	0.00	0.50	0.20 REF	0.25	1.90	1.90	0.76	0.55	0.55	0.20 REF	0.17	0.25	0.25
Max.	0.80	0.05	0.60		0.35	2.10	2.10	0.96	0.75	0.75		0.37	0.35	0.45

Recommended minimum pads

