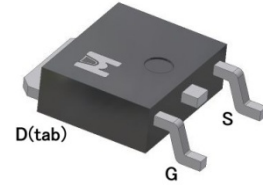


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	100V
R <sub>DS(on)</sub> (MAX.)	12mΩ
I <sub>D</sub>	68A



UIS, R<sub>g</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	68	A
	T <sub>C</sub> = 100 °C		43	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	150	
Avalanche Current		I <sub>AS</sub>	18	
Avalanche Energy	L = 0.1mH, I <sub>D</sub> =18A, R <sub>G</sub> =25Ω	E <sub>AS</sub>	16.2	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	8.1	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	89	W
	T <sub>C</sub> = 100 °C		35	
Operating Junction & Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		1.4	°C / W
Junction-to-Ambient	R <sub>θJA</sub>		62.5	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%



ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = 70V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	68			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$		9.5	12	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$		11.5	15	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 12A$		45		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = 50V, f = 1MHz$		2130		$pF$
Output Capacitance	$C_{oss}$			336		
Reverse Transfer Capacitance	$C_{rss}$			29		
Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.5		$\Omega$
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	$V_{DS} = 50V, V_{GS} = 10V,$ $I_D = 12A$		38		nC
	$Q_g(V_{GS}=4.5V)$			23		
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			10		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			8.2		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$		$V_{DS} = 50V,$ $I_D = 12A, V_{GS} = 10V, R_{GS} = 6\Omega$		6	
Rise Time <sup>1,2</sup>	$t_r$			10		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$			8		
Fall Time <sup>1,2</sup>	$t_f$			25		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_C = 25\text{ }^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				68	A
Pulsed Current <sup>3</sup>	$I_{SM}$				150	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = 12A, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = 12A, di_F/dt = 100A / \mu S$		30		nS
Reverse Recovery Charge	$Q_{rr}$			130		nC

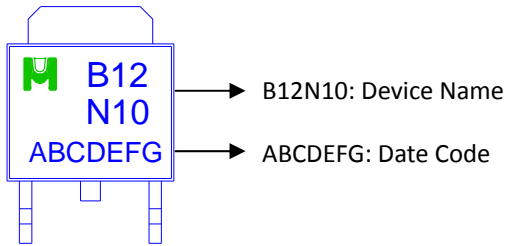
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\ \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

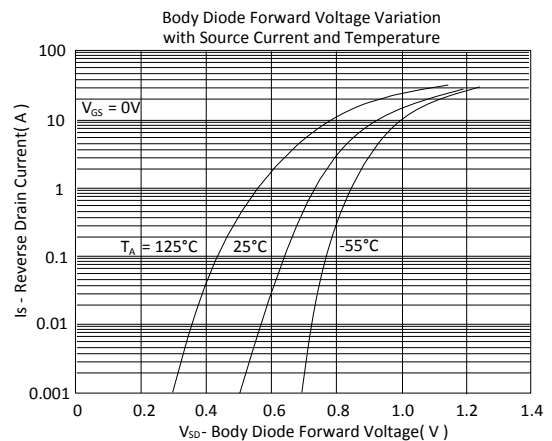
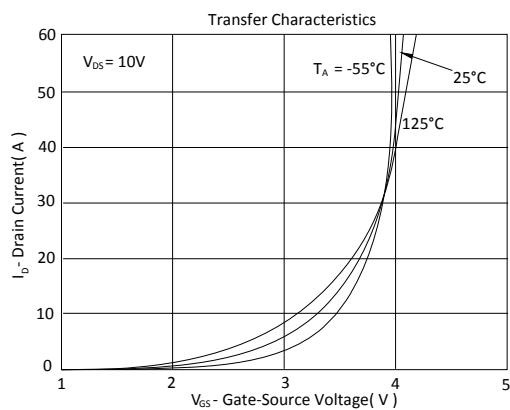
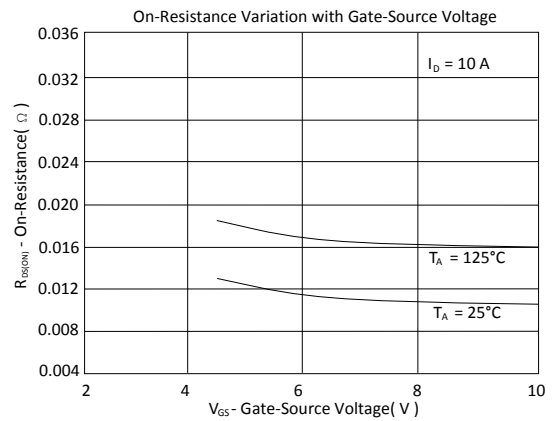
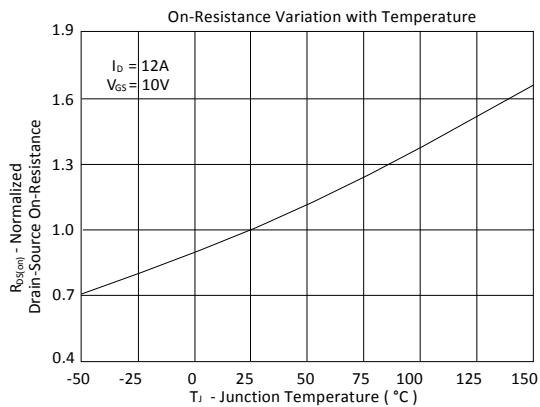
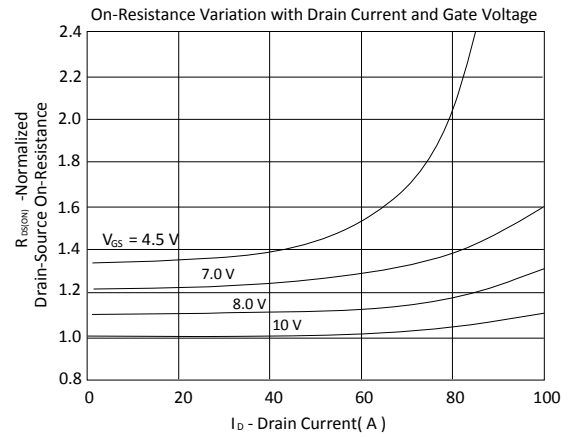
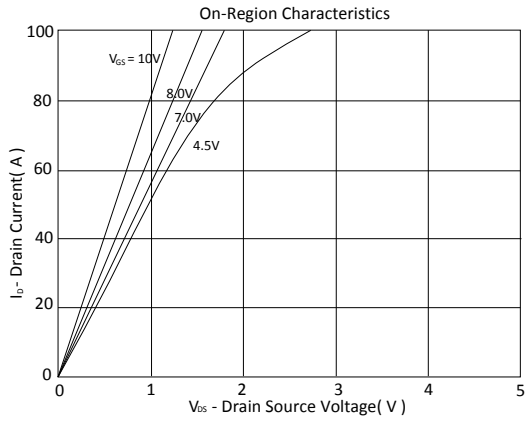
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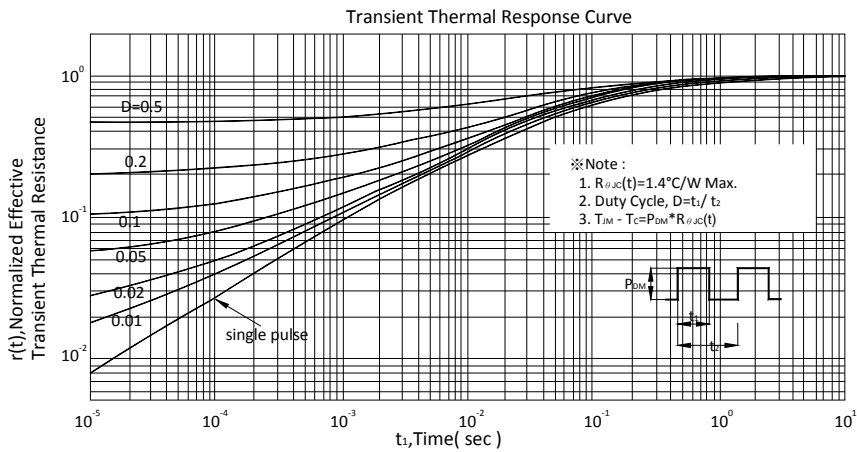
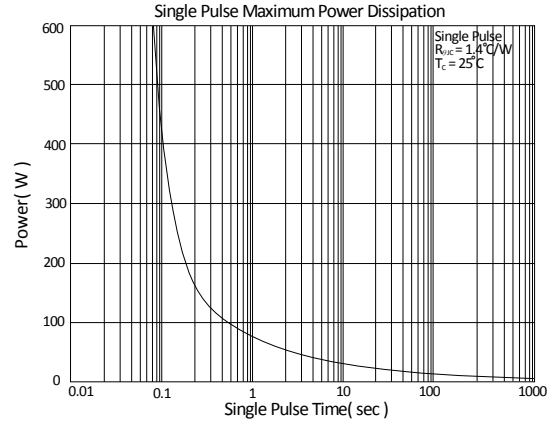
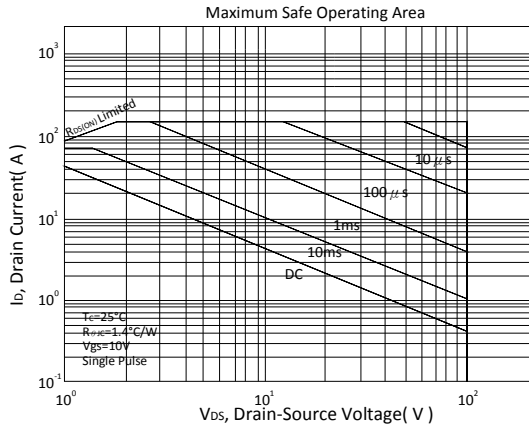
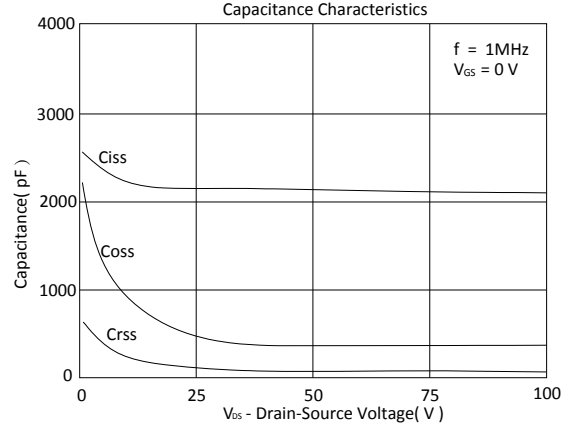
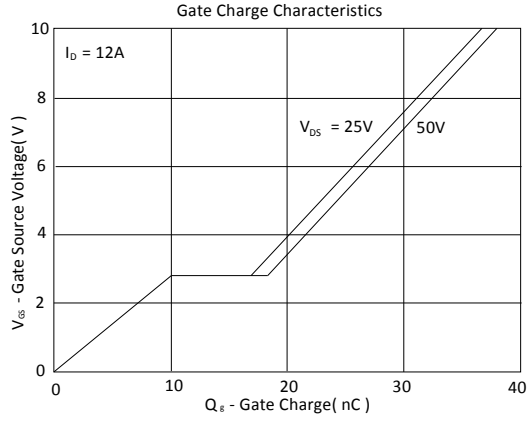
Device Name: EMB12N10A for DPAK (TO-252)





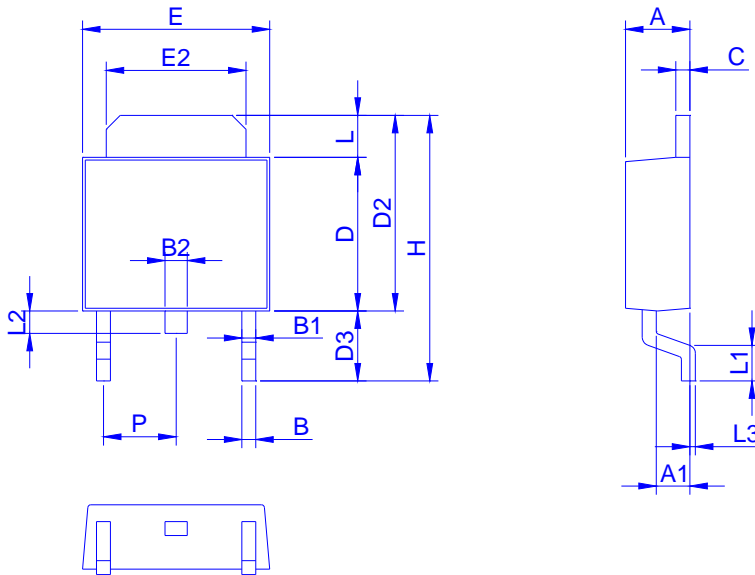
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint

