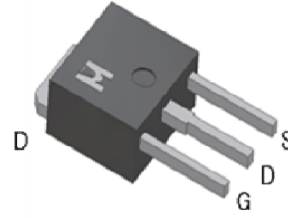


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)} (MAX.)$	14.6m Ω
I_D	62A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	62	A
	$T_C = 100\text{ }^\circ\text{C}$		39	
Pulsed Drain Current ¹		I_{DM}	240	
Avalanche Current		I_{AS}	60	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 70\text{A}, R_G = 25\Omega$	E_{AS}	245	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	122	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	89	W
	$T_C = 100\text{ }^\circ\text{C}$		35	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 50\text{V}$, $L = 0.1\text{mH}$, $V_G = 10\text{V}$, $I_L = 40\text{A}$, Rated $V_{DS} = 100\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.4	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	2.0	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	62			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		13	14.6	mΩ
		V _{GS} = 4.5V, I _D = 10A		15	20	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		42		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		4505		pF
Output Capacitance	C _{oss}			195		
Reverse Transfer Capacitance	C _{rss}			44		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.6		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 50V, V _{GS} = 10V, I _D = 20A		64		nC
Gate-Source Charge ^{1,2}	Q _{gs}			15		
Gate-Drain Charge ^{1,2}	Q _{gd}			11		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		20		nS
Rise Time ^{1,2}	t _r			25		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			80		
Fall Time ^{1,2}	t _f			30		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				62	A
Pulsed Current ³	I _{SM}				240	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 20A, dI _F /dt = 100A / μS		45		nS
Reverse Recovery Charge	Q _{rr}				90	

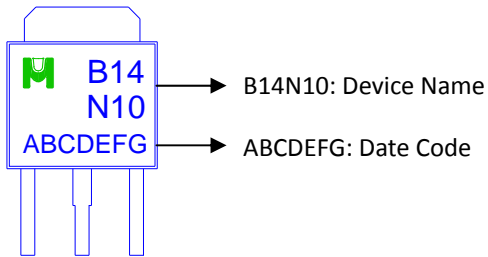
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

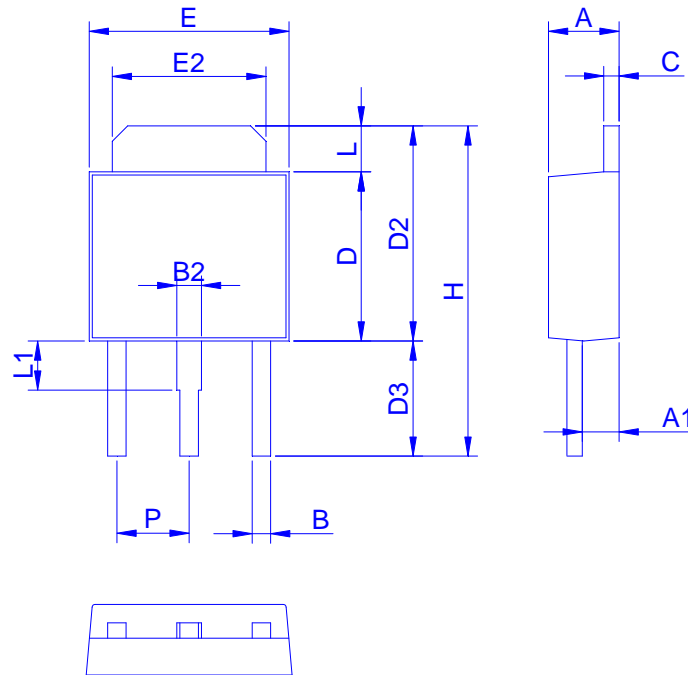
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB14N10CS for IPAK (TO-251)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50



TYPICAL CHARACTERISTICS

