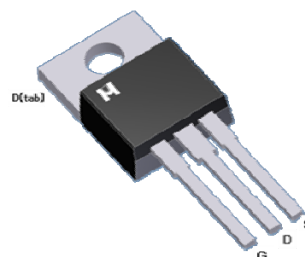
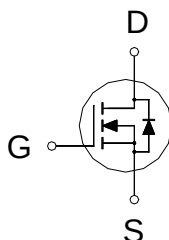


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	60V
$R_{DS(on)} (MAX.)$	4.0m Ω
I_D	150A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	150	A
	$T_C = 100^\circ\text{C}$		97	
Pulsed Drain Current ¹		I_{DM}	450	
Avalanche Current		I_{AS}	80	mJ
Avalanche Energy	$L = 0.1\text{mH}, I_D = 80\text{A}, R_G = 25\Omega$	E_{AS}	320	
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	160	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	166	W
	$T_C = 100^\circ\text{C}$		66	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 30\text{V}$, $L = 0.1\text{mH}$, $V_G = 10\text{V}$, $I_L = 50\text{A}$, Rated $V_{DS} = 60\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.75	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	3.0	3.9	4.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V			1	μA
		V _{DS} = 40V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	150			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 24A		3.4	4.0	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		57		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 30V, f = 1MHz		3260		pF
Output Capacitance	C _{oss}			965		
Reverse Transfer Capacitance	C _{rss}			155		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		2.5		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 30V, V _{GS} = 10V, I _D = 24A		46		nC
Gate-Source Charge ^{1,2}	Q _{gs}			18		
Gate-Drain Charge ^{1,2}	Q _{gd}			12		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 30V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		55		nS
Rise Time ^{1,2}	t _r			100		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			65		
Fall Time ^{1,2}	t _f			120		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				150	A
Pulsed Current ³	I _{SM}				450	
Forward Voltage ¹	V _{SD}	I _F = 24A, V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 24A, dI _F /dt = 100A / μS		25		nS
Reverse Recovery Charge	Q _{rr}			125		nC

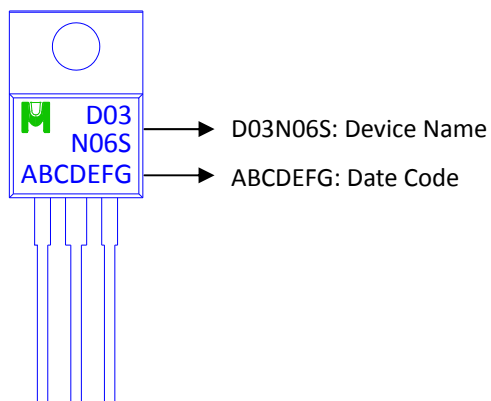
¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

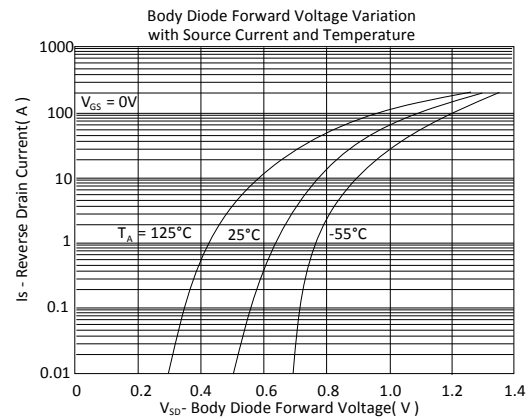
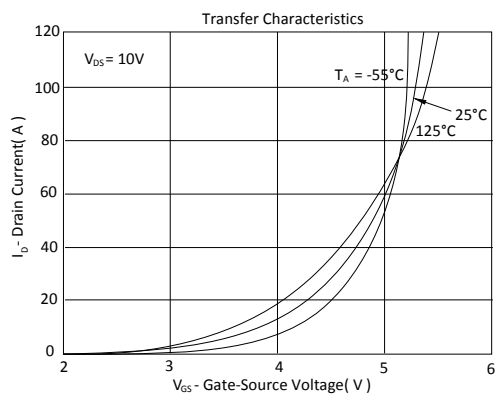
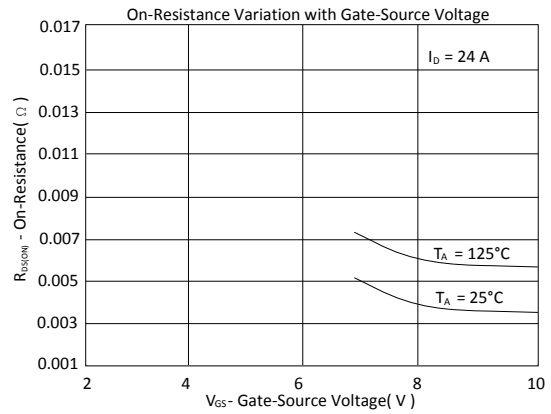
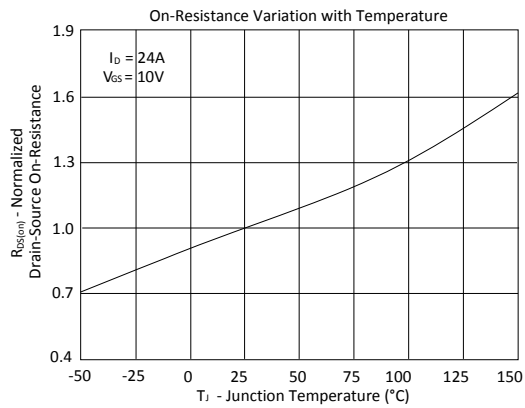
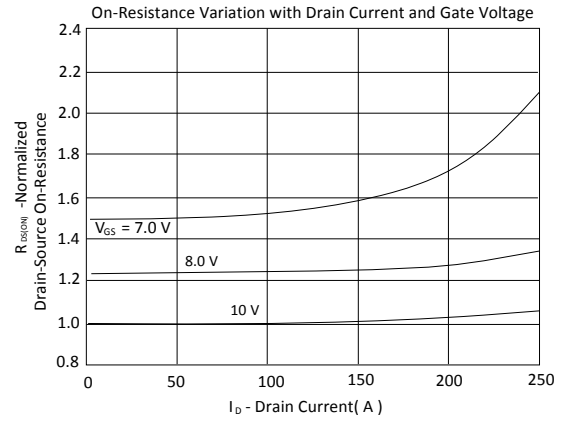
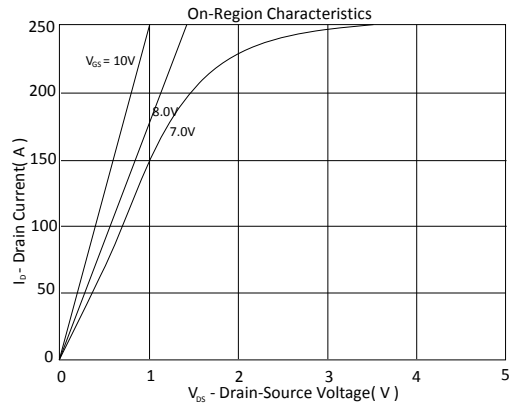
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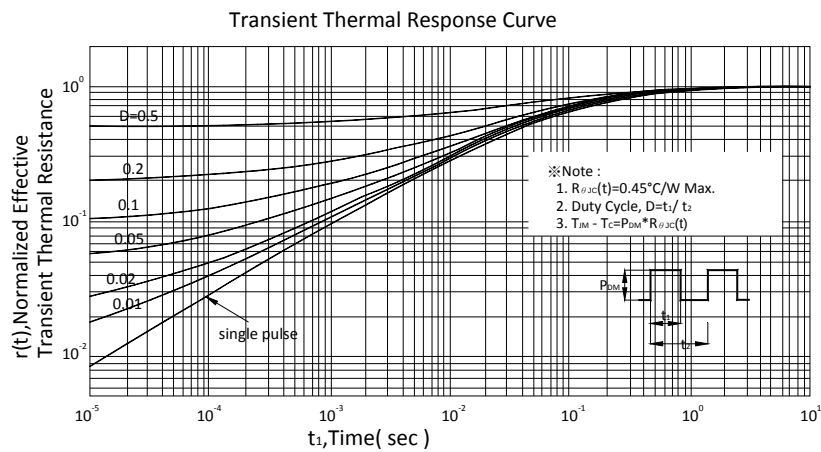
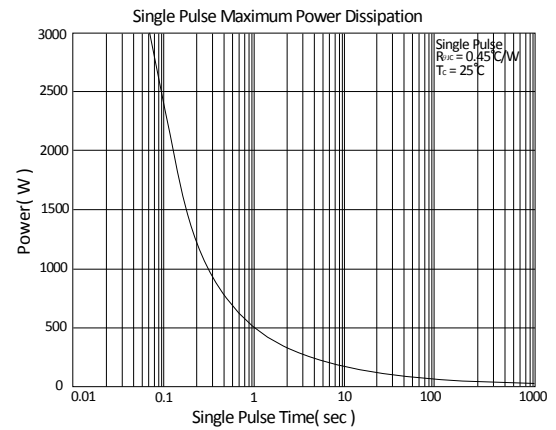
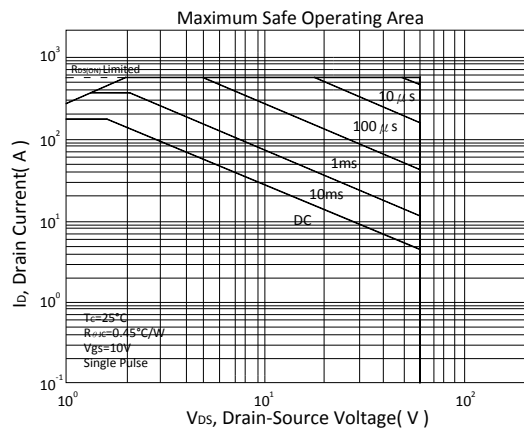
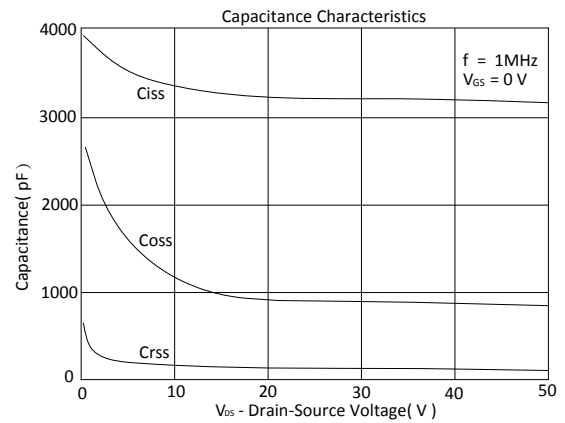
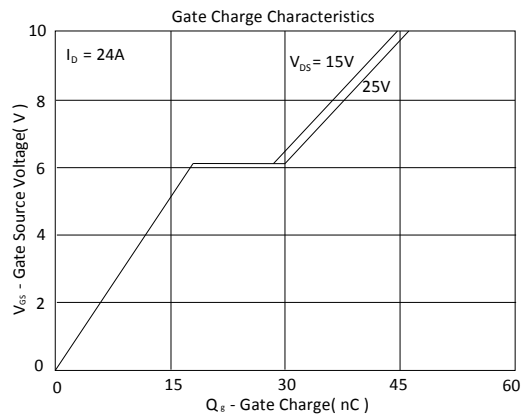
Device Name: EMD03N06ES for TO-220



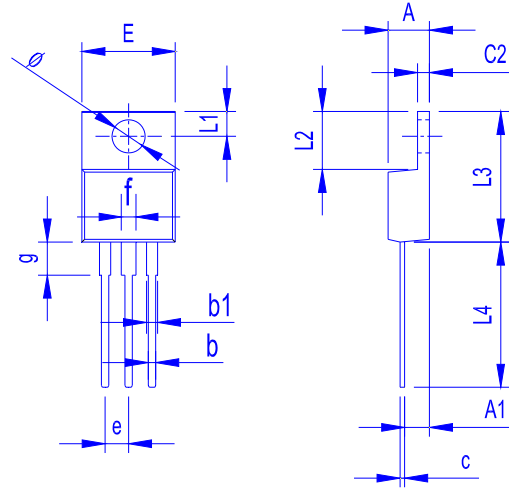


TYPICAL CHARACTERISTICS





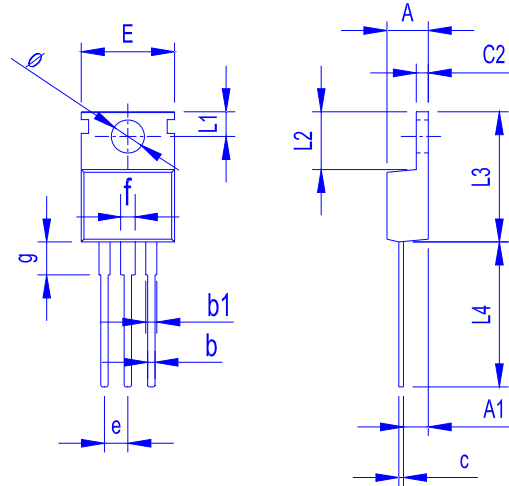
Outline Drawing A



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	∅	e	f	g
Min.	4.20	2.40	0.70	0.90	0.30	1.10	9.80	2.55	6.10	14.80	13.50	3.40	2.35	1.30	3.40
Max.	4.80	3.00	1.10	1.50	0.70	1.50	10.50	2.85	6.50	15.40	14.50	3.80	2.75	1.90	3.80

Outline Drawing B



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L1	L2	L3	L4	ø	e	f	g
Min.	4.20	2.20	0.70	1.17	0.30	1.10	9.66	2.55	6.10	14.80	12.70	3.40	2.35	1.17	2.60
Max.	4.80	2.60	1.10	1.72	0.70	1.50	10.50	3.00	6.85	16.10	14.50	3.80	2.75	1.90	3.80