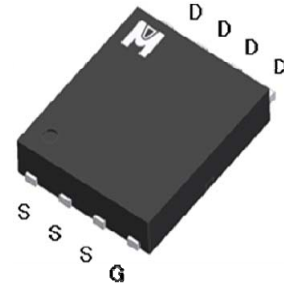
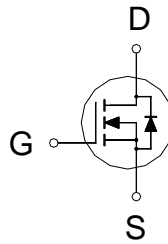


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	30V
$R_{DS(on)}$ (MAX.)	2.1m Ω
I_D	100A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ\text{C}$	I_D	100	A
	$T_C = 100^\circ\text{C}$		75	
Pulsed Drain Current ²		I_{DM}	400	
Avalanche Current		I_{AS}	65	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 65\text{A}, R_G = 25\Omega$	E_{AS}	211	mJ
Repetitive Avalanche Energy ³	$L = 0.05\text{mH}$	E_{AR}	105	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	50	W
	$T_C = 100^\circ\text{C}$		20	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 15\text{V}, L = 0.1\text{mH}, V_G = 10\text{V}, I_L = 40\text{A}$, Rated $V_{DS} = 30\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ⁴	$R_{\theta JA}$		50	

¹Package Limited.

²Pulse width limited by maximum junction temperature.

³Duty cycle $\leq 1\%$

⁴ $50^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
		V _{DS} = 20V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	100			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 25A		1.8	2.1	mΩ
		V _{GS} = 4.5V, I _D = 15A		2.7	3.3	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 25A		70		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		3813		pF
Output Capacitance	C _{oss}			540		
Reverse Transfer Capacitance	C _{rss}			440		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 25A		59		nC
	Q _g (V _{GS} =4.5V)			28		
Gate-Source Charge ^{1,2}	Q _{gs}			13		
Gate-Drain Charge ^{1,2}	Q _{gd}			11		
Turn-On Delay Time ^{1,2}	t _{d(on)}		V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 2.7Ω		25	
Rise Time ^{1,2}	t _r			16		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			60		
Fall Time ^{1,2}	t _f			25		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current ⁴	I _S				100	A
Pulsed Current ³	I _{SM}				400	
Forward Voltage ¹	V _{SD}	I _F = 30A, V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		35		nS
Peak Reverse Recovery Current	I _{RM(REC)}			200		A
Reverse Recovery Charge	Q _{rr}			25		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

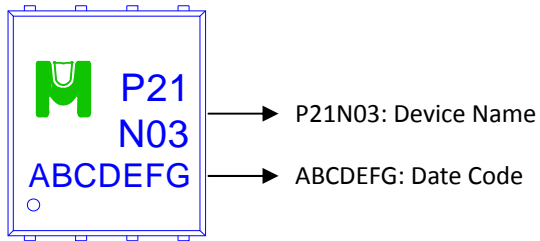
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Package Limited.

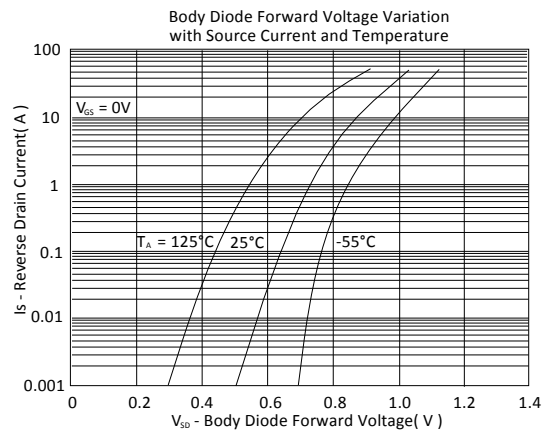
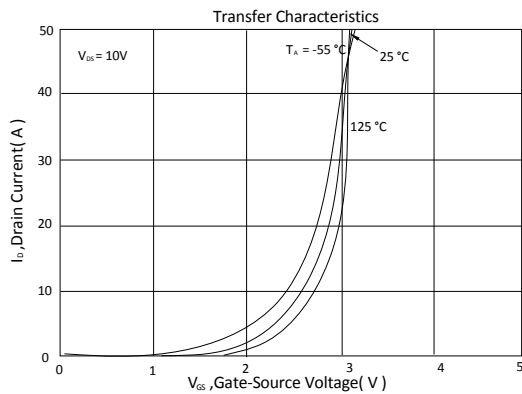
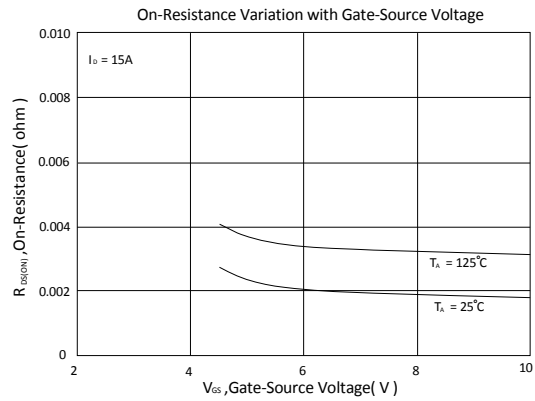
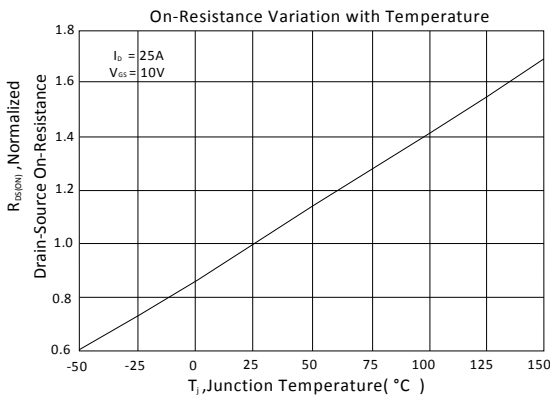
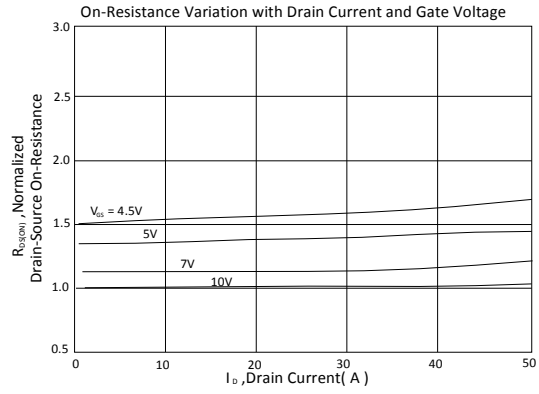
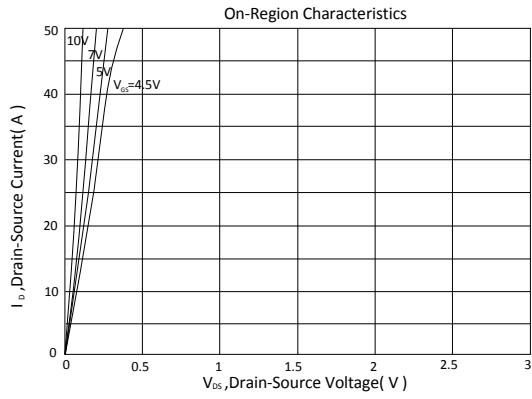
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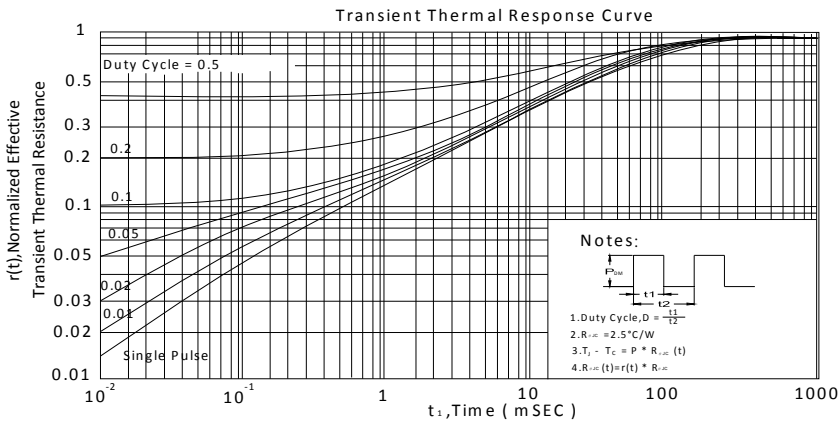
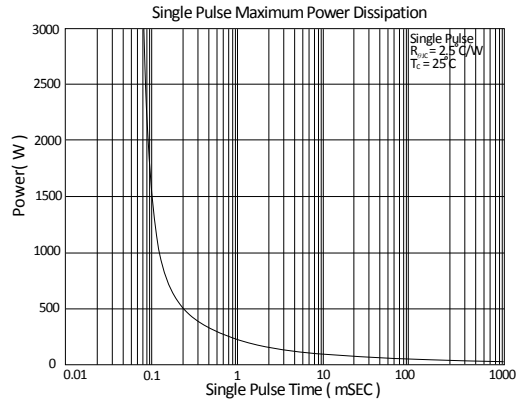
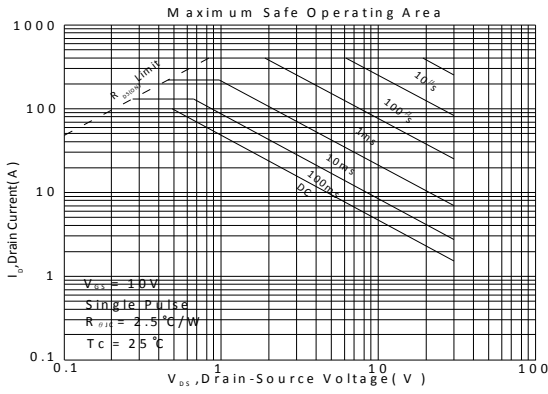
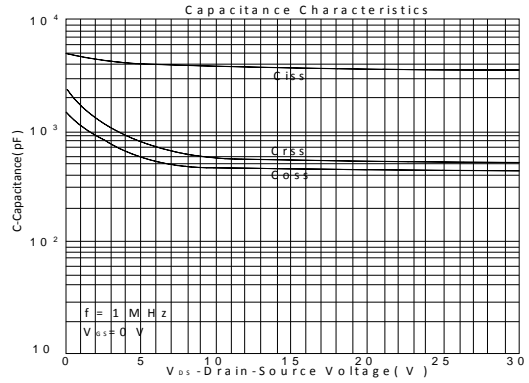
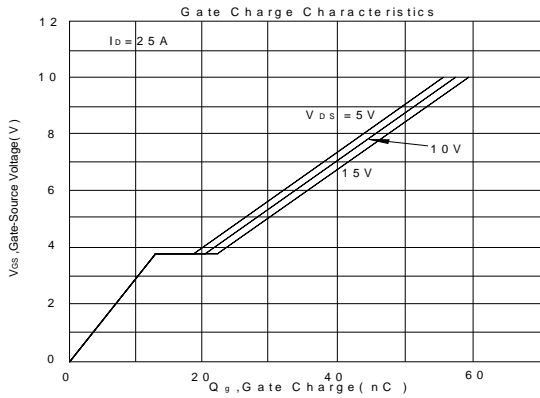
Device Name: EMP21N03HC for EDFN 5 x 6





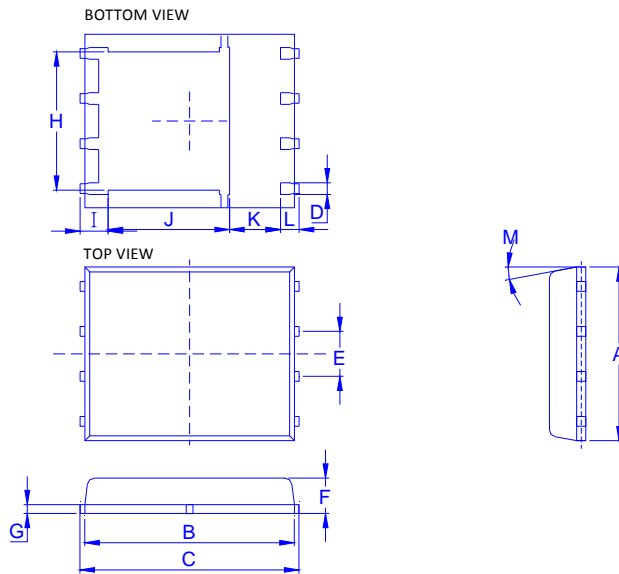
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

