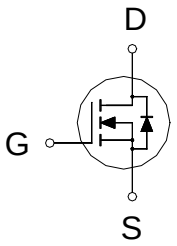
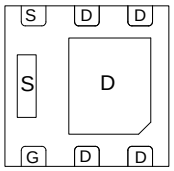
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DSON\ (MAX.)}$	14.8mΩ
I_D	8A



Bottom View



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	8	A
	T_A = 70 °C		6.2	
Pulsed Drain Current[1]		I_{DM}	32	
Avalanche Current		I_{AS}	10	
Avalanche Energy	L = 0.1mH, ID=10A, RG=25Ω	E_{AS}	5	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	E_{AR}	2.5	
Power Dissipation	T_A = 25 °C	P_D	2.08	W
	T_A = 70 °C		1.33	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		12	°C / W
Junction-to-Ambient[3]	$R_{\theta JA}$		60	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]60°C / W when mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.4	0.75	1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 4.5V	8			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 8A		13	14.8	mΩ
		V_{GS} = 2.5V, I_D = 5A		19	23	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 8A		9		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		1192		pF
Output Capacitance	C_{oss}			203		
Reverse Transfer Capacitance	C_{rss}			174		
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 8A		14.2		nC
Gate-Source Charge[1,2]	Q_{gs}			1.8		
Gate-Drain Charge[1,2]	Q_{gd}			5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		15		nS
Rise Time[1,2]	t_r			18		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			35		
Fall Time[1,2]	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				8	A
Pulsed Current[3]	I_{SM}				32	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

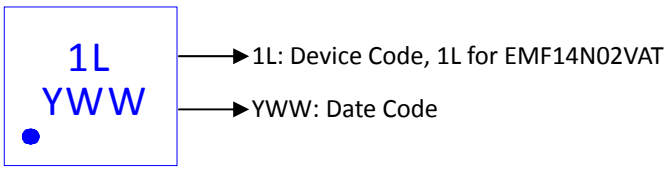
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

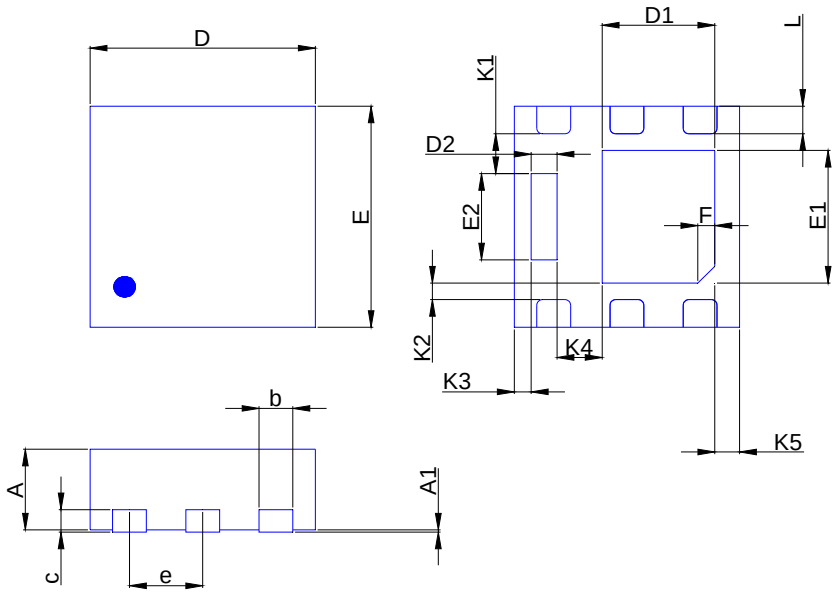
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMF14N02VAT for EDFN 2 x 2



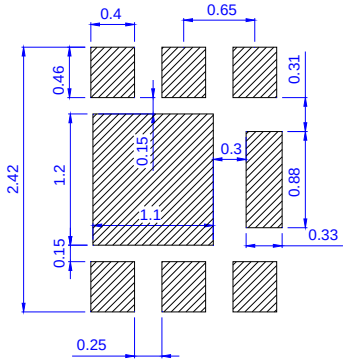
Outline Drawing



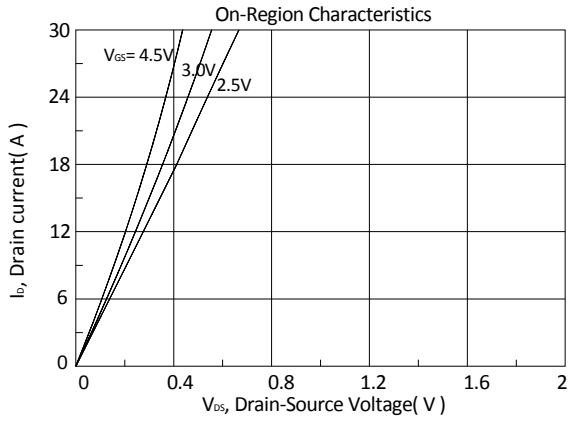
Dimension in mm

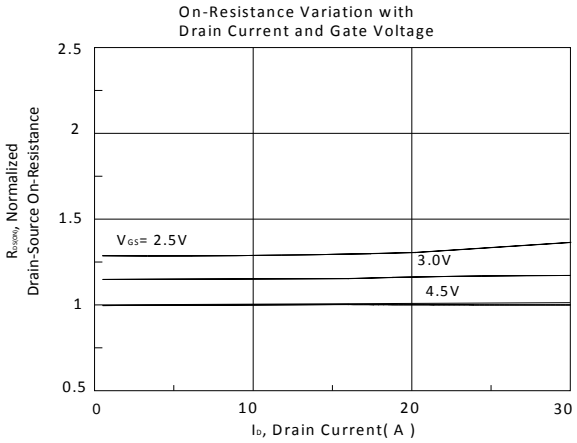
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	F	f	K1	K2	L	K3	K4	K5
Min.	0.50	0.00	0.25		1.9	1.0	0.13	1.9	1.1	0.65				0.306	0.10	0.2	0.10	0.27	0.17
Typ.		0.02	0.30	0.1	2.0	1.1	0.25	2.0	1.2	0.75	0.65	0.15	45°	0.356	0.15	0.25	0.15		0.22
Max.	0.65	0.05	0.35		2.1	1.2	0.35	2.1	1.3	0.88				0.406	0.20	0.3	0.20		0.27

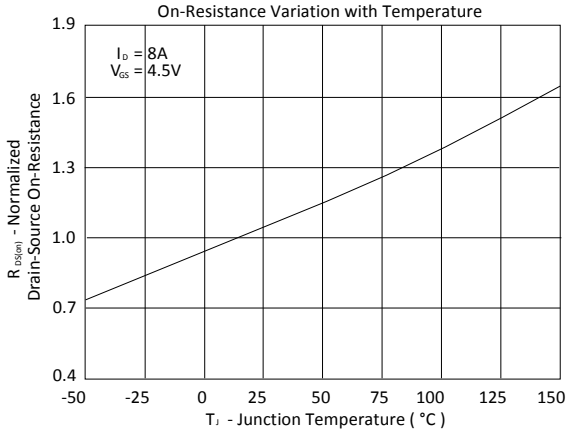
Recommended minimum pads

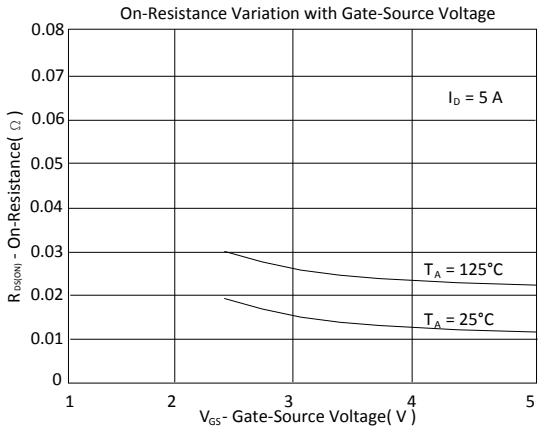


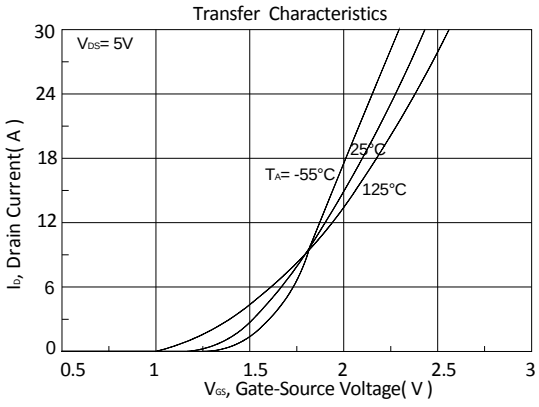
TYPICAL CHARACTERISTICS

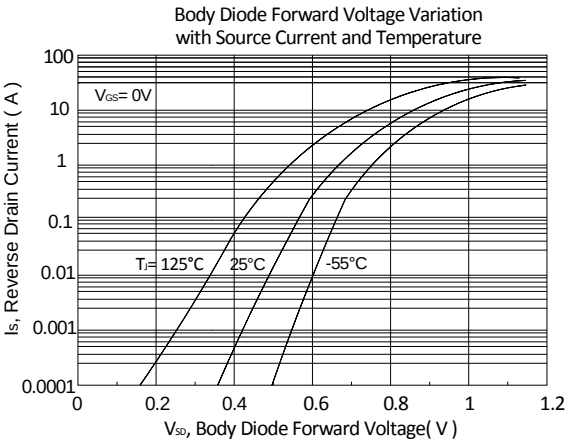




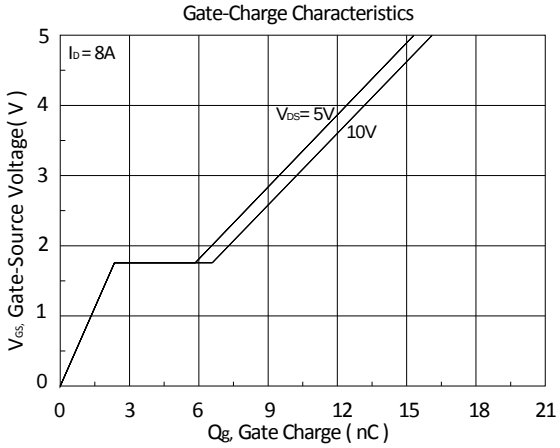




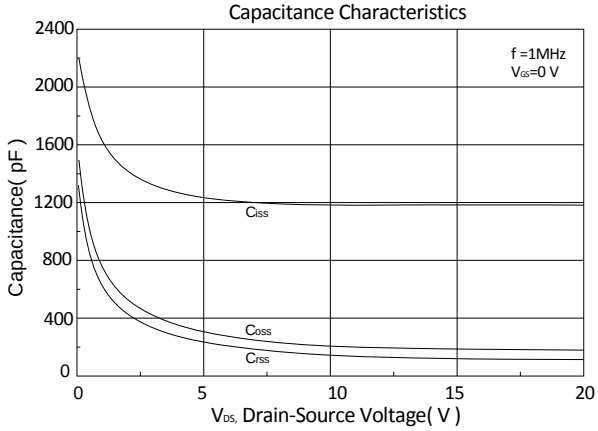




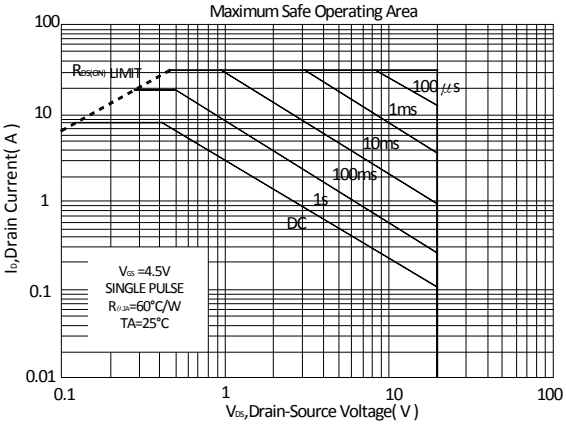
Gate-Charge Characteristics



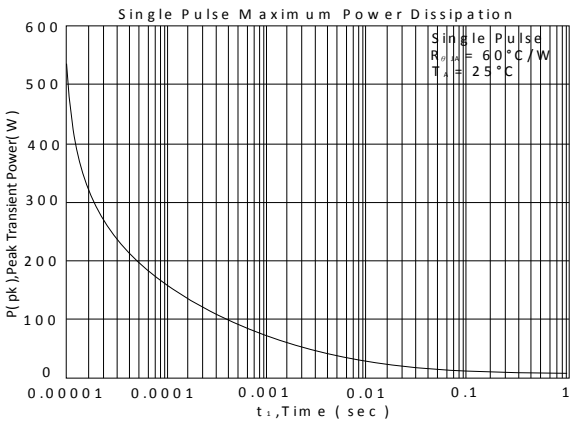
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve