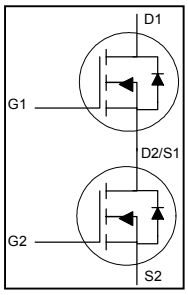
AP3D5R0MT

Halogen-Free Product

Advanced Power Electronics Corp.

DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Easy for Synchronous Buck Converter Application**
- ▼ **RoHS Compliant & Halogen-Free**

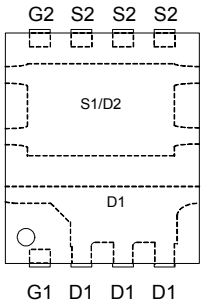


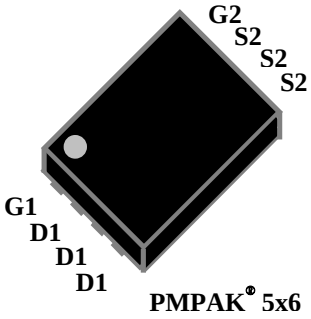
CH-1	BV_{DSS}	30V
	$R_{DS(ON)}$	11.5mΩ
CH-2	BV_{DSS}	30V
	$R_{DS(ON)}$	5mΩ

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The control MOSFET (CH-1) and synchronous MOSFET (CH-2) co-package for synchronous buck converters.





Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V (Silicon Limited)	34	74	A
I_D@T_A=25℃	Drain Current[3] , V_{GS} @ 10V	13.2	22.7	A
I_D@T_A=70℃	Drain Current[3] , V_{GS} @ 10V	10.5	18.2	A
I_{DM}	Pulsed Drain Current[1]	40	60	A
P_D@T_A=25℃	Total Power Dissipation	3.13	3.9	W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Rating		Units
		CH-1	CH-2	
Rthj-c	Maximum Thermal Resistance, Junction-case	6	3	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	40	32	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[4]	70	60	℃/W

CH-1 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=10A	-	-	11.5	mΩ
		V_{GS}=4.5V, I_D=6A	-	-	21.5	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=10A	-	24	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=10A	-	10	16	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	3.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	3.5	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	7	-	ns
t_r	Rise Time	I_D=1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	19	-	ns
t_f	Fall Time	V_{GS}=10V	-	4.5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1100	1760	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	120	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	85	-	pF
R_g	Gate Resistance	f=1.0MHz	-	0.9	1.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=10A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=10A, V_{GS}=0V,	-	8.5	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	2.4	-	nC

CH-2 Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V, I_D=18A	-	-	5	mΩ
		V_{GS}=4.5V, I_D=10A	-	-	8	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	3	V
g_{fs}	Forward Transconductance	V_{DS}=5V, I_D=18A	-	55	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V, V_{GS}=0V	-	-	10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=18A	-	20	32	nC
Q_{gs}	Gate-Source Charge	V_{DS}=15V	-	4.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	11	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V	-	8	-	ns
t_r	Rise Time	I_D=1A	-	9	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	32	-	ns
t_f	Fall Time	V_{GS}=10V	-	18	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	1430	2288	pF
C_{oss}	Output Capacitance	V_{DS}=15V	-	385	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	270	-	pF
R_g	Gate Resistance	f=1.0MHz	-	1	2	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=18A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time	I_S=18A, V_{GS}=0V,	-	23	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	11	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec.

4.Surface mounted on 1 in^2 copper pad of FR4 board, on steady-state

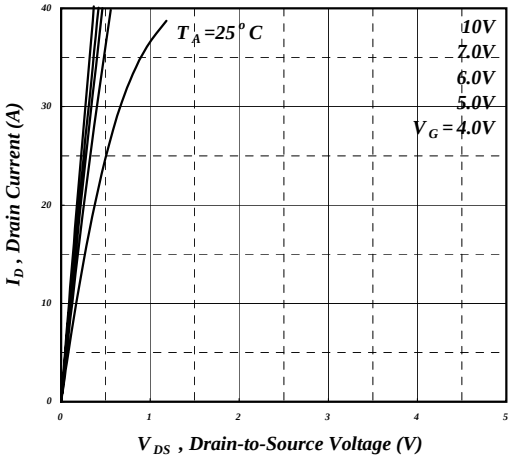


Fig 1. Typical Output Characteristics

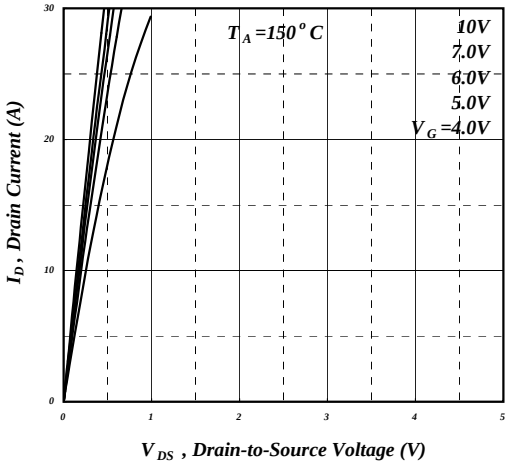


Fig 2. Typical Output Characteristics

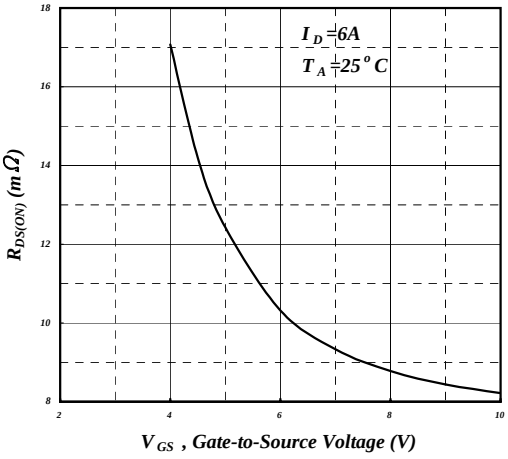


Fig 3. On-Resistance v.s. Gate Voltage

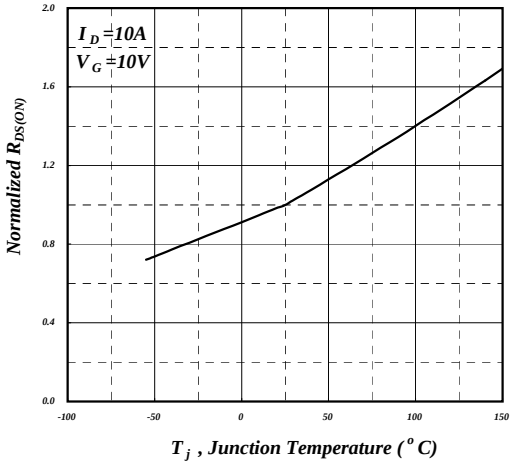


Fig 4. Normalized On-Resistance v.s. Junction Temperature

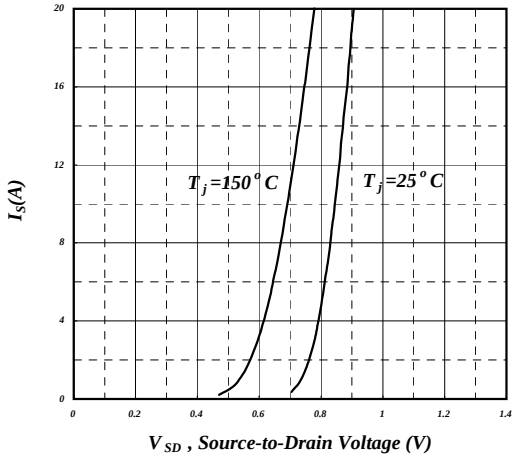


Fig 5. Forward Characteristic of Reverse Diode

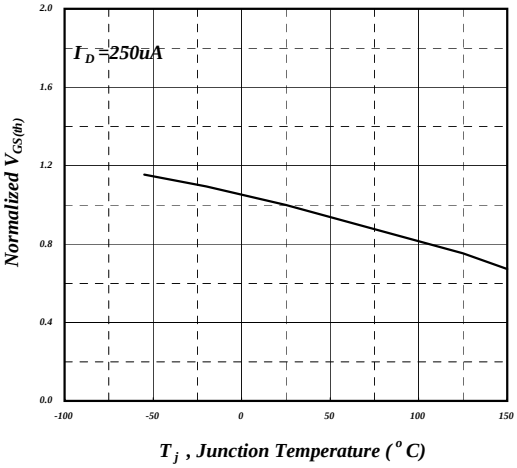


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-1

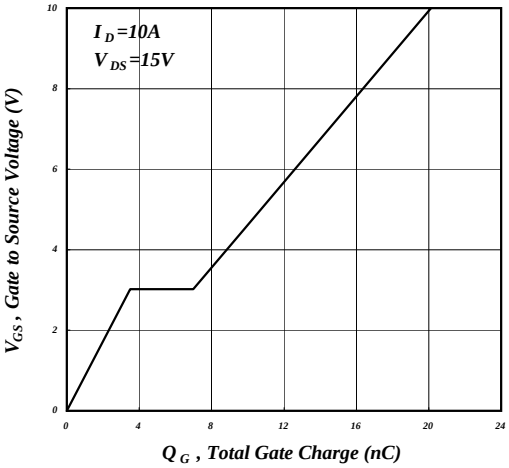


Fig 7. Gate Charge Characteristics

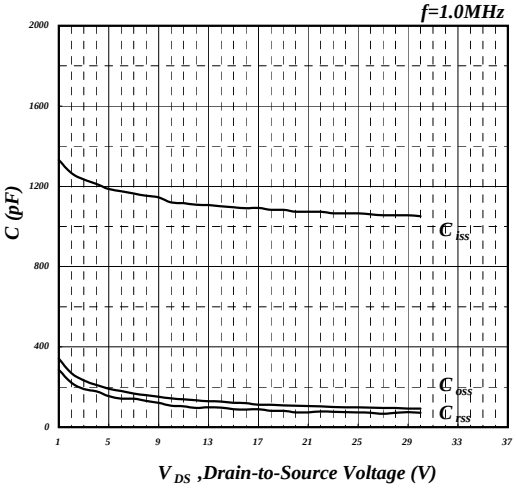


Fig 8. Typical Capacitance Characteristics

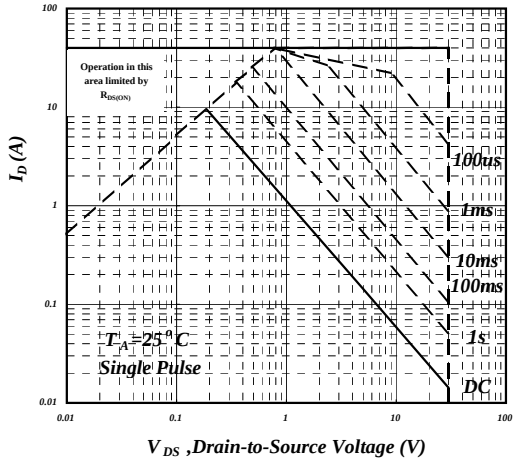


Fig 9. Maximum Safe Operating Area

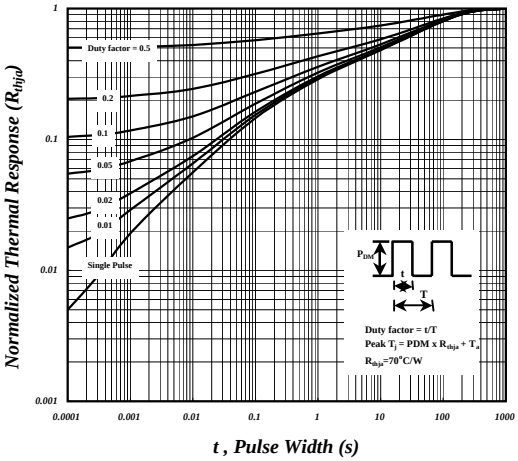


Fig 10. Effective Transient Thermal Impedance

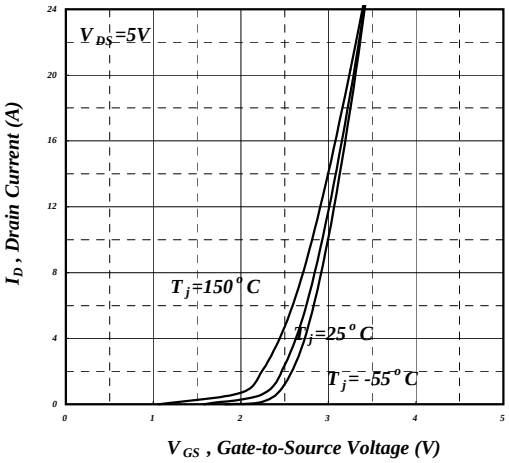


Fig 11. Transfer Characteristics

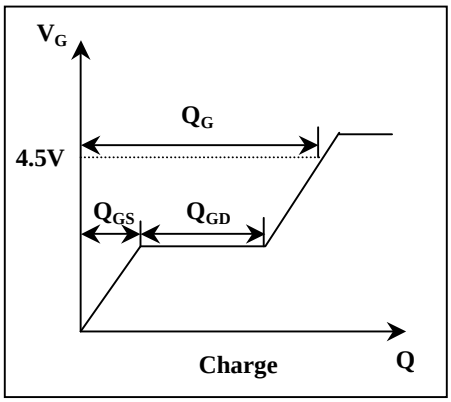


Fig 12. Gate Charge Waveform

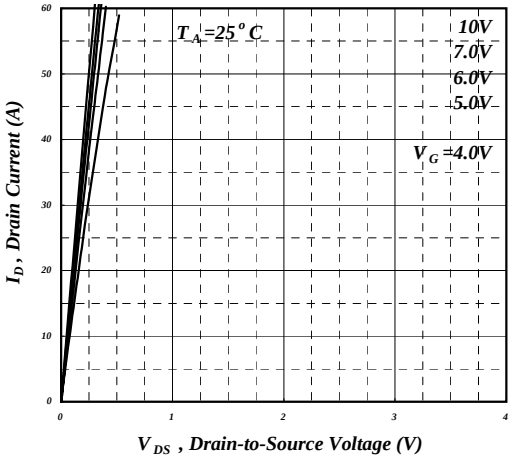


Fig 1. Typical Output Characteristics

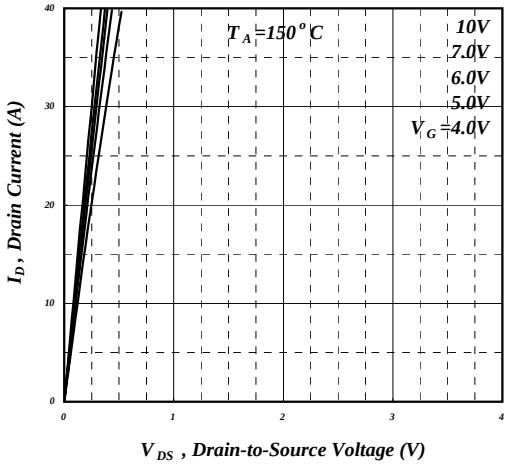


Fig 2. Typical Output Characteristics

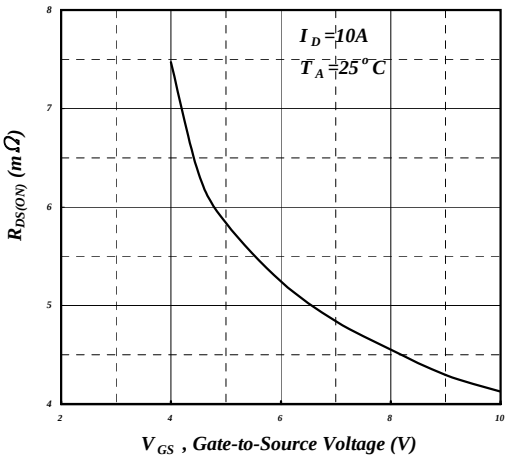


Fig 3. On-Resistance v.s. Gate Voltage

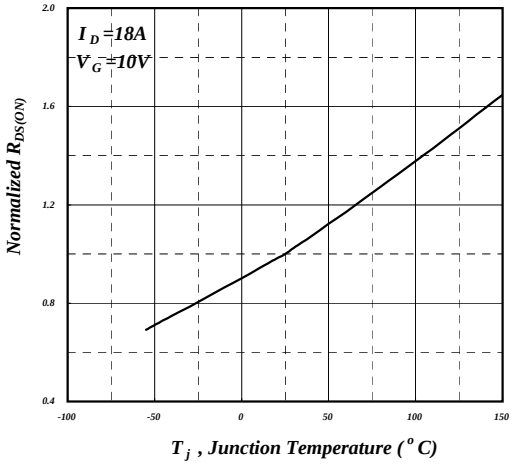
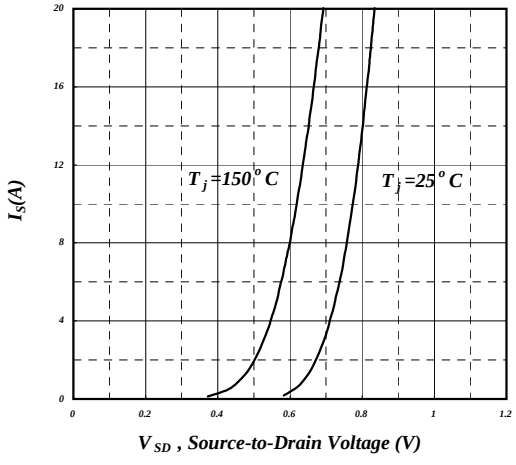


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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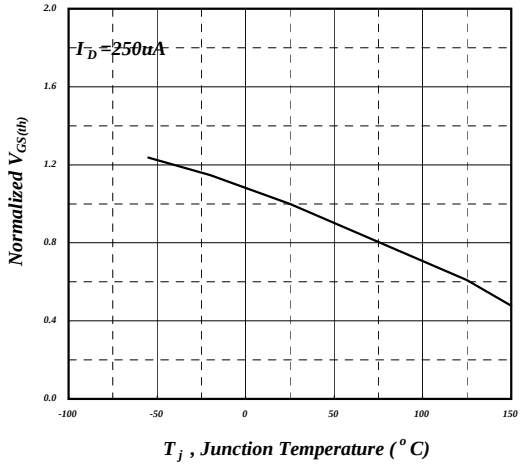


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Channel-2

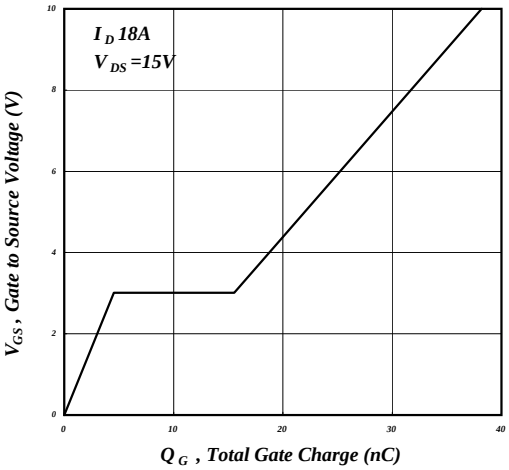
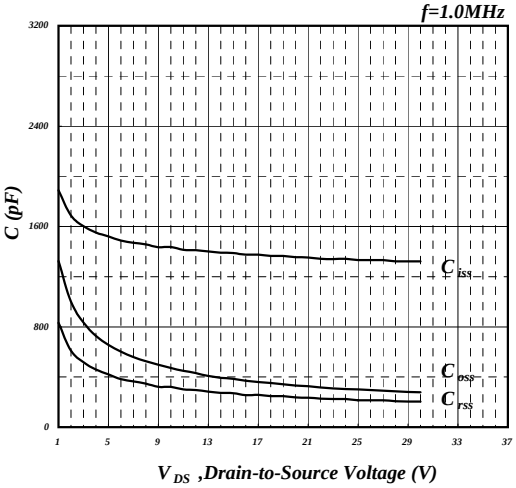


Fig 7. Gate Charge Characteristics



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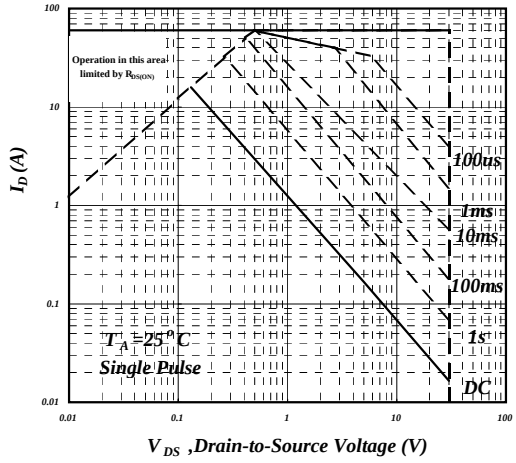

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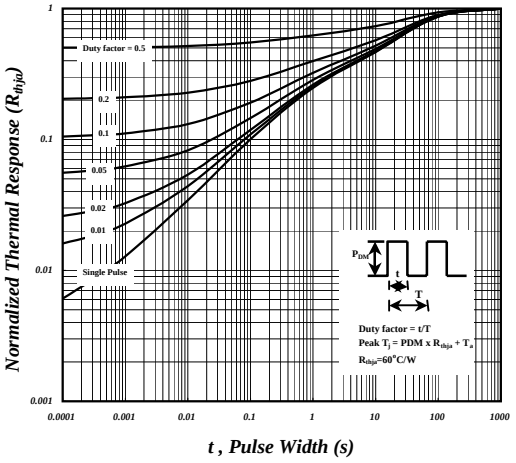


Fig 10. Effective Transient Thermal Impedance

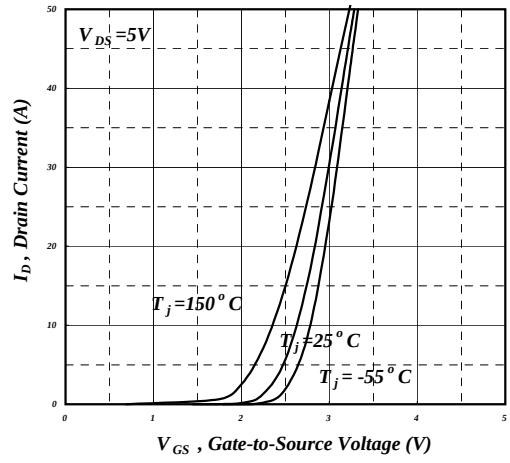


Fig 11. Transfer Characteristics

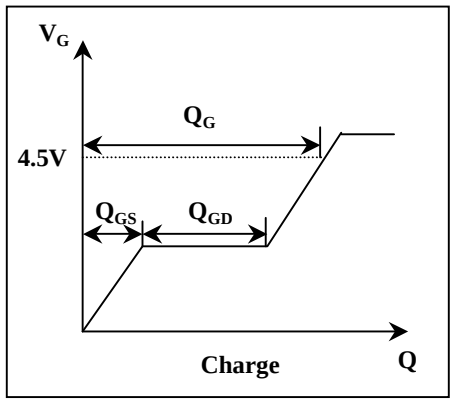
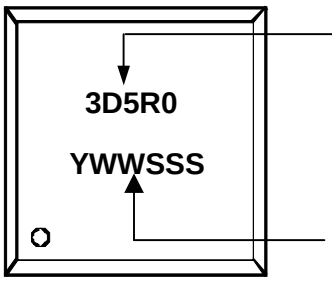


Fig 12. Gate Charge Waveform

MARKING INFORMATION



Part Number

Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence