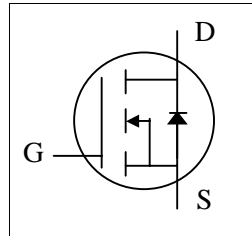




- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

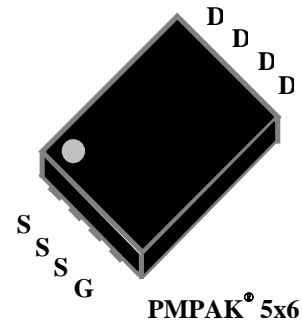


BV_{DSS}	30V
$R_{DS(ON)}$	1.05m Ω
I_D^{4}	245A

Description

AP3N1R0 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



PMPAK[®] 5x6

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current (Chip), V _{GS} @ 10V ⁴	245	A
I _D @T _A =25°C	Drain Current, V _{GS} @ 10V ³	54.2	A
I _D @T _A =70°C	Drain Current, V _{GS} @ 10V ³	43.3	A
I _{DM}	Pulsed Drain Current ¹	650	A
P _D @T _C =25°C	Total Power Dissipation	104	W
P _D @T _A =25°C	Total Power Dissipation ³	5	W
E _{AS}	Single Pulse Avalanche Energy ⁵	450	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.2	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W



AP3N1R0MT

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =10mA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	-	-	1.05	mΩ
		V _{GS} =4.5V, I _D =20A	-	-	1.4	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	0.9	-	2.2	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	-	135	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V	-	-	10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =20A	-	75	120	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	15	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	35	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	18	-	ns
t _r	Rise Time	I _D =1A	-	18	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	108	-	ns
t _f	Fall Time	V _{GS} =10V	-	73	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	7700	12320	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	1330	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	710	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.3	2.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Source Current (Body Diode)		-	-	60	A
V _{SD}	Forward On Voltage ²	I _S =20A, V _{GS} =0V	-	-	1.2	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _{GS} =0V,	-	45	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	40	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec ; 60°C/W at steady state.
- 4.Package limitation current is 100A .
- 5.Starting T_j=25°C , V_{DD}=25V , L=1mH , R_G=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

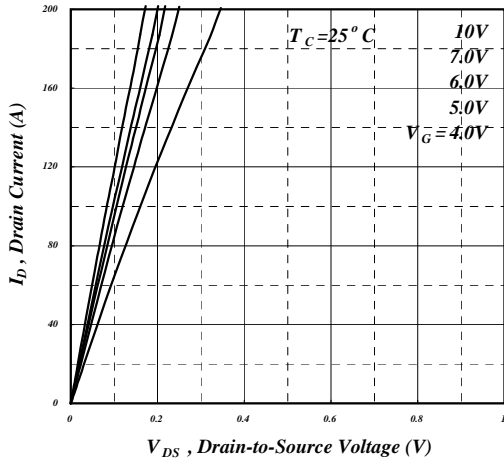


Fig 1. Typical Output Characteristics

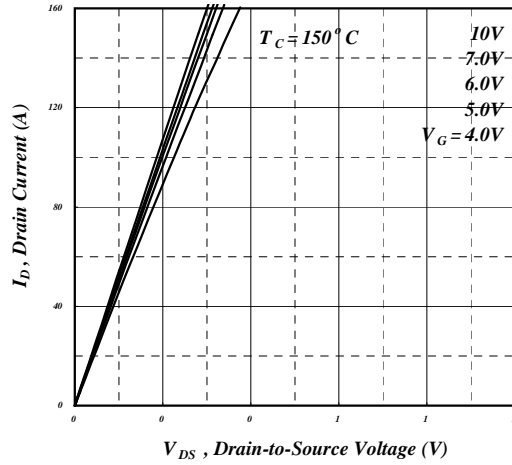


Fig 2. Typical Output Characteristics

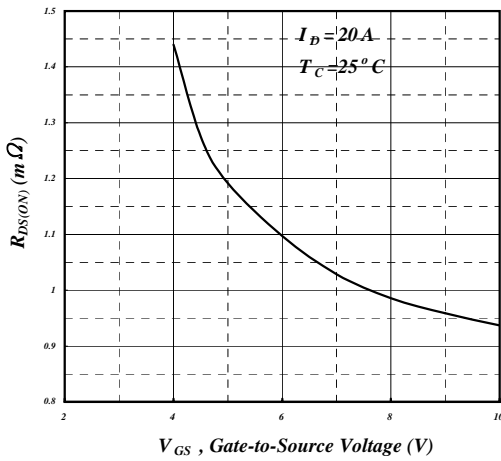


Fig 3. On-Resistance v.s. Gate Voltage

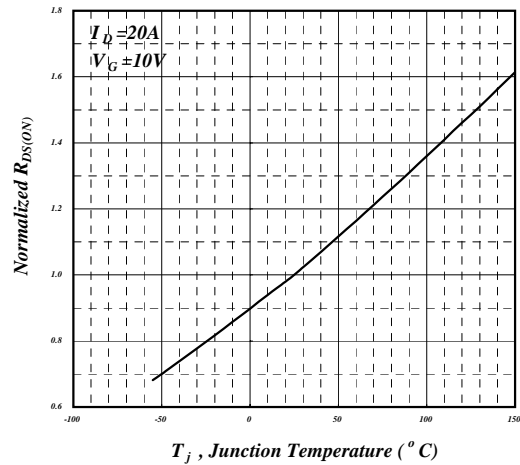


Fig 4. Normalized On-Resistance v.s. Junction Temperature

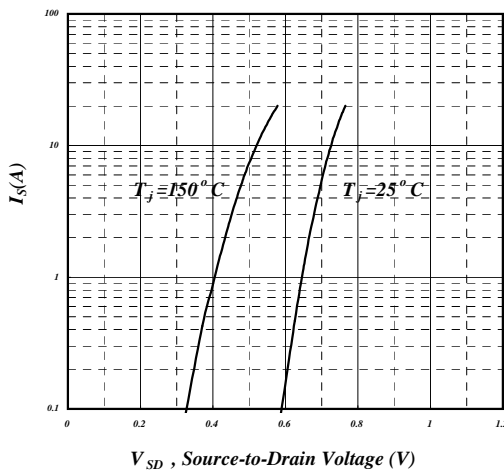


Fig 5. Forward Characteristic of Reverse Diode

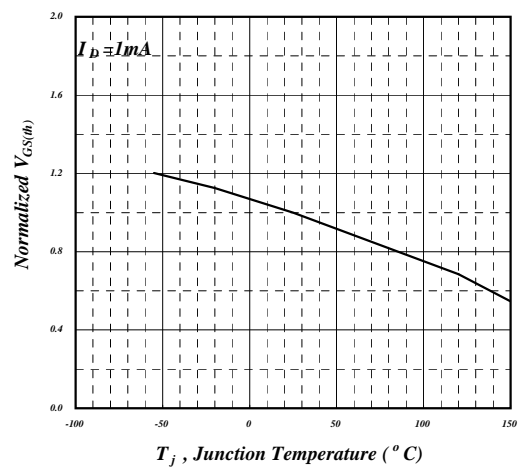


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

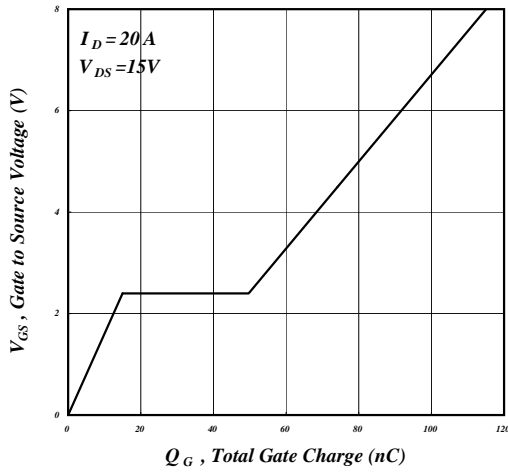


Fig 7. Gate Charge Characteristics

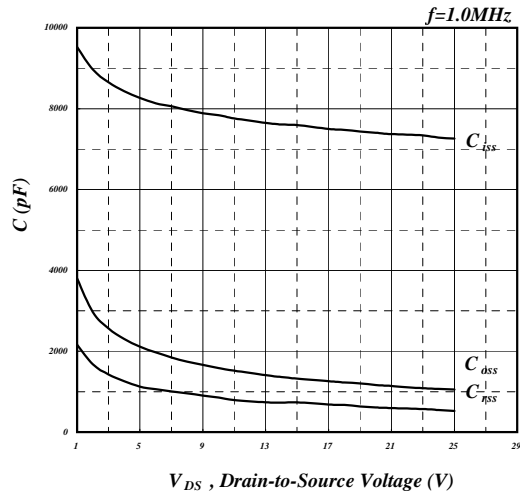


Fig 8. Typical Capacitance Characteristics

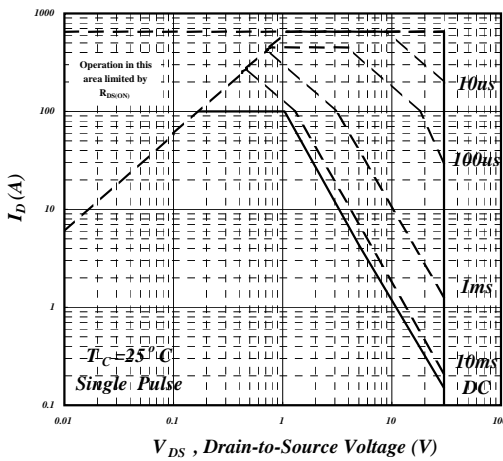


Fig 9. Maximum Safe Operating Area

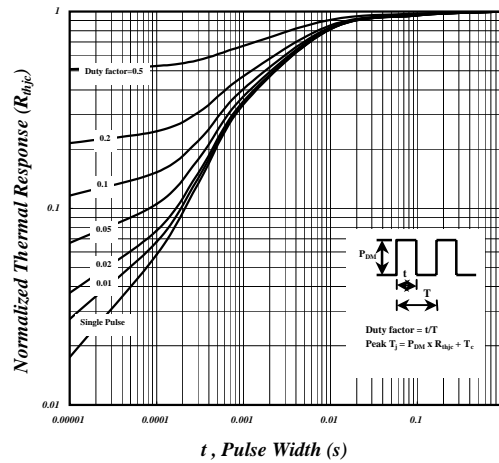


Fig 10. Effective Transient Thermal Impedance

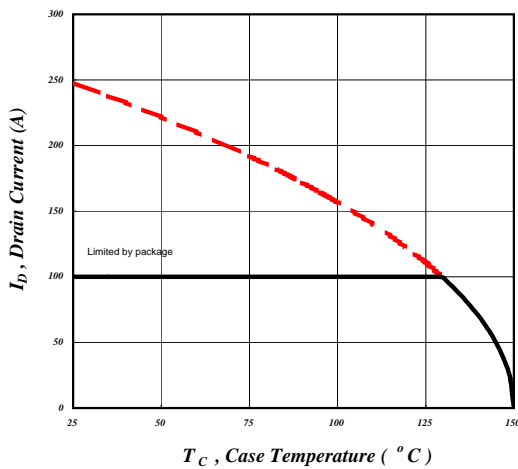


Fig 11. Drain Current v.s. Case Temperature

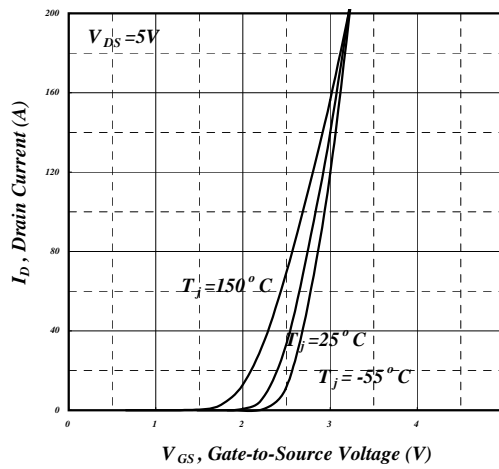


Fig 12. Transfer Characteristics

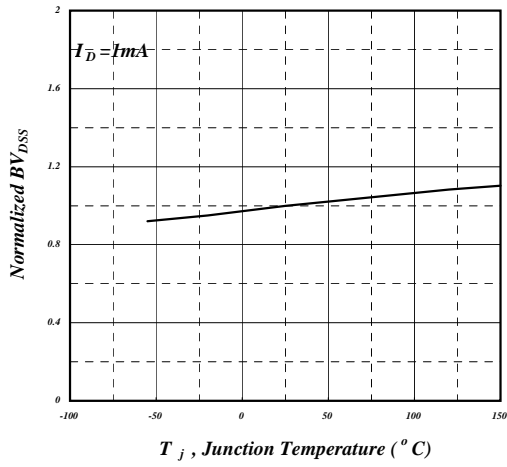


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

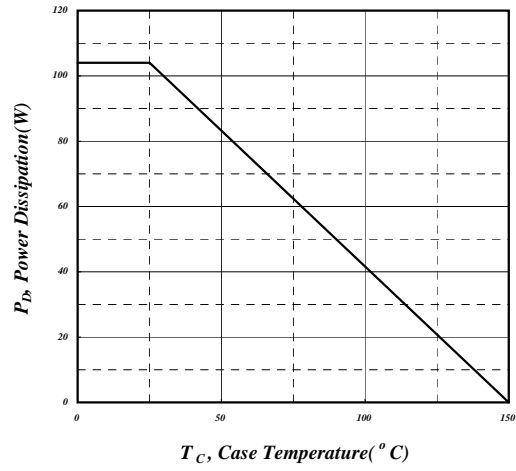


Fig 14. Total Power Dissipation

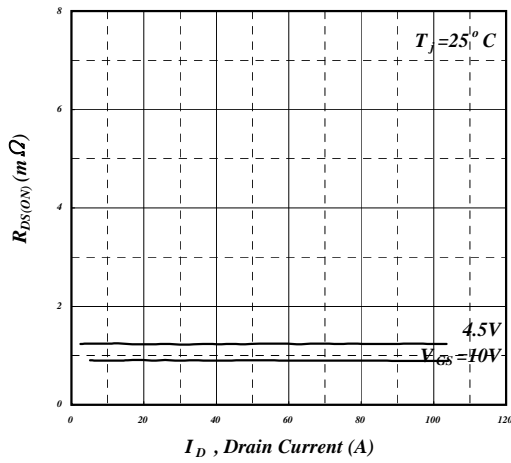
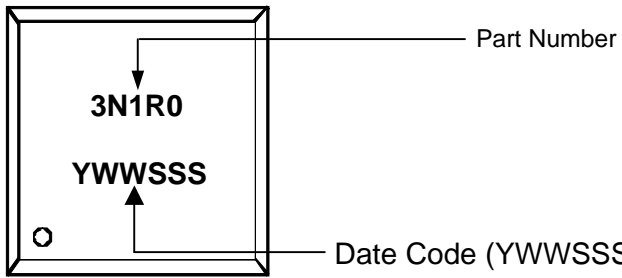


Fig 15. Typ. Drain-Source on State Resistance



MARKING INFORMATION



Y : Last Digit Of The Year
WW : Week
SSS : Sequence