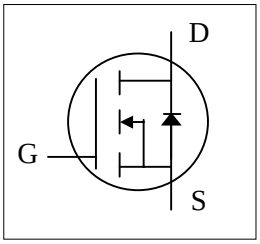
# AP3N5R0MT

**Halogen-Free Product**

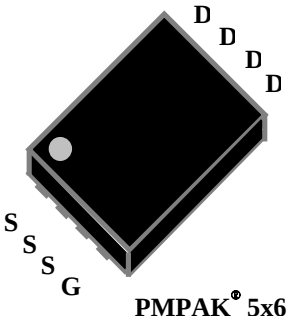
**Advanced Power Electronics Corp.**

*N-CHANNEL ENHANCEMENT MODE POWER MOSFET*

- ▼ **100% $R_g$ & UIS Test**
- ▼ **Simple Drive Requirement**
- ▼ **Low On-resistance**
- ▼ **RoHS Compliant & Halogen-Free**




| | |
|---|---|
| $BV_{DSS}$ | 30V |
| $R_{DS(ON)}$ | 5mΩ |




PMPAK® 5x6

## Description

AP3N5R0 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK ® 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

## Absolute Maximum Ratings@$T_j$=25°C(unless otherwise specified)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | 30 | V |
| $V_{GS}$ | Gate-Source Voltage | ±20 | V |
| $I_D$@$T_C$=25℃ | Drain Current, $V_{GS}$ @ 10V | 61 | A |
| $I_D$@$T_A$=25℃ | Drain Current, $V_{GS}$ @ 10V[3] | 24.7 | A |
| $I_D$@$T_A$=70℃ | Drain Current, $V_{GS}$ @ 10V[3] | 19.7 | A |
| $I_{DM}$ | Pulsed Drain Current[1] | 200 | A |
| $P_D$@$T_C$=25℃ | Total Power Dissipation | 31.2 | W |
| $P_D$@$T_A$=25℃ | Total Power Dissipation[3] | 5 | W |
| $E_{AS}$ | Single Pulse Avalanche Energy[4] | 61.2 | mJ |
| $T_{STG}$ | Storage Temperature Range | -55 to 150 | ℃ |
| $T_J$ | Operating Junction Temperature Range | -55 to 150 | ℃ |

## Thermal Data

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Rthj-c | Maximum Thermal Resistance, Junction-case | 4 | ℃/W |
| Rthj-a | Maximum Thermal Resistance, Junction-ambient[3] | 25 | ℃/W |

## Electrical Characteristics@$T_j$=25°C(unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=1mA | 30 | - | - | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance[2] | $V_{GS}$=10V, $I_D$=19A | - | - | 5 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$=16A | - | - | 8 | mΩ |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250uA | 1.3 | - | 2.3 | V |
| $g_{fs}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=19A | - | 69 | - | S |
| $I_{DSS}$ | Drain-Source Leakage Current | $V_{DS}$=24V, $V_{GS}$=0V | - | - | 10 | uA |
| $I_{GSS}$ | Gate-Source Leakage | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| $Q_g$ | Total Gate Charge | $I_D$=16A | - | 22 | 35.2 | nC |
| $Q_{gs}$ | Gate-Source Charge | $V_{DS}$=15V | - | 7 | - | nC |
| $Q_{gd}$ | Gate-Drain ("Miller") Charge | $V_{GS}$=4.5V | - | 10.5 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DS}$=15V | - | 11 | - | ns |
| $t_r$ | Rise Time | $I_D$=19A | - | 59 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G$=3.3Ω | - | 29 | - | ns |
| $t_f$ | Fall Time | $V_{GS}$=10V | - | 13 | - | ns |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V | - | 1900 | 3040 | pF |
| $C_{oss}$ | Output Capacitance | $V_{DS}$=15V | - | 305 | - | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | f=1.0MHz | - | 245 | - | pF |
| $R_g$ | Gate Resistance | f=1.0MHz | - | 1.5 | 3 | Ω |

## Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Forward On Voltage[2] | $I_S$=19A, $V_{GS}$=0V | - | - | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_S$=20A, $V_{GS}$=0V, | - | 15 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | dI/dt=100A/μs | - | 6 | - | nC |

### Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 $in^2$ copper pad of FR4 board, t ≤10sec ; 60°C/W at steady state.

4.Starting $T_j$=25°C , $V_{DD}$=30V , L=0.1mH , $R_G$=25Ω, $V_{GS}$=10V

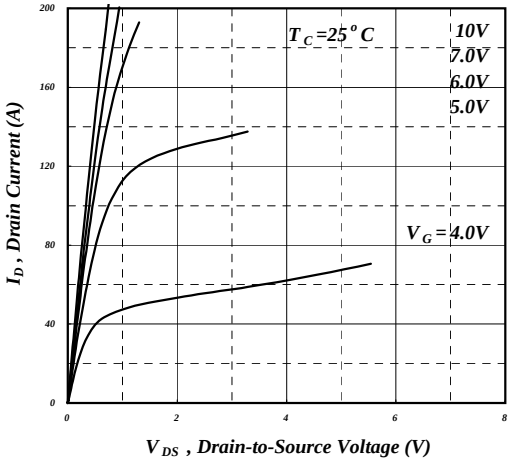



**Fig 1. Typical Output Characteristics**

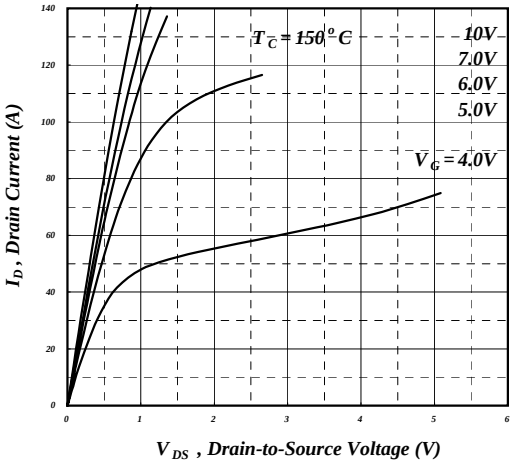



**Fig 2. Typical Output Characteristics**

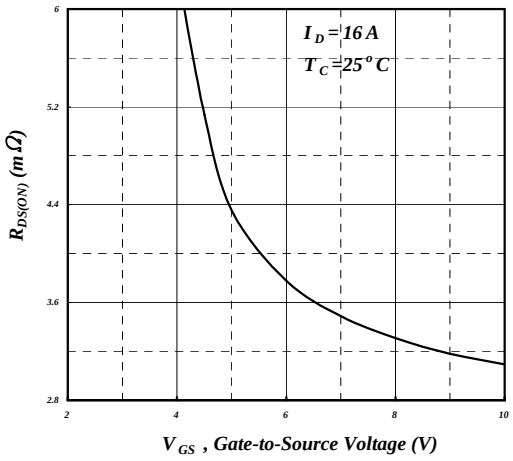



**Fig 3. On-Resistance v.s. Gate Voltage**

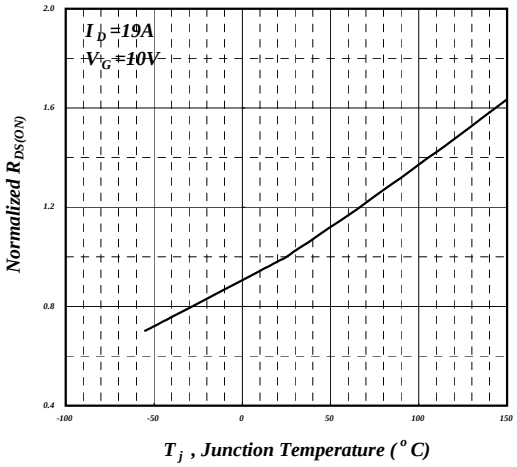



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

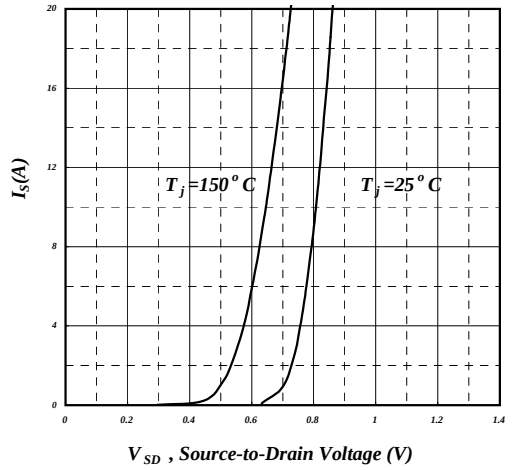



**Fig 5. Forward Characteristic of Reverse Diode**

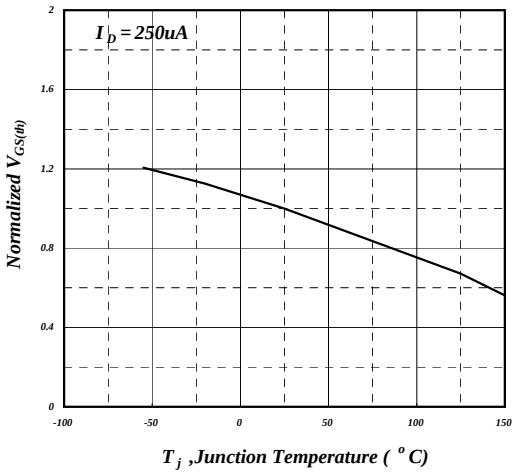



**Fig 6. Transfer Characteristics**

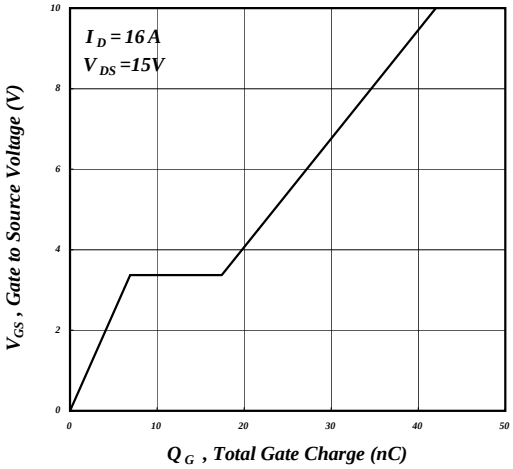



Fig 7. Gate Charge Characteristics

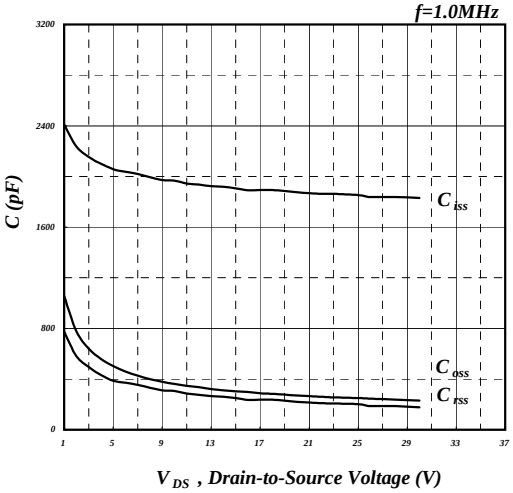



Fig 8. Typical Capacitance Characteristics

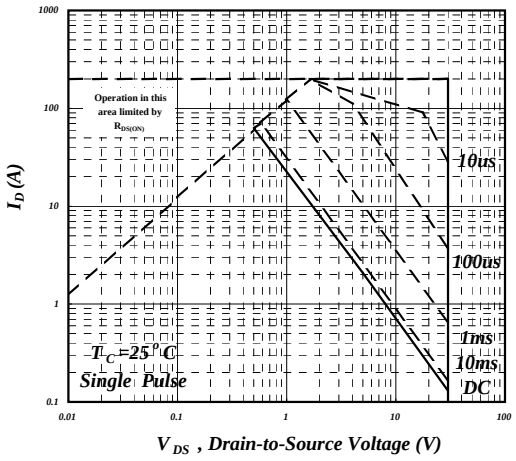



Fig 9. Maximum Safe Operating Area

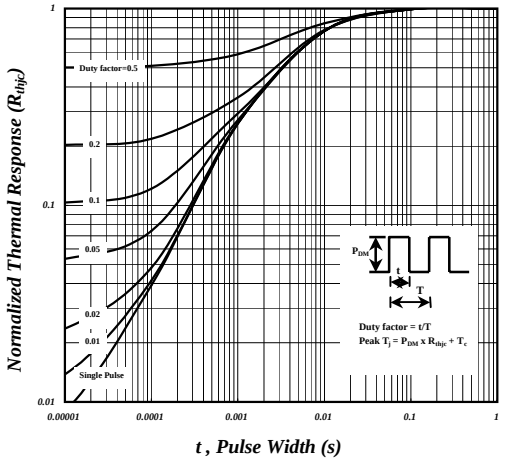



Fig 10. Effective Transient Thermal Impedance

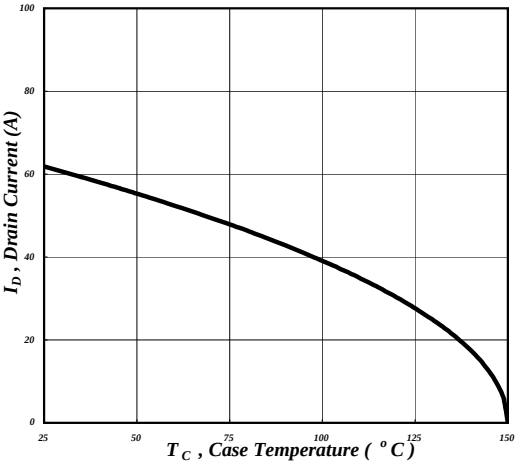



Fig 11. Drain Current v.s. Case Temperature

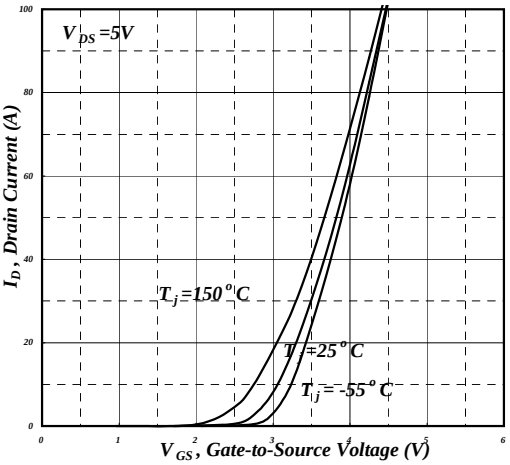



Fig 6. Gate Threshold Voltage v.s. Junction Temperature

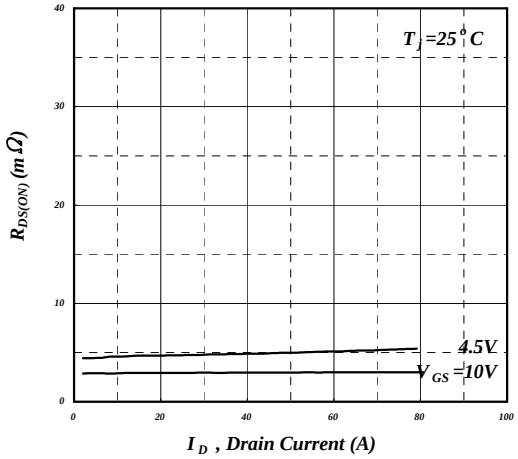



Fig 13. Typ. Drain-Source on State Resistance

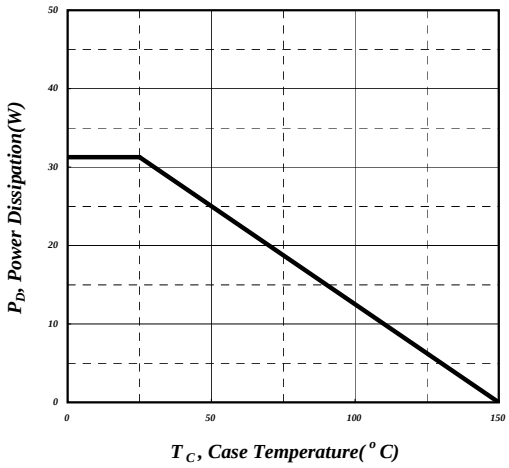
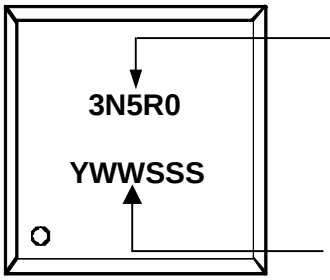



Fig 14. Total Power Dissipation

## MARKING INFORMATION




Part Number

Date Code (YWWSSS)

Y：Last Digit Of The Year

WW：Week

SSS：Sequence