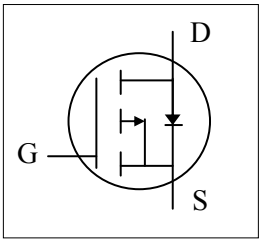
AP3P050AG

Halogen-Free Product

Advanced Power Electronics Corp.

P-CHANNEL ENHANCEMENT MODE POWER MOSFET

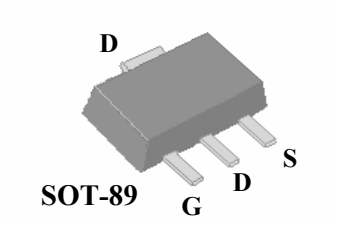
- ▼ **Low Gate Charge**
- ▼ **Fast Switching Characteristic**
- ▼ **Simple Drive Requirement**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	-30V
$R_{DS(ON)}$	50mΩ
I_D	- 4.1A

Description

AP3P050A series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	- 4.1	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	-3.2	A
I_{DM}	Pulsed Drain Current[1]	-20	A
P_D@T_A=25℃	Total Power Dissipation	1.25	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	100	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-4A	-	-	50	mΩ
		V_{GS}=-4.5V, I_D=-2A	-	-	75	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance[2]	V_{DS}=-10V, I_D=-4A	-	8	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g	Total Gate Charge	I_D=-2A	-	6.5	10.4	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-15V	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	2.5	-	nC
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=-15V	-	8	-	ns
t_r	Rise Time	I_D=-1A	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω	-	25	-	ns
t_f	Fall Time	V_{GS}=-10V	-	10	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	600	960	pF
C_{oss}	Output Capacitance	V_{DS}=-15V	-	100	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	70	-	pF
R_g	Gate Resistance	f=1.0MHz	-	13	26	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-1A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time	I_S=-2A, V_{GS}=0V	-	14	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=-100A/μs	-	5	-	nC

Notes:

1.Pulse width limited by Max junction temperature.

2.Pulse test

3.Surface mount on FR4 board, t ≤ 10s.

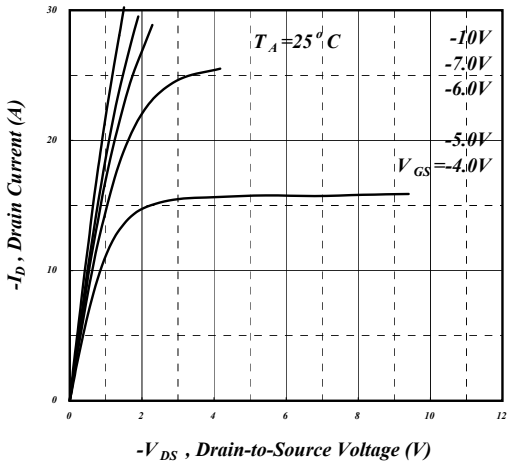


Fig 1. Typical Output Characteristics

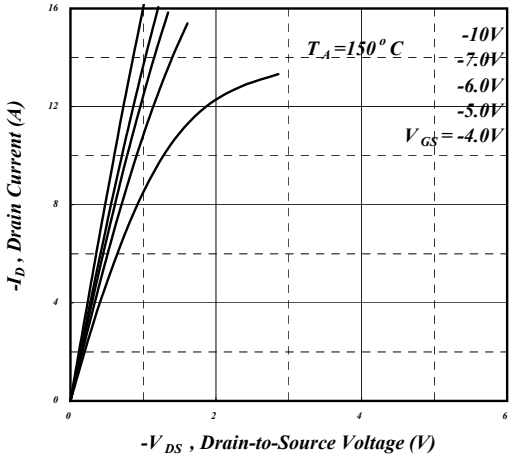


Fig 2. Typical Output Characteristics

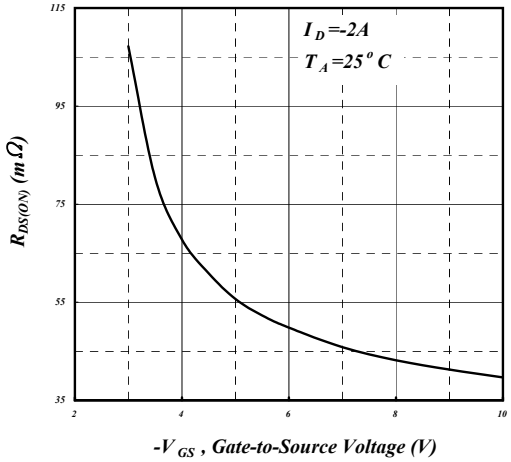


Fig 3. On-Resistance v.s. Gate Voltage

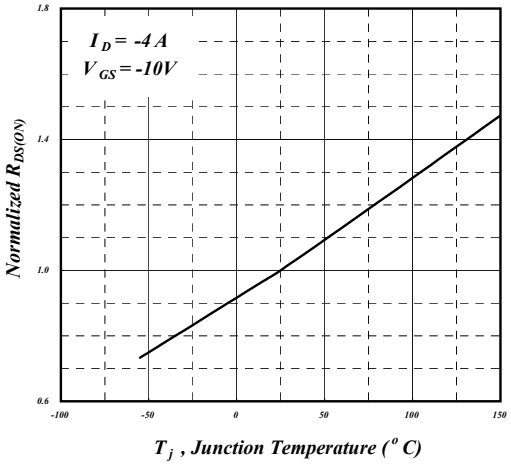


Fig 4. Normalized On-Resistance v.s. Junction Temperature

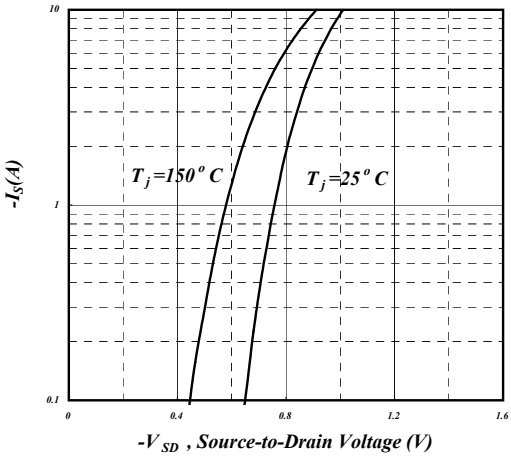


Fig5. Forward Characteristic of Reverse Diode

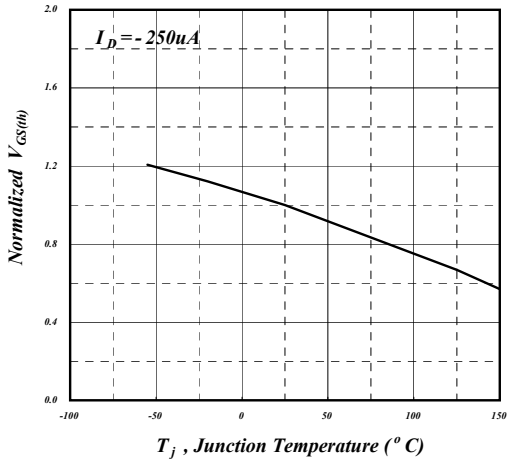


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

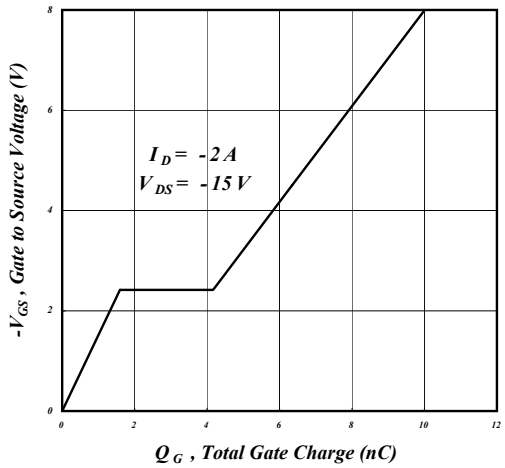


Fig 7. Gate Charge Characteristics

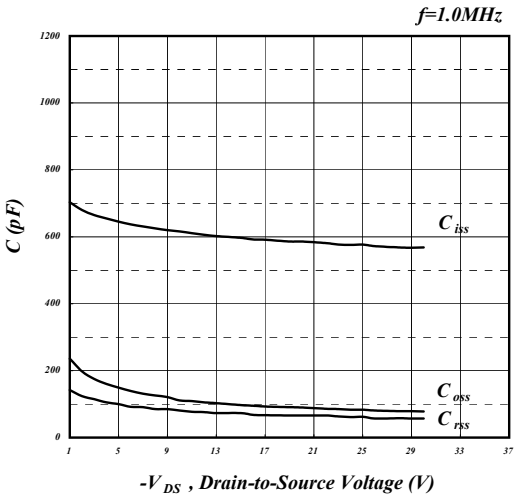


Fig 8. Typical Capacitance Characteristics

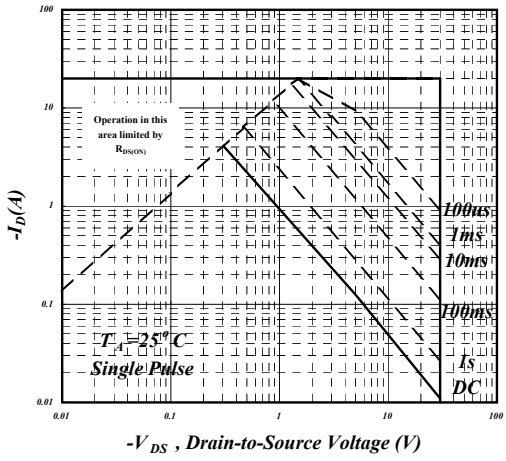


Fig 9. Maximum Safe Operating Area

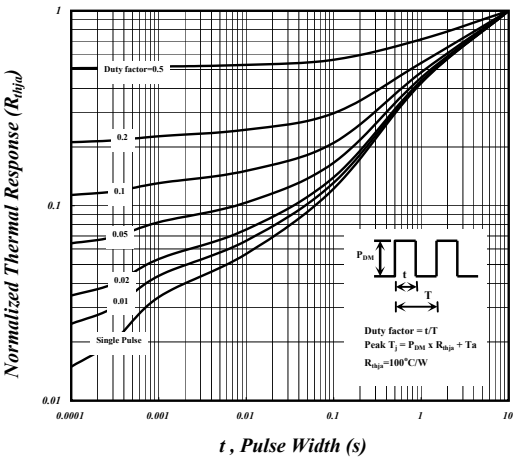


Fig 10. Effective Transient Thermal Impedance

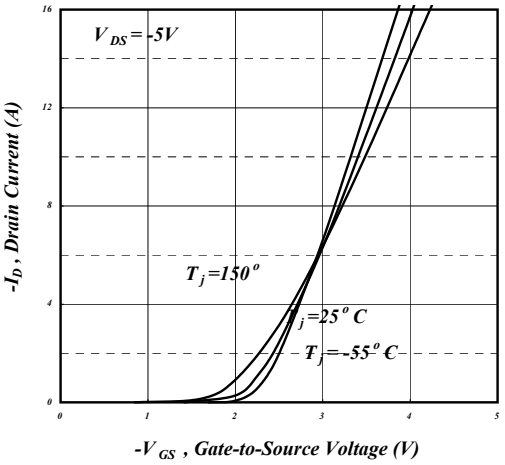


Fig 11. Transfer Characteristics

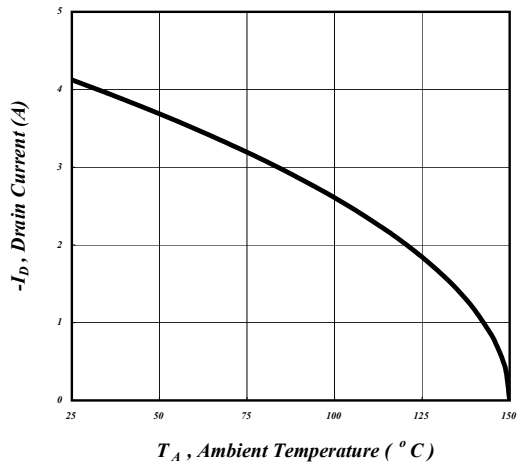


Fig 12. Drain Current v.s. Ambient Temperature

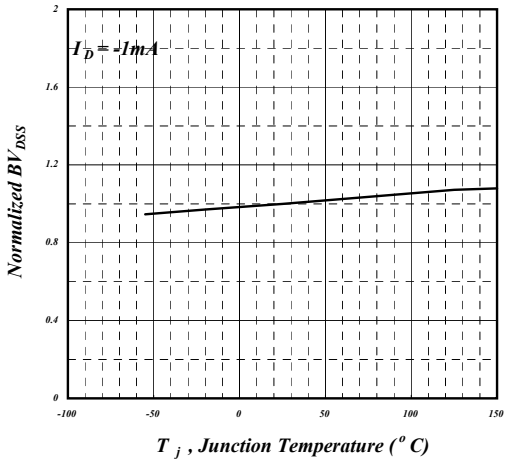


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

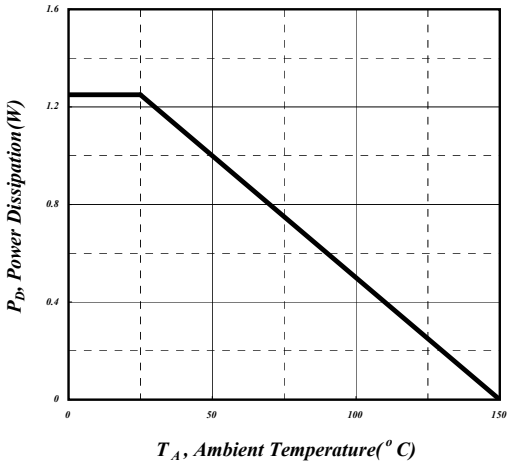


Fig 14. Total Power Dissipation

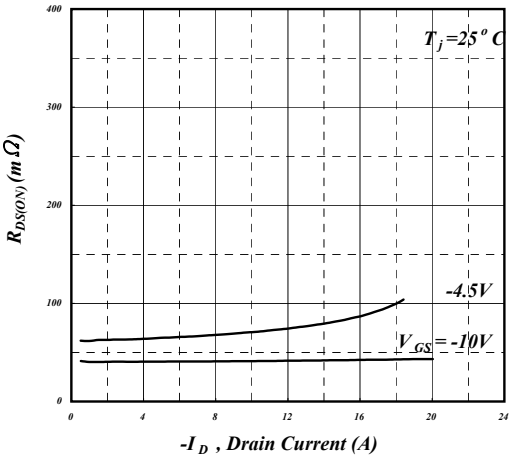
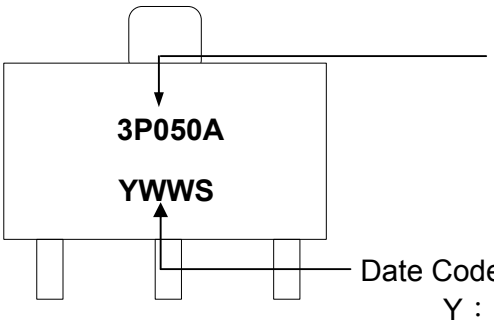


Fig 15. Typ. Drain-Source on State Resistance

MARKING INFORMATION



Y：Last Digit Of The Year
WW：Week
S：Sequence