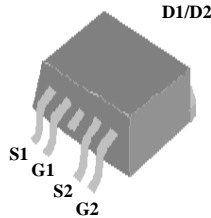




- ▼ Simple Drive Requirement
- ▼ Good Thermal Performance
- ▼ Fast Switching Performance
- ▼ RoHS Compliant & Halogen-Free

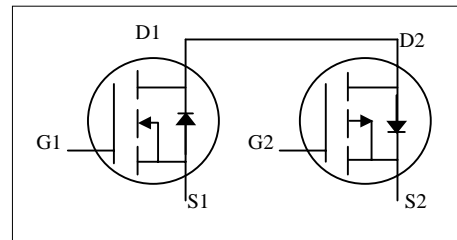


TO-252-4L

N-CH	BV_{DSS}	40V
	$R_{DS(ON)}$	20m Ω
	I_D	9.6A
P-CH	BV_{DSS}	-40V
	$R_{DS(ON)}$	36m Ω
	I_D	-7.3A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



Absolute Maximum Ratings @ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	+20	+20	V
$I_D@T_A=25^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	9.6	-7.3	A
$I_D@T_A=70^\circ\text{C}$	Drain Current ³ , V_{GS} @ 10V	7.7	-5.8	A
I_{DM}	Pulsed Drain Current ¹	40	-40	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	3.13		W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	6	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	$^\circ\text{C}/\text{W}$



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N-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=7A$	-	-	20	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	-	30	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=7A$	-	17	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=40V, V_{GS}=0V$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=7A$	-	13.5	21.6	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=32V$	-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	8	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=20V$	-	7	-	ns
t_r	Rise Time	$I_D=7A$	-	18	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	22	-	ns
t_f	Fall Time	$V_{GS}=10V$	-	6	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	960	1540	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	105	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	90	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=2.6A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=7A, V_{GS}=0V$	-	21	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	16	-	nC

**P-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-7A$	-	-	36	m Ω
		$V_{GS}=-4.5V, I_D=-5A$	-	-	60	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-	-3	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-7A$	-	19	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-40V, V_{GS}=0V$	-	-	-10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=-7A$	-	17.5	28	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-32V$	-	3.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	10	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-20V$	-	8.5	-	ns
t_r	Rise Time	$I_D=-7A$	-	17.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega$	-	39	-	ns
t_f	Fall Time	$V_{GS}=-10V$	-	44	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	1360	2180	pF
C_{oss}	Output Capacitance	$V_{DS}=-25V$	-	155	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	140	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-2.6A, V_{GS}=0V$	-	-	-1.2	V
t_{rr}	Reverse Recovery Time ²	$I_S=-7A, V_{GS}=0V$	-	25	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	20	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test.
3. N-CH, P-CH are same, mounted on 2oz FR4 board $t \leq 10s$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



N-Channel

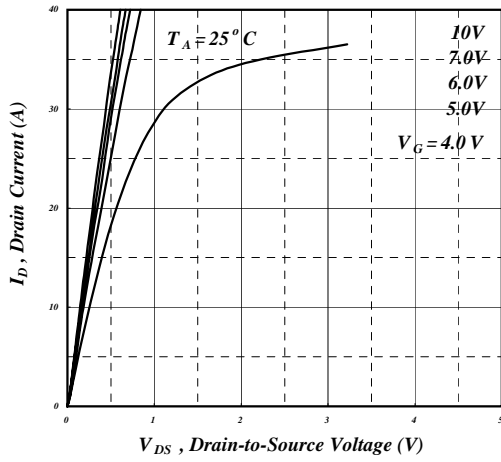


Fig 1. Typical Output Characteristics

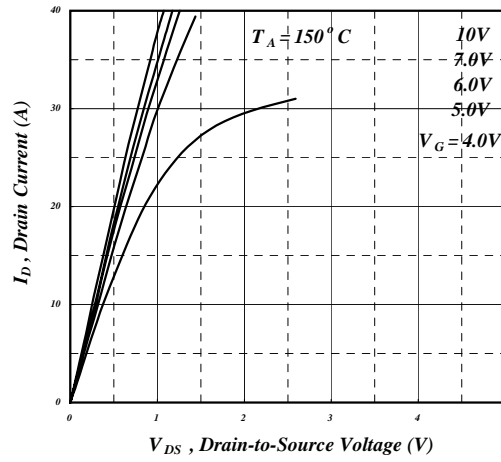


Fig 2. Typical Output Characteristics

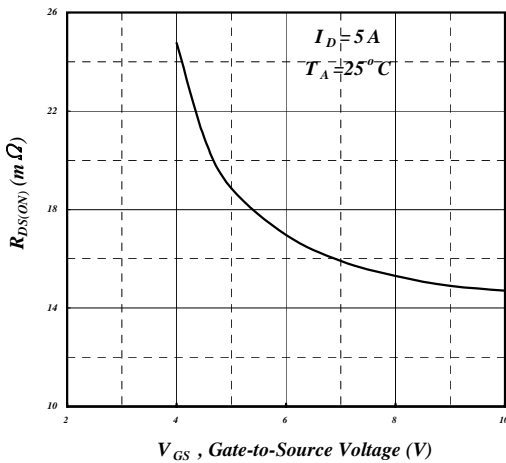


Fig 3. On-Resistance v.s. Gate Voltage

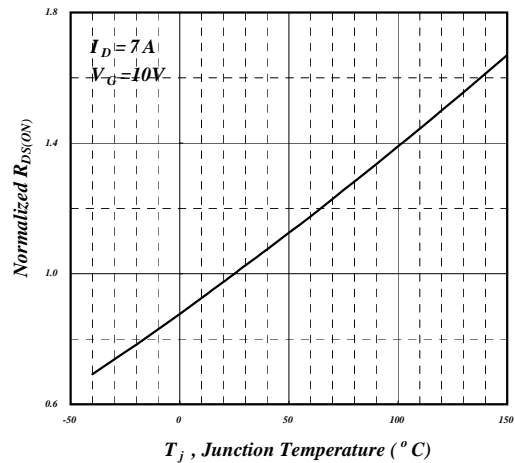


Fig 4. Normalized On-Resistance v.s. Junction Temperature

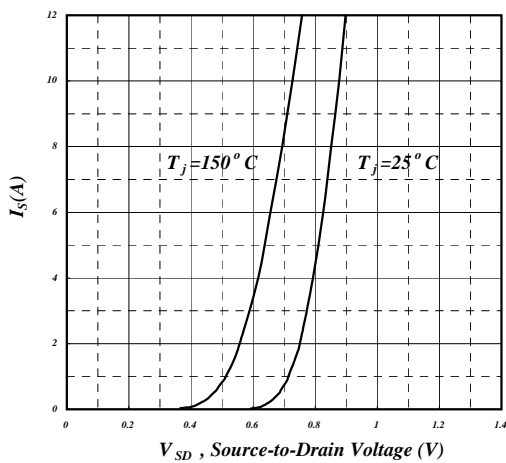


Fig 5. Forward Characteristic of Reverse Diode

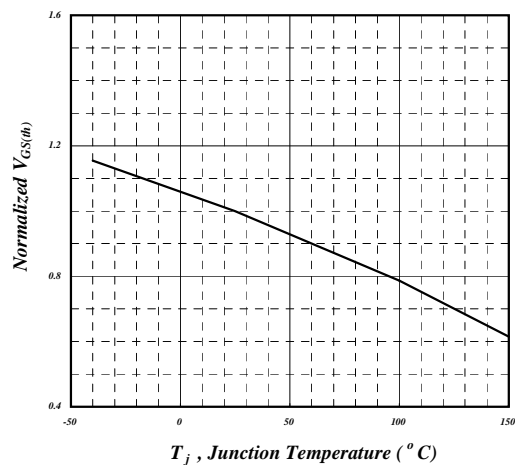


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

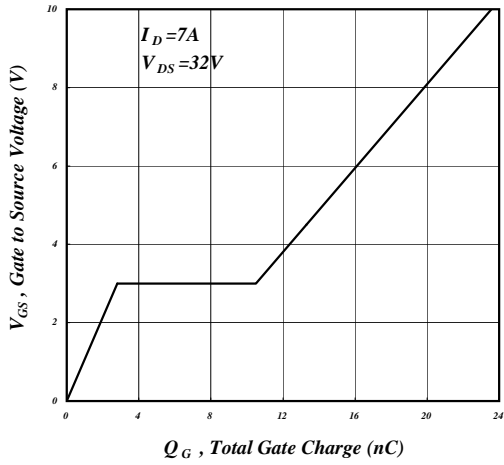


Fig 7. Gate Charge Characteristics

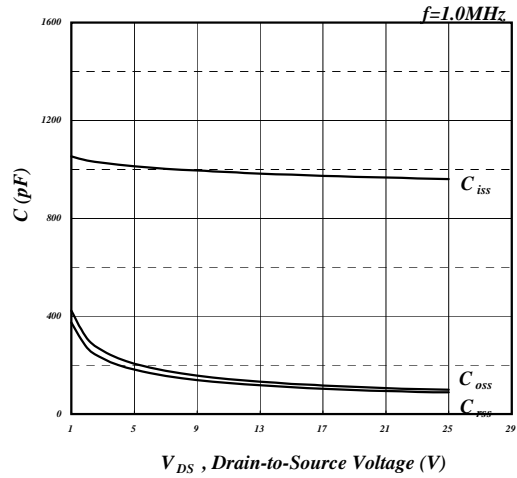


Fig 8. Typical Capacitance Characteristics

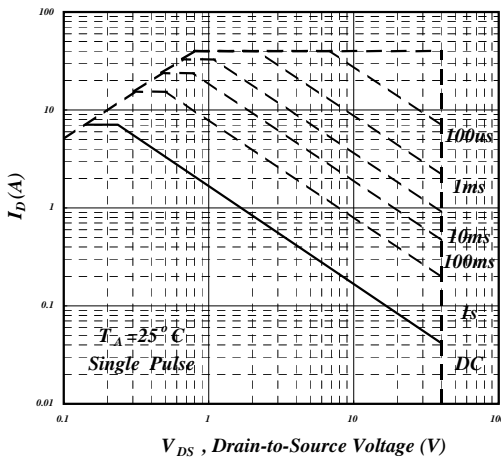


Fig 9. Maximum Safe Operating Area

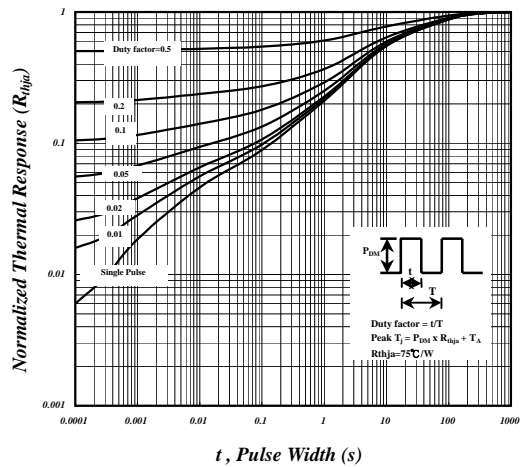


Fig 10. Effective Transient Thermal Impedance

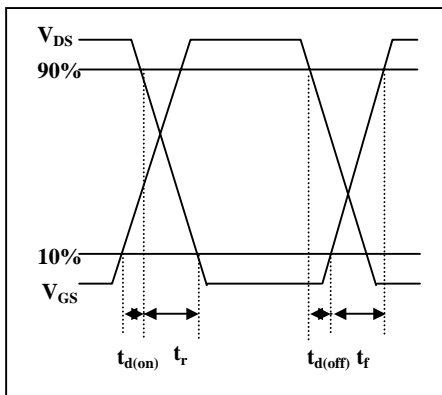


Fig 11. Switching Time Waveform

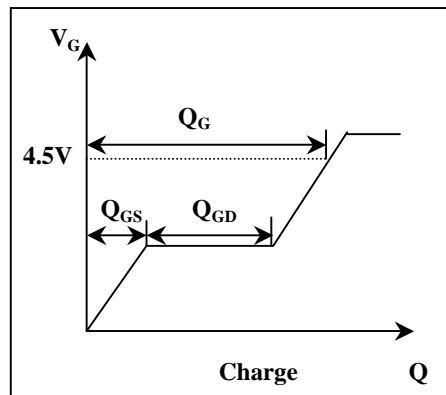


Fig 12. Gate Charge Waveform



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P-Channel

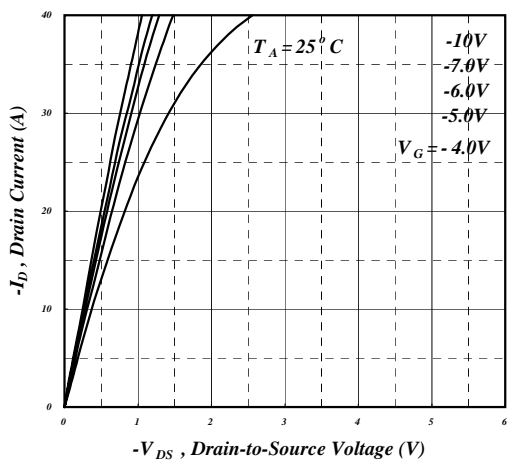


Fig 1. Typical Output Characteristics

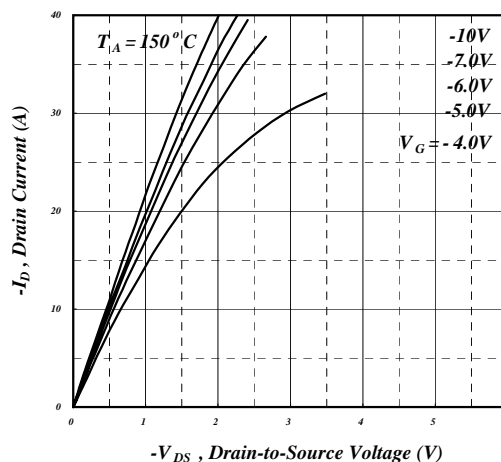


Fig 2. Typical Output Characteristics

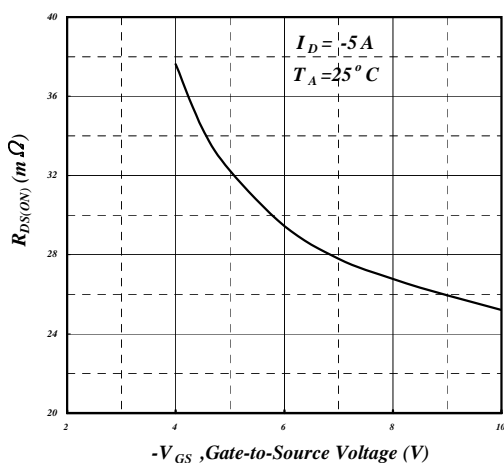


Fig 3. On-Resistance v.s. Gate Voltage

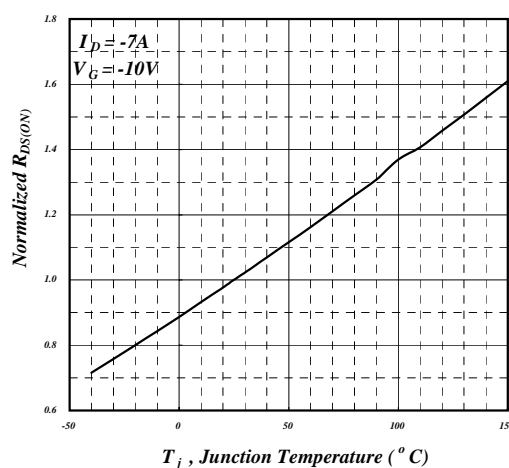


Fig 4. Normalized On-Resistance v.s. Junction Temperature

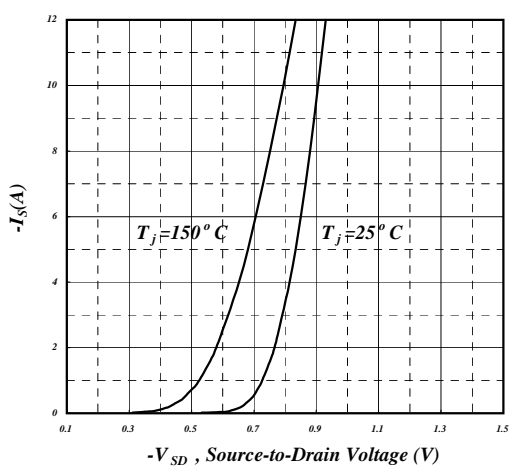


Fig 5. Forward Characteristic of Reverse Diode

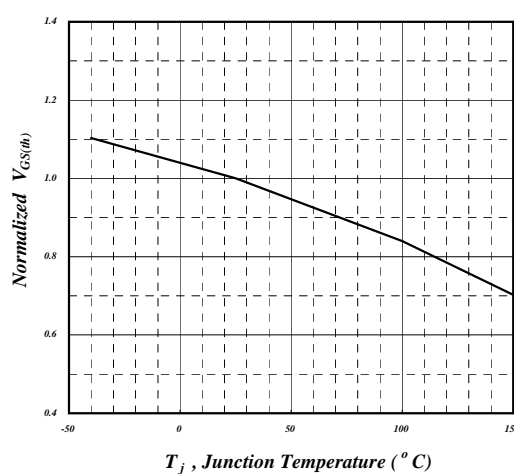


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

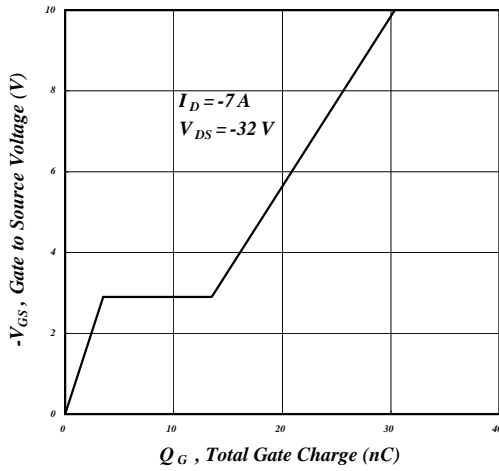


Fig 7. Gate Charge Characteristics

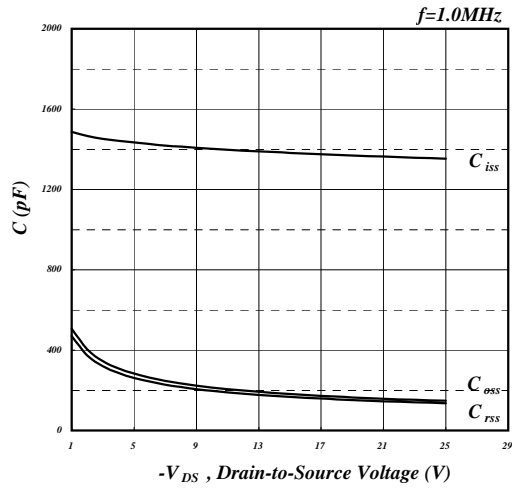


Fig 8. Typical Capacitance Characteristics

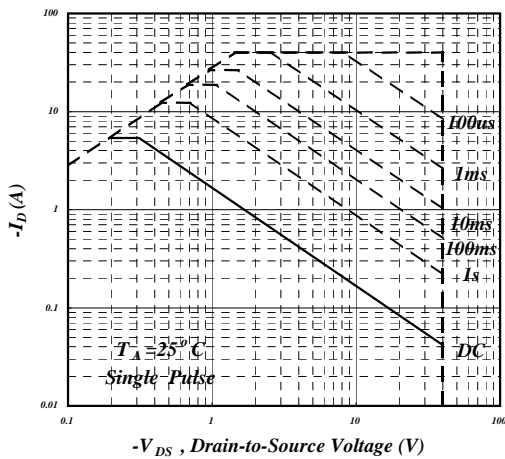


Fig 9. Maximum Safe Operating Area

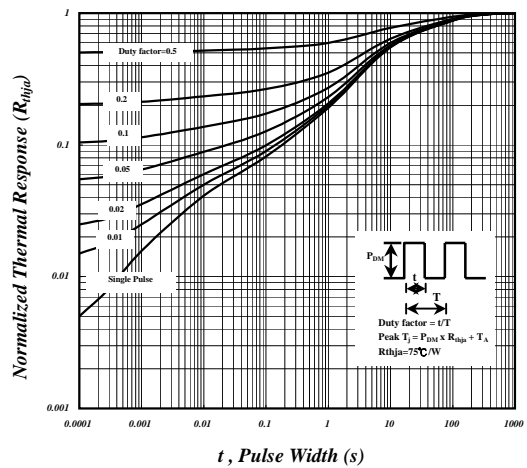


Fig 10. Effective Transient Thermal Impedance

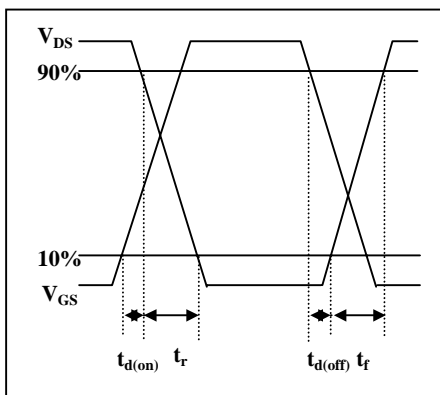


Fig 11. Switching Time Waveform

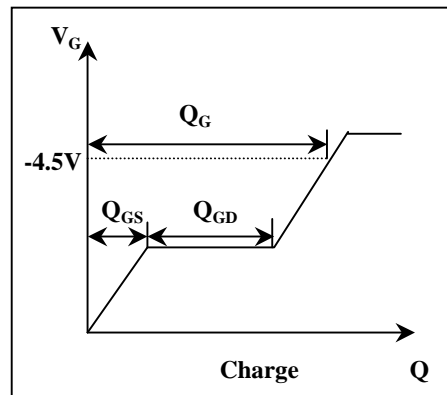


Fig 12. Gate Charge Waveform



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MARKING INFORMATION

