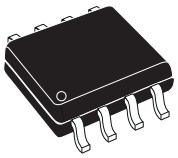
ST1480US

Datasheet

3.3 V powered, 15 kV ESD protected, up to 12 Mbps true RS-485/RS-422 transceiver



SO8

Product status link
ST1480US

Features

- ESD protection
  - – ±15 kV human body model
  - – ±8 kV IEC 1000-4-2 contact discharge
- Operates from a single 3.3 V supply - no charge pump required
- Interoperable with 5 V logic
- 1 µA low current shutdown mode max.
- Guaranteed 12 Mbps data rate
- -7 to 12 common mode input voltage range
- Half duplex versions available
- Industry standard 75176 pinout
- Current limiting and thermal shutdown for driver overload protection
- Guaranteed high receiver output state for floating, shorted or terminated inputs with no signal present
- Allows up to 64 transceivers on the bus

Description

The ST1480US is ±15 kV ESD protected, 3.3 V low power transceiver for RS-485 and RS-422 communications. The device contains one driver and one receiver in half duplex configuration. The ST1480US transmits and receives at a guaranteed data rate of at least 12 Mbps. All transmitter outputs and receiver inputs are protected to ±15 kV using human body model. Driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state.

The ST1480US input has a true fail-safe feature that guarantees a logic high output if both inputs are open circuit, shorted together or in the presence of a termination with no signal on the bus.

1 Pin configuration

Figure 1. Pin connections

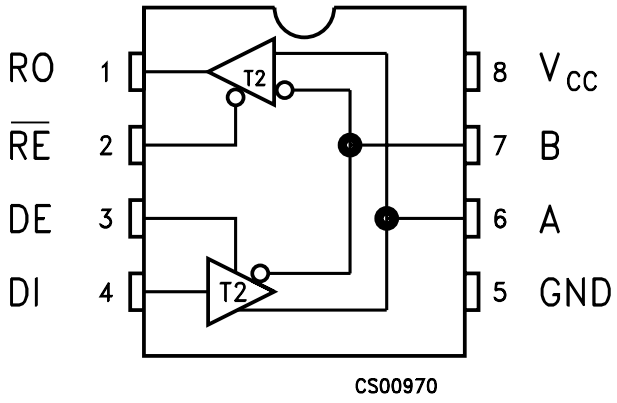


Table 1. Pin description

Pin	Symbol	Name and function
1	RO	Receiver output. If A>B by 200 mV, RO is high; if A< B by 200 mV, RO is low.
2	$\overline{RE}$	Receiver output enable. RO is enabled when RE is low; RO is high impedance when RE is high. If RE is high and DE is low, the device enters a low power shutdown mode.
3	DE	Driver output enable. The driver outputs are enabled by bringing DE high. They are high impedance when DE is low. If RE is high DE is low, the device enters a low-power shutdown mode. If the driver outputs are enabled, the part functions as line driver, while they are high impedance, it functions as line receivers if RE is low.
4	DI	Driver input. A low on DI forces output A low and output B high. Similarly, a high on DI forces output A high and output B low.
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output.
7	B	Inverting receiver input and inverting driver output.
8	VCC	Supply voltage: VCC=3 V to 3.6 V.

2 Truth tables

Table 2. Truth table (driver)

Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B	A	
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal
H	L	X	Z	Z	Shutdown

Note: X= do not care; Z= high impedance

Inputs			Output	Mode
$\overline{RE}$	DE	A-B	RO	
L	L	≥+0.2V	H	Normal
L	L	≤-0.2V	L	Normal
L	L	Inputs open	H	Normal
L	L	Inputs shorted	H	Normal
H	L	X	Z	Shutdown

Note: X= do not care; Z= high impedance

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		7	V
V_I	Control input voltage ($\overline{RE}$, DE)		-0.3 to 7	V
V_{DI}	Driver input voltage (DI)		-0.3 to 7	V
V_{DO}	Driver output voltage (A, B)		± 14	V
V_{RI}	Receiver input voltage (A, B)		± 14	V
V_{RO}	Receiver output voltage (RO)		-0.3 to (V_{CC}+ 0.3)	V
ESD	ESD protection voltage	Human body model	±15	kV
		IEC-1000-4-2 contact discharge	±8	

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

4 Electrical characteristics

V_{CC} = 3 V to 3.6 V, T_A = -40 to 85 °C, unless otherwise specified. Typical values are referred to T_A = 25 °C).

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{SUPPLY}	V_{CC} power supply current	No Load, DI = 0 V or V_{CC}	DE = V_{CC}, $\overline{RE}$ = 0 V or V_{CC}		1.3	2.2	mA
			DE=0 V, $\overline{RE}$=0 V		1.2	1.9	mA
I_{SHDN}	Shutdown supply current	DE = 0 V, RE = V_{CC}, DI = 0 V or V_{CC}			0.002	1	µA

Table 5. Logic input electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{IL}	Input logic threshold low	DE, DI, RE				0.8	V
V_{IH}	Input logic threshold high	DE, DI, RE		2			V
I_{IN1}	Logic input current	DE, DI, RE				±2.0	µA
I_{IN2}	Input current (A, B)	DE=0 V, V_{CC}=0 or 3.6 V	VIN = 12 V			1	mA
			VIN = -7 V			-0.8	mA

Table 6. Transmitter electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential drive output	R_L= 100 Ω (RS-422) (Figure 1. Pin connections)	2			V
		R_L= 54 Ω (RS-485) (Figure 1. Pin connections)	1.5			V
		R_L= 60 Ω (RS-485) (Figure 2. Driver and V_{OC} test load)	1.5			V
ΔV_{OD}	Change in magnitude of driver differential output voltage for complementary output states (1)	R_L= 54 Ω or 100 Ω (Figure 1. Pin connections)			0.2	V
V_{OC}	Driver common mode output voltage	R_L= 54 Ω or 100 Ω (Figure 1. Pin connections)			3	V
ΔV_{OC}	Change in magnitude of driver common mode output voltage(1)	R_L= 54 Ω or 100 Ω (Figure 1. Pin connections)			0.2	V
I_{OSD}	Driver short-circuit output current				±250	mA

1. *ΔVOD and ΔVOC are the changes in VOD and VOC, respectively, when the DI input changes state.*

Table 7. Receiver electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{TH}	Receiver differential threshold voltage	V_{CM}=-7 V to 12 V, DE = 0	-0.2		-0.015	V
ΔV_{TH}	Receiver input hysteresis	V_{CM}=0 V		30		µV
V_{OH}	Receiver output high voltage	I_{OUT} = -4 mA, V_{ID} = 200 mV, (Figure 8. Drive enable and disable times waveforms)	2			V
V_{OL}	Receiver output low voltage	I_{OUT}= 4 mA, V_{ID} = -200 mV, (Figure 3. Driver V_{OD} with varying common mode voltage test load)			0.4	V
I_{OZR}	3-state (high impedance) output current at receiver	V_{CC}= 3.6 V, V_O = 0 V to V_{CC}			±1	µA
R_{RIN}	Receiver input resistance	V_{CM} = -7 V to 12 V	24			kΩ
I_{OSR}	Receiver short-circuit current	V_{RO} = 0 V to V_{CC}	7		60	mA

Table 8. Driver switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
D_R	Maximum data rate		12	15		Mbps
t_{DD}	Differential output delay	R_L= 60 Ω, C_L= 15 pF, (Figure 4. Receiver V_{OH} and V_{OL} test circuit and Figure 5. Drive differential output delay transition time test circuit)		18	30	ns
t_{TD}	Differential output transition time	R_L= 60 Ω, C_L= 15 pF, (Figure 4. Receiver V_{OH} and V_{OL} test circuit and Figure 5. Drive differential output delay transition time test circuit)		12	20	ns
t_{PLH} t_{PHL}	Propagation delay	R_L= 27 Ω, C_L= 15 pF, (Figure 8. Drive enable and disable times waveforms and Figure 9. Drive propagation time test circuit)		18	30	ns
t_{PDS}	$\lvert t_{PLH} - t_{PHL} \rvert$propagation delay skew(1)	R_L= 27 Ω, C_L= 15 pF, (Figure 8. Drive enable and disable times waveforms and Figure 9. Drive propagation time test circuit)		2	5	ns
t_{PZL}	Output enable time	R_L= 110 Ω, (Figure 10. Drive propagation time waveform and Figure 11. Drive enable and disable times test circuit (R_L= 110 Ω))		19	35	ns
t_{PZH}	Output enable time	R_L= 110 Ω, (Figure 10. Drive propagation time waveform and Figure 11. Drive enable and disable times test circuit (R_L= 110 Ω))		30	50	ns
t_{PHZ}	Output disable time	R_L= 110 , (Figure 6. Drive differential output delay transition time waveform and Figure 7. Drive enable and disable times test circuit)		19	35	ns
t_{PLZ}	Output disable time	R_L= 110 Ω (Figure 10. Drive propagation time waveform and Figure 11. Drive enable and disable times test circuit (R_L= 110 Ω))		30	50	ns
t_{SKEW}	Differential output delay skew			1	3	ns
$t_{ZH(SHDN)}$	Driver enable from shutdown to output high			30	50	ns
$t_{ZL(SHDN)}$	Driver enable from shutdown to output low			19	35	ns

1. *Measured on $\lvert t_{PLH}(A)-t_{PHL}(A) \rvert$ and $\lvert t_{PLH}(B)-t_{PHL}(B) \rvert$*

Table 9. Receiver switching characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH} t_{PHL}	Propagation delay	V_{ID}= 0 V to 3 V, C_{L1}=15 pF (Figure 12. Drive enable and disable times waveforms (B) and Figure 13. Receiver propagation delay time test circuit)		30	50	ns
t_{RPDS}	|tPLH - tPHL| propagation delay skew	V_{ID}= 0 V to 3 V, C_{L1}=15 pF (Figure 12. Drive enable and disable times waveforms (B) and Figure 13. Receiver propagation delay time test circuit)		1	3	ns
t_{PZL}	Outputenable time	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		10	20	ns
t_{PZH}	Outputenable time	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		10	20	ns
t_{PHZ}	Outputdisable time	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		10	20	ns
t_{PLZ}	Outputdisable time	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		10	20	ns
$t_{ZH(SHDN)}$	Receiver enable from shutdown to output high	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		10	20	ns
$t_{ZL(SHDN)}$	Receiver enable from shutdown to output low	C_{RL}= 15 pF, (Figure 14. Receiver propagation delay time waveforms and Figure 18. Receiver enable and disable times waveform (S2 closed))		20	40	µs

5 Test circuits and typical characteristics

Figure 2. Driver and V_{OC} test load

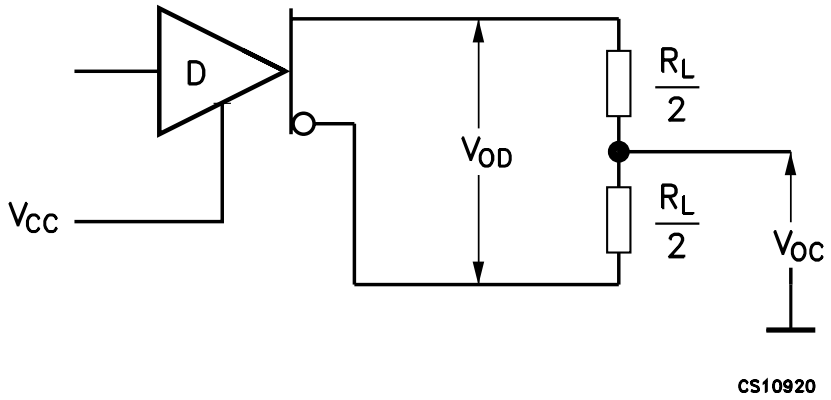


Figure 3. Driver V_{OD} with varying common mode voltage test load

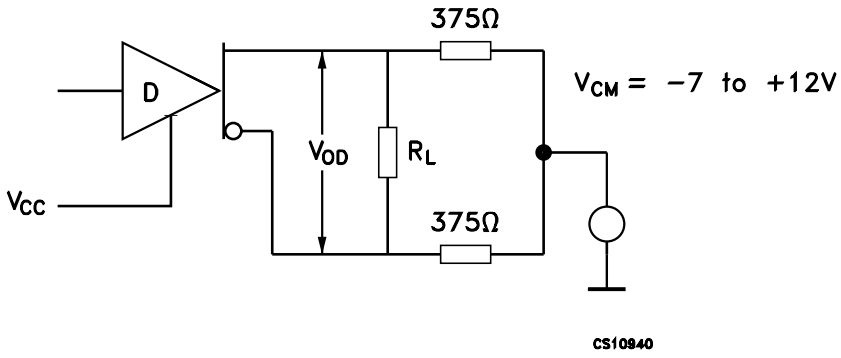


Figure 4. Receiver V_{OH} and V_{OL} test circuit

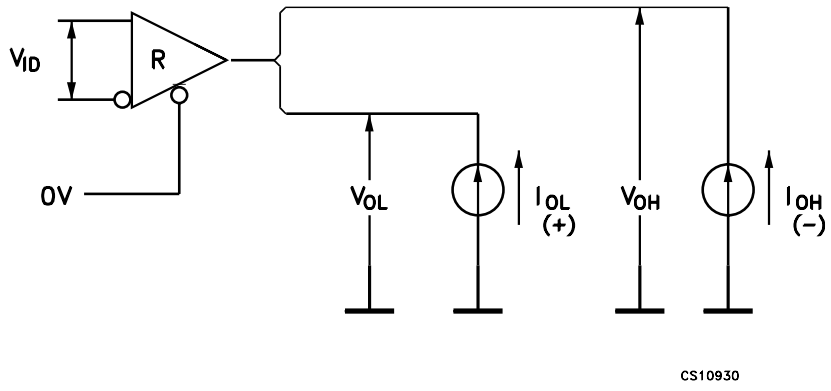


Figure 5. **Drive differential output delay transition time test circuit**

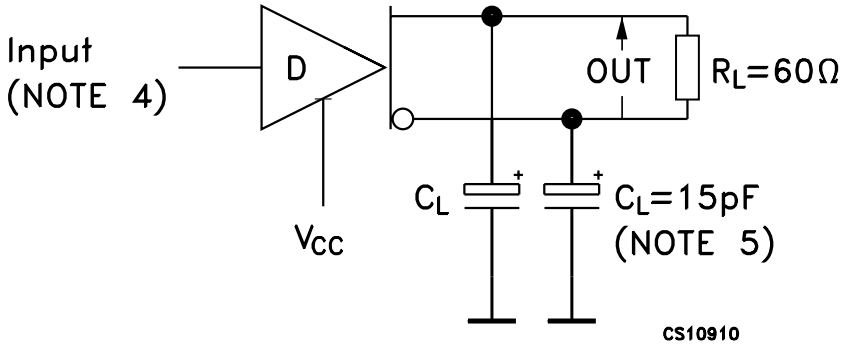


Figure 6. **Drive differential output delay transition time waveform**

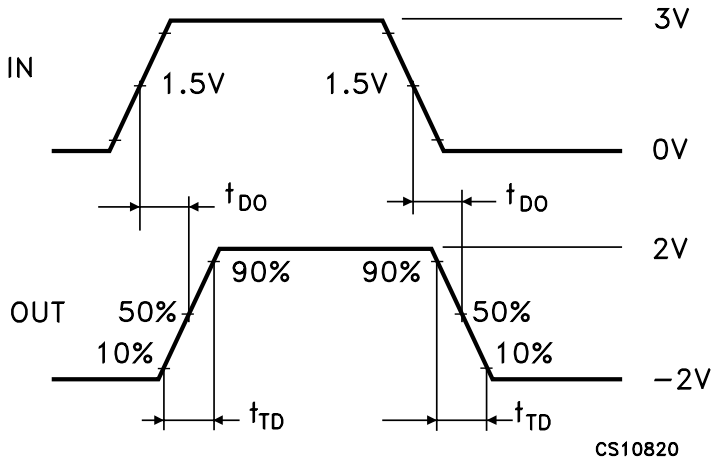


Figure 7. **Drive enable and disable times test circuit**

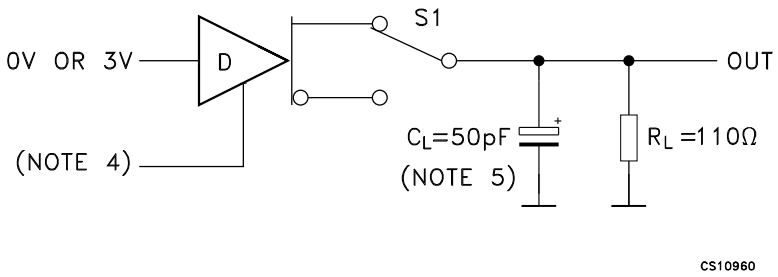


Figure 8. **Drive enable and disable times waveforms**

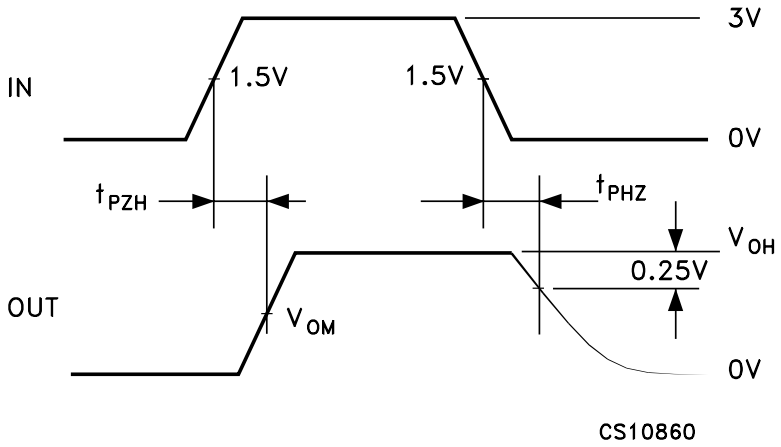


Figure 9. **Drive propagation time test circuit**

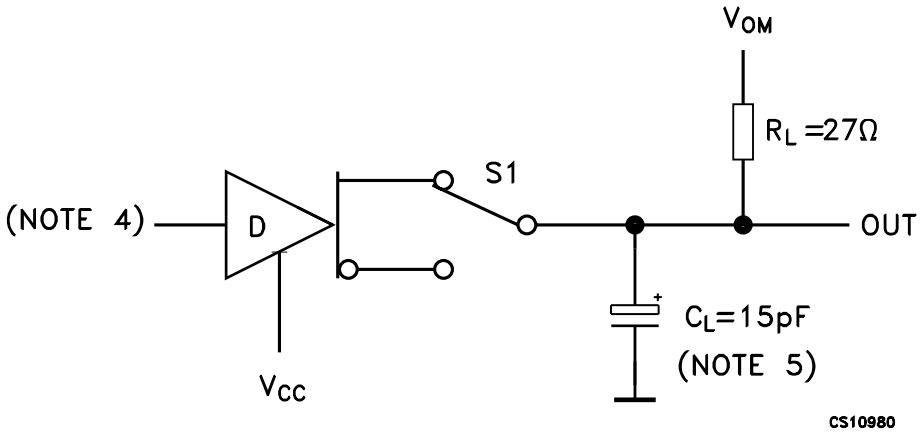


Figure 10. **Drive propagation time waveform**

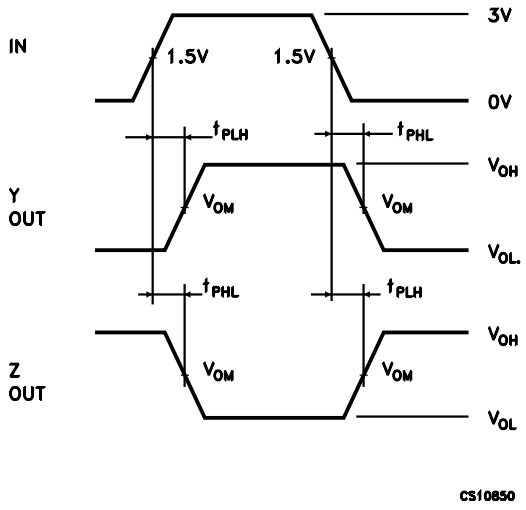


Figure 11. **Drive enable and disable times test circuit (R_L= 110 Ω)**

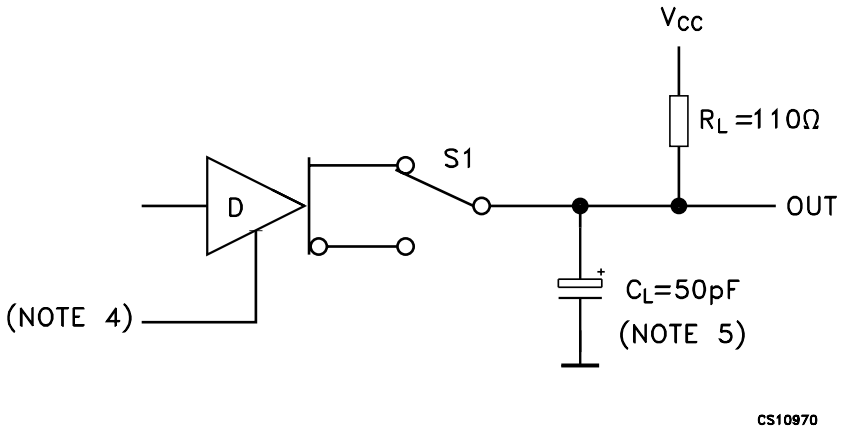


Figure 12. **Drive enable and disable times waveforms (B)**

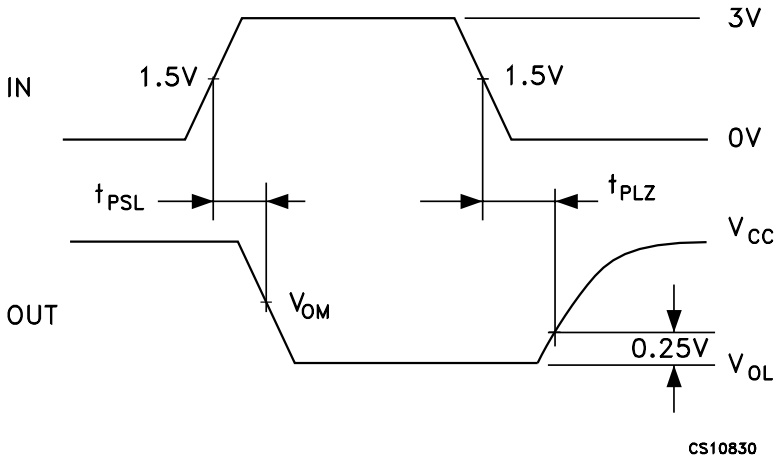


Figure 13. **Receiver propagation delay time test circuit**

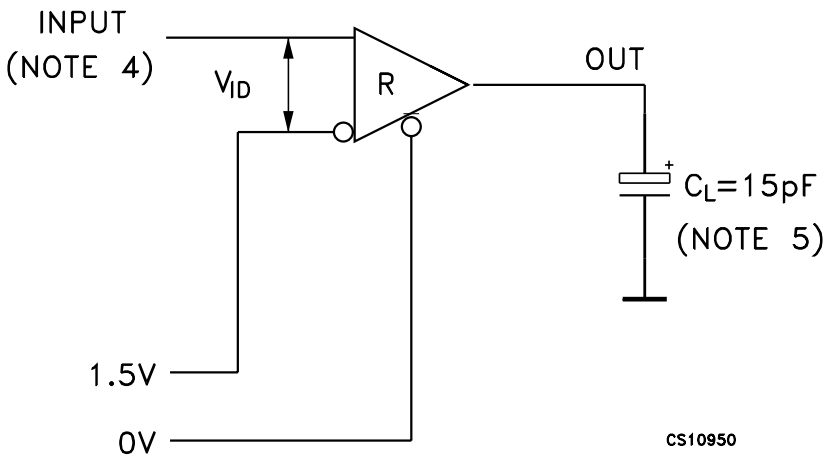


Figure 14. **Receiver propagation delay time waveforms**

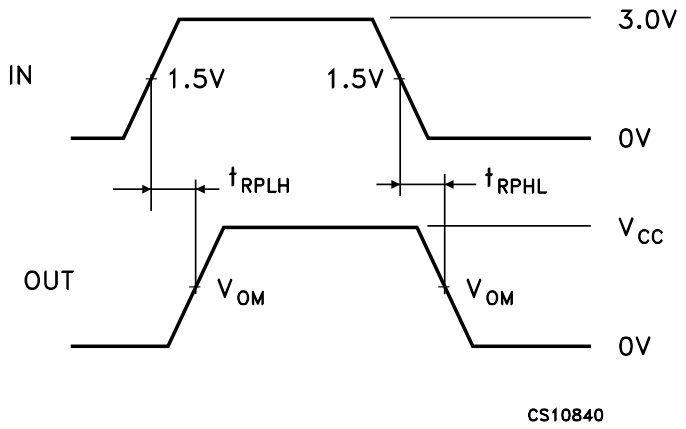


Figure 15. **Receiver enable and disable times test circuit (B)**

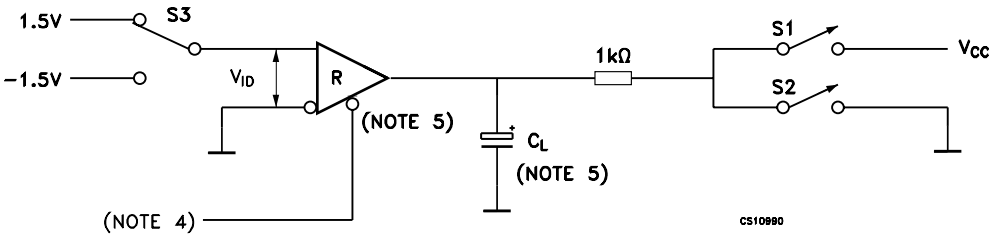


Figure 16. **Receiver enable and disable times waveform (S1 open)**

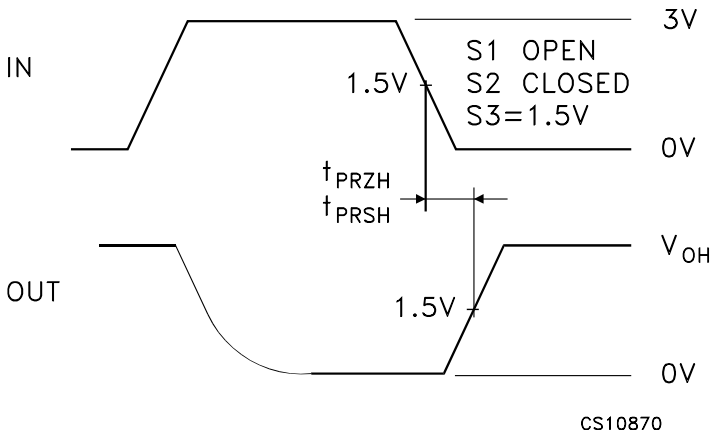


Figure 17. Receiver enable and disable times waveform (S1 closed)

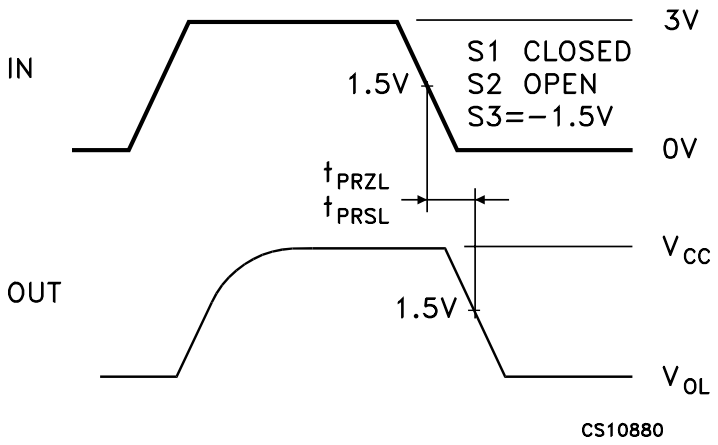


Figure 18. Receiver enable and disable times waveform (S2 closed)

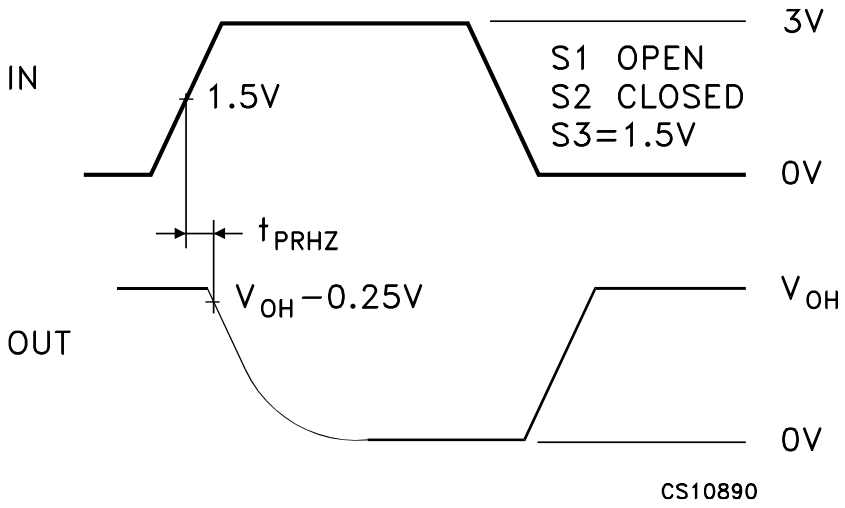


Figure 19. Receiver enable and disable times waveform (S2 open)

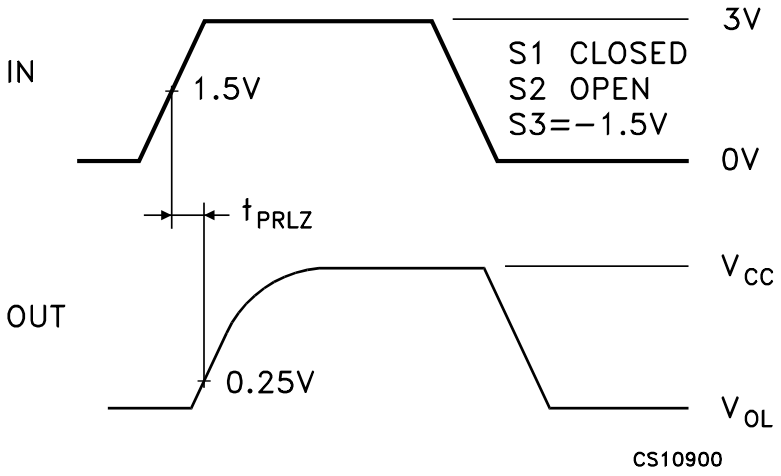


Figure 20. Receiver output current vs. output low voltage

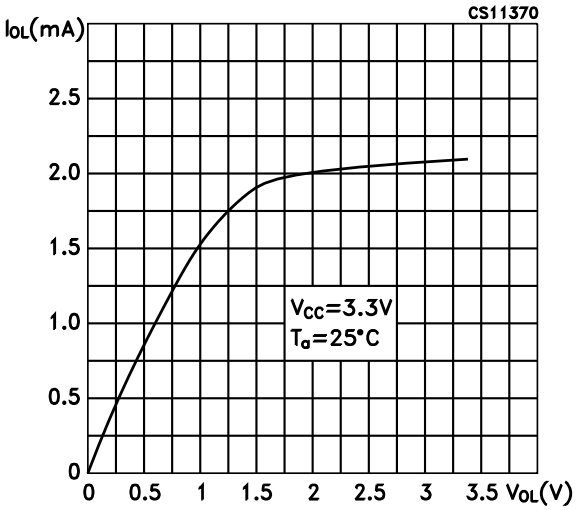


Figure 21. Receiver output current vs. output high voltage

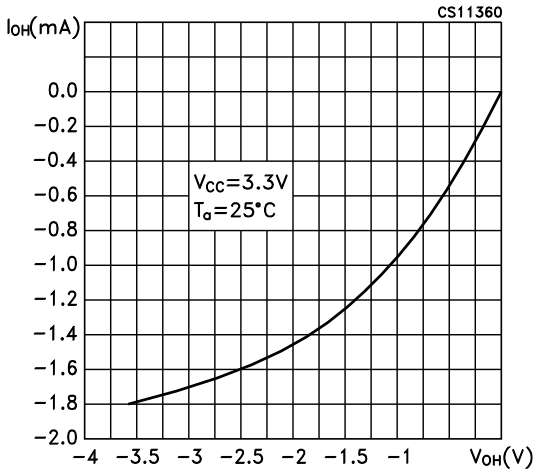


Figure 22. Low level driver output capability

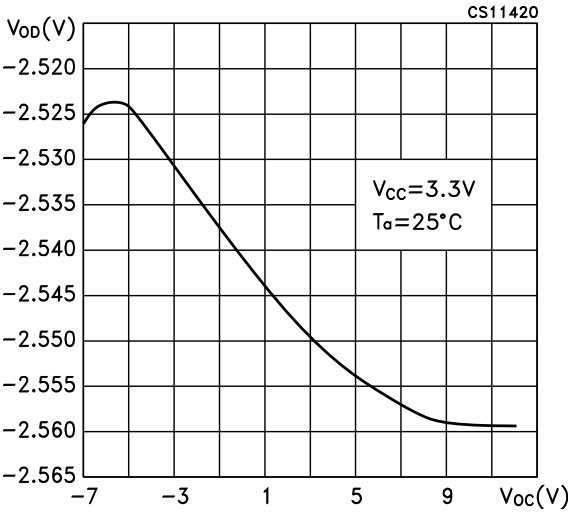


Figure 23. High level driver output capability

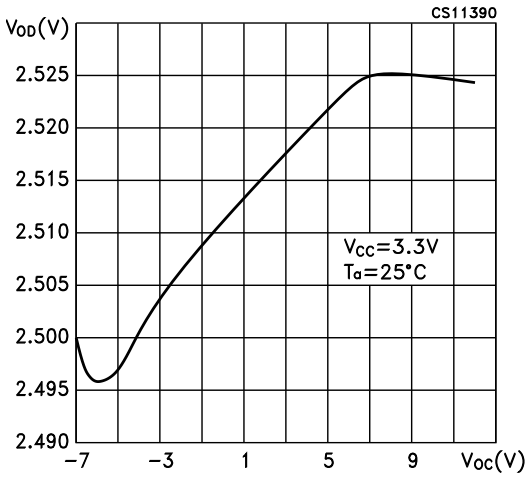


Figure 24. Receiver input characteristics

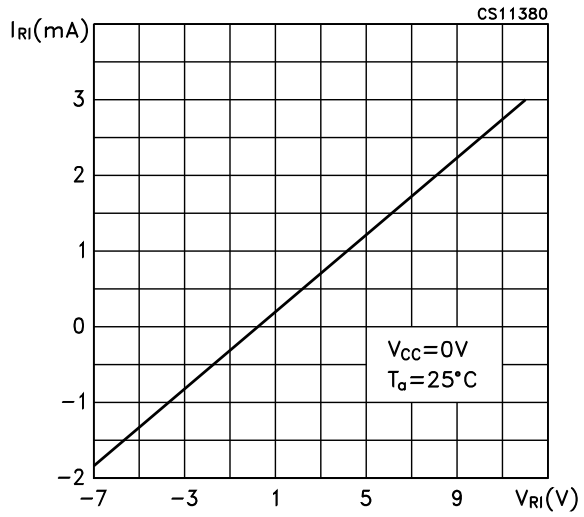


Figure 25. Driver short-circuit current

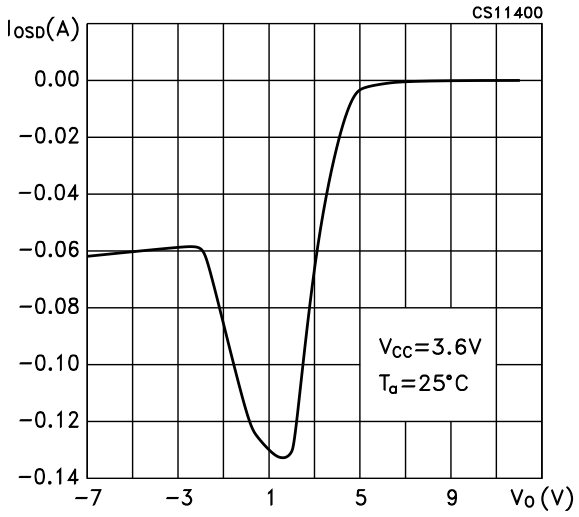
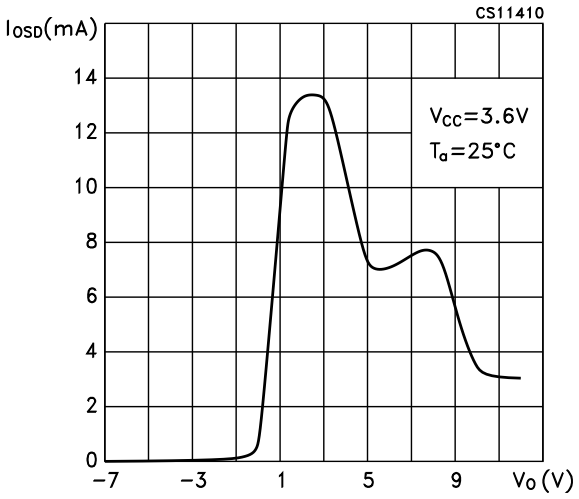


Figure 26. Driver short-circuit current



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 27. SO8 package outline

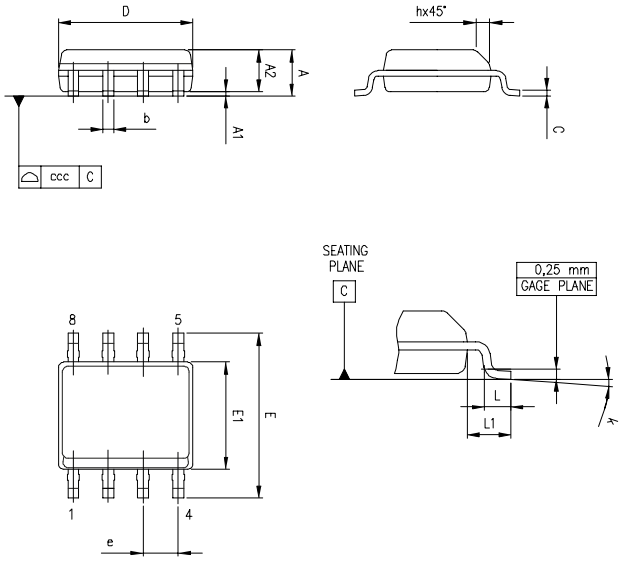


Table 10. SO-8 mechanical data

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

7 Ordering information

Table 11. **Ordering information**

Order codes	Temperature range	Package	Packing
ST1480ACDR/US	0 to 70 °C	SO-8 tape and reel	2500 parts per reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
06-Apr-2021	1	Initial release.

Contents

List of tables