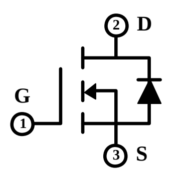
7A 800V N-channel Enhancement Mode Power MOSFET

1 Description

The F7N80 is an N-channel enhancement mode power field effect transistor. It optimized stripe cell structure design improves the EAS capability of the device.Which accords with the RoHS standard.



V_{DSS} = 800V

$R_{DS(on)}$ （TYP)= 1.5Ω

I_D = 7A

TO-262

2 Features

- Low Gate Charge
- Excellent RDSON
- Fast Switching
- Low ON Resistance
- 100% Single Pulse Avalanche Energy Test
- 100% Δ V_{DS} Test

3 Applications

- LED Power Switch Circuit
- Electronic Ballast
- ATX Power
- High Voltage H Bridge PWM Motor Drive

4 Electrical Characteristics

4.1 Absolute Maximum Rating（Tc=25℃,unless otherwise noted）

PARAMETER		SYMBOL	VALUE	UNIT
Drian-Source Voltage		V_{DS}	800	V
Gate-Drain Voltage		V_{GS}	±30	V
Drain Current(continuous)		I_D （T=25℃）	7	A
		（T=100℃）	4	A
Drain Current(Pulsed)(Note 1)		I_{DM}	28	A
Single Pulse Avalanche Energy(Note 5)		E_{AS}	150	mJ
Avalanche Energy Repetitive(Note 1)		E_{AR}	20	mJ
Avalanche Current(Note 1)		I_{AR}	2	A
Peak Diode Recovery dv/dt(Note 6)		dv/dt	5	V/ns
Total Dissipation	T_a=25℃	P_{tot}	2	W
	T_C=25℃	P_{tot}	48	W
Junction Temperature		T_j	150	℃
storage Temperature		T_{stg}	-55～150	℃
Maximum Temperature for soldering		T_L	300	℃

4.2 Thermal Characteristics

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance Junction to Case-sink	R_{thJC}	1.04	℃/W
Thermal Resistance Junction to Ambient	R_{thJA}	62.5	℃/W

4.3 Electrical Characteristics（Tc=25℃,unless otherwise noted）

PARAMETER	SYMBOL	Test Condition	VALUE			UNIT
			MIN	TYP	MAX	
Off Characteristics						
Drain-source Breakdown Voltage	BV_{DSS}	I_D=250μA,V_{GS}=0V	800	--	--	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=800V,V_{GS}=0V,T_C=25℃	--	--	25	μA
		V_{DS}=640V,V_{GS}=0V,T_C=125℃	--	--	250	μA
Gate-to-Source Forward Leakage	I_{GSSF}	V_{GS}=+30V, V_{DS}=0V	--	--	100	nA
Gate-to-Source Reverse Leakage	I_{GSSR}	V_{GS}= - 30V, V_{DS}=0V	--	--	−100	nA
On Characteristics(Note 3)						
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	--	4	V
Drain-source on Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=3.5A	--	1.5	1.8	Ω
Dynamic Characteristics(Note 4)						
Forward Transfer conductance	g_{fs}	V_{DS}=15V,I_D=3.5A	--	7.5	--	S
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V,f=1.0MHz	--	1350	--	pF
Output Capacitance	C_{oss}		--	115	--	
Reverse Transfer Capacitance	C_{rss}		--	12	--	
Switching Characteristics(note4)						
Turn-on Delay Time	$t_{d(on)}$	I_D=7A, V_{DD}=400V, V_{GS}=10V, R_G=12Ω	--	15	--	nS
Turn-on Rise Time	t_r		--	25	--	nS
Turn-off Delay Time	$t_{d(off)}$		--	51	--	nS
Turn-off Fall Time	t_f		--	31	--	nS
Total Gate Charge	Q_g	I_D=7A,V_{DD}=400V,V_{GS}=10V	--	34	--	nC
Gate-to-Source Charge	Q_{gs}		--	6	--	
Gate-to-Drain("Miller")Charge	Q_{gd}		--	14	--	
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{FSD}	V_{GS}=0V,I_S=7A	--	--	1.5	V
Diode Forward Current (Note 2)	I_S		--	--	7	A
Reverse Recovery Time	t_{rr}	T_J=25℃,I_F=7A, dI_F/dt=100A/μS,V_{GS}=0V	--	186	--	nS
Reverse Recovery Charge	Q_{rr}		--	878	--	nC

Notes：

1: Repetitive rating, pulse width limited by maximum junction temperature.

2: Surface mounted on FR4 Board, t≤10sec.

3: Pulse width ≤ 300μs, duty cycle ≤ 2%.

4: Guaranteed by design, not subject to production.

5. L=10mH,I_D=5.5A,V_{DD}=50V,V_{GATE}=800V,Start T_J=25℃.

6. I_{SD}=7A,di/dt≤100A/μs,V_{DD}≤BV_{DSS}, Start T_J=25℃.

5 Typical characteristics diagrams

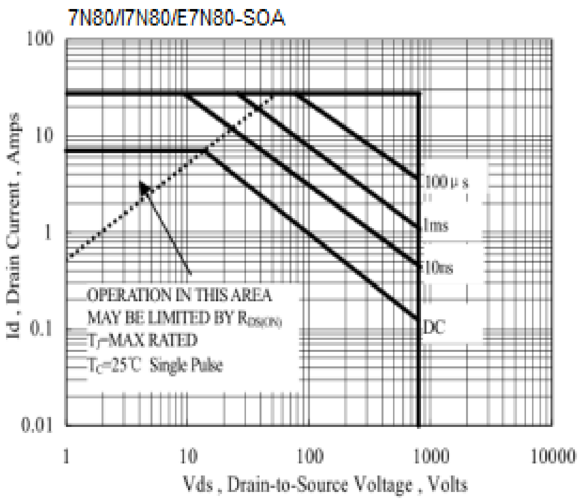


Figure 1a Maximum Forward Bias Safe Operating Area

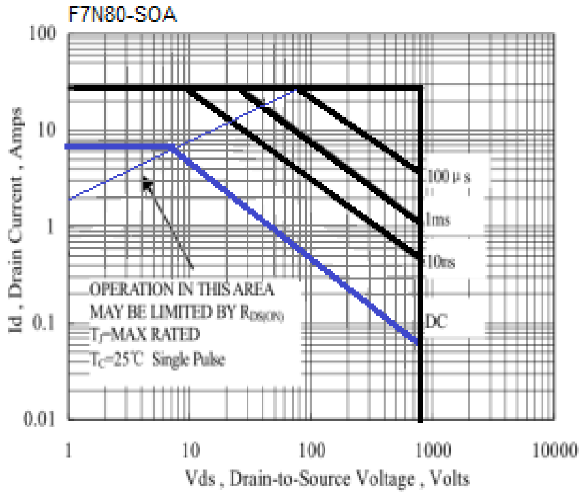


Figure 1b Maximum Forward Bias Safe Operating Area

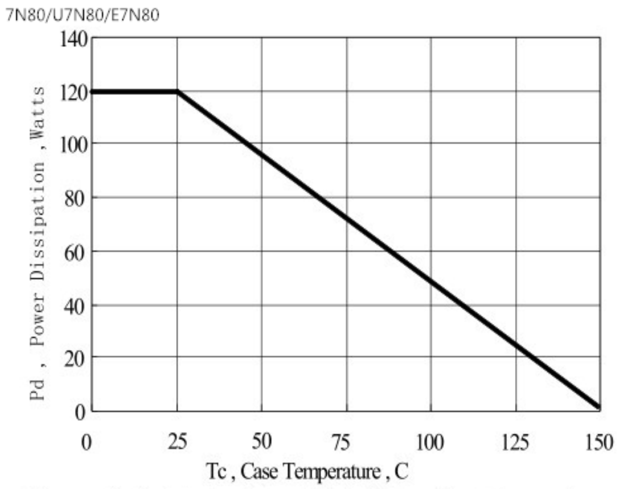


Figure.2(a) Maximum Power Dissipation VS Case Temperature

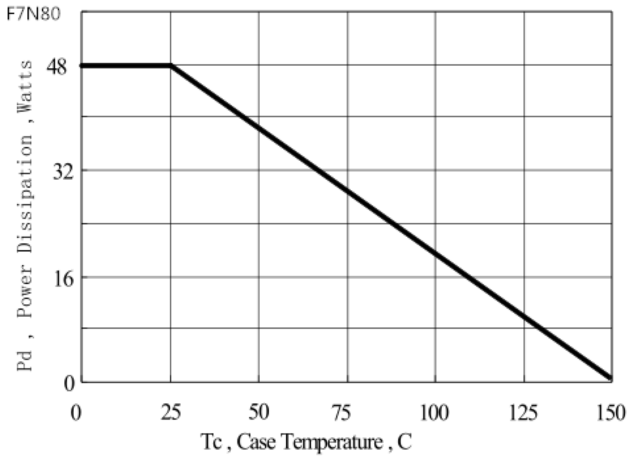


Figure.2(b) Maximum Power Dissipation VS Case Temperature

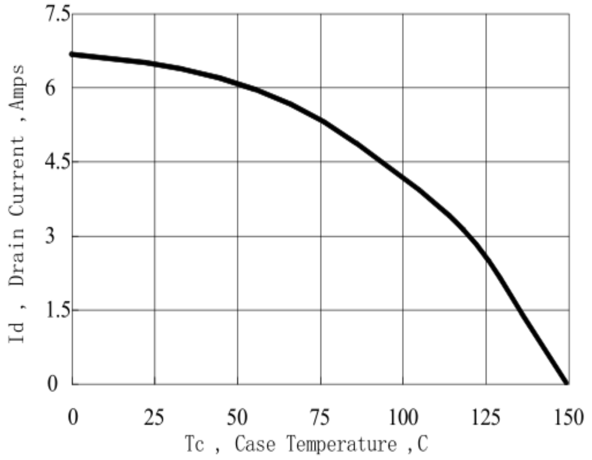


Figure 3 Maximum Continuous Drain Current vs Case Temperature

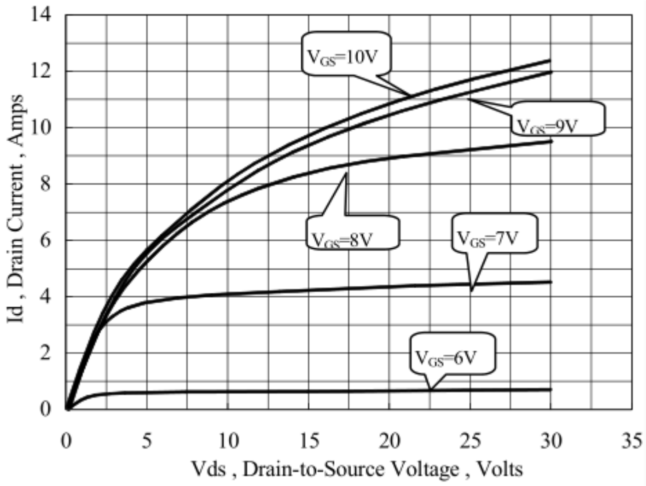


Figure 4 Typical Output Characteristics

5 Typical characteristics diagrams(continues)

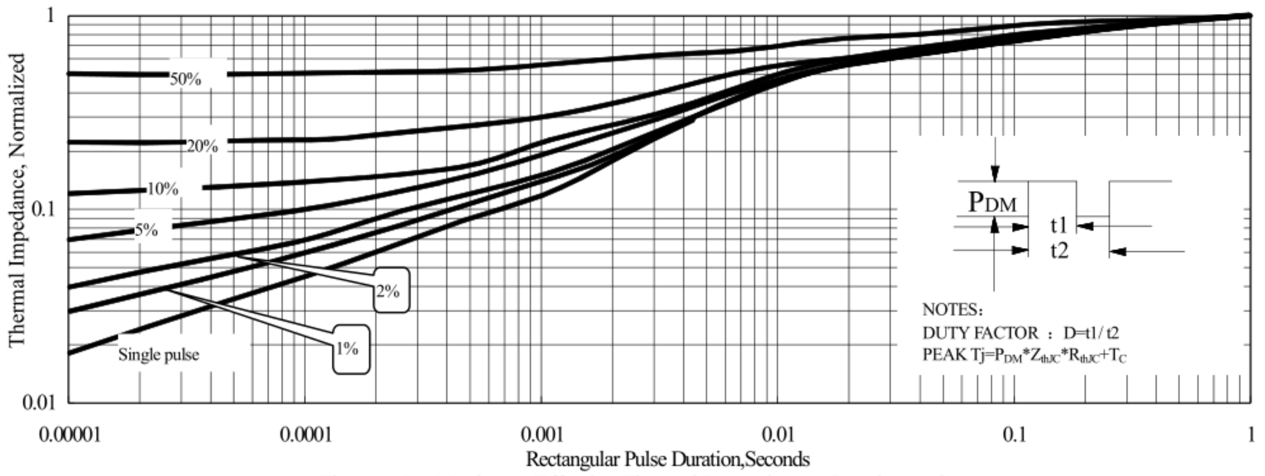


Figure 5 Maximum Effective Thermal Impendance , Junction to Case

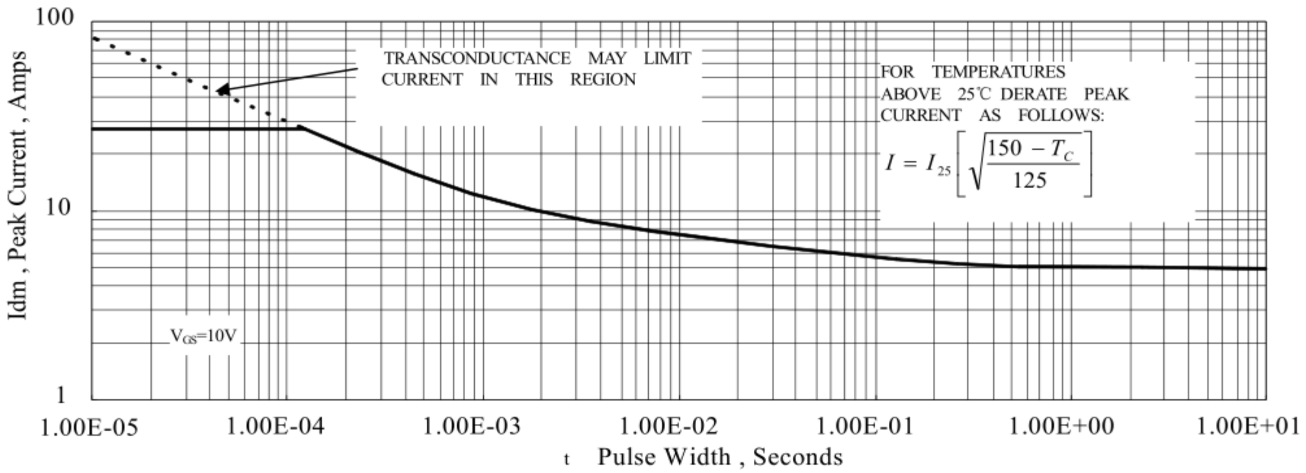


Figure 6 Maximun Peak Current Capability

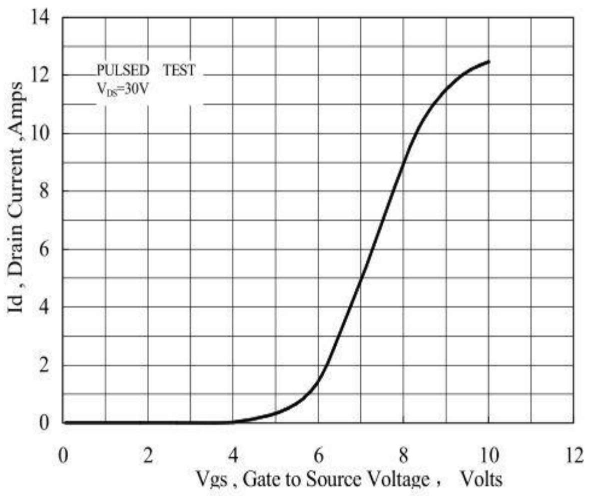


Figure 7 Typical Transfer Characteristics

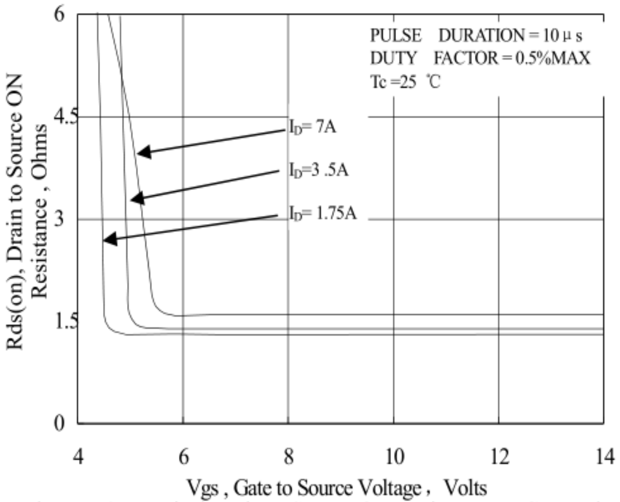


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

5 Typical characteristics diagrams(continues)

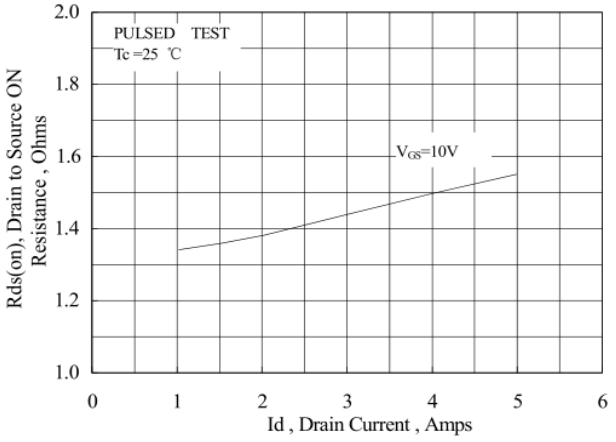


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

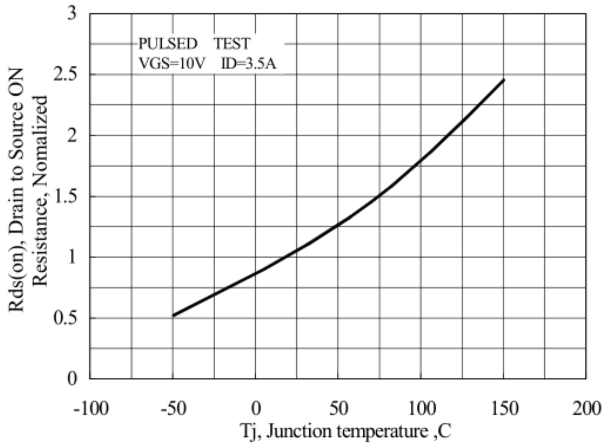


Figure 10 Typical Drian to Source on Resistance vs Junction Temperature

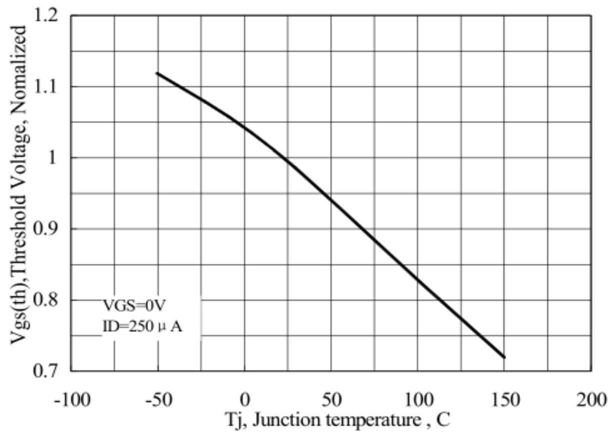


Figure 11 Typical Theshold Voltage vs Junction Temperature

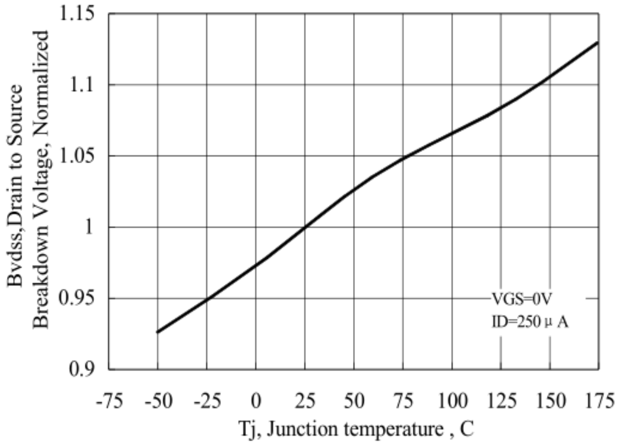


Figure 12 Typical Breakdown Voltage vs Junction Temperature

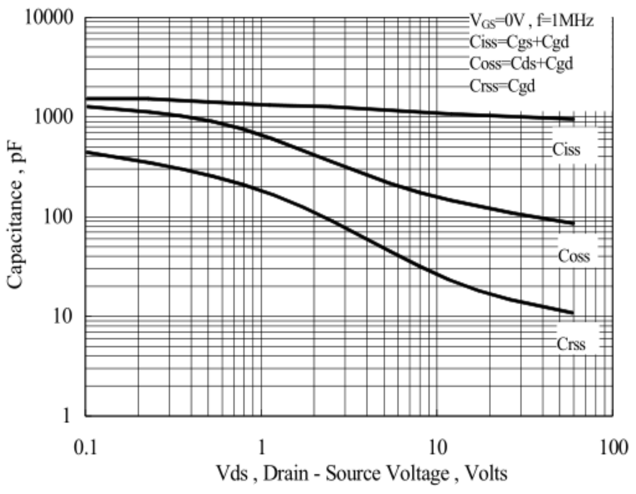


Figure 13 Typical Capacitance vs Drain to Source Voltage

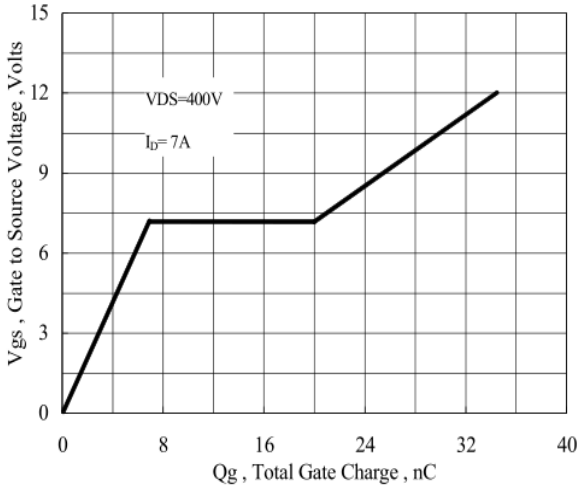


Figure 14 Typical Gate Charge vs Gate to Source Voltage

5 Typical characteristics diagrams(continues)

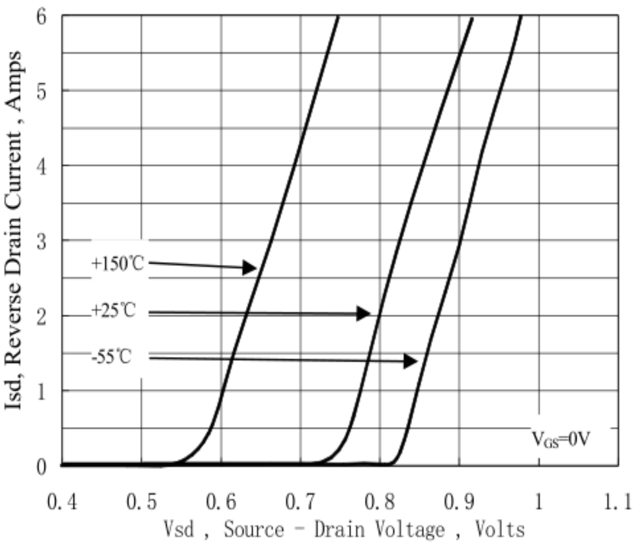


Figure 15 Typical Body Diode Transfer Characteristics

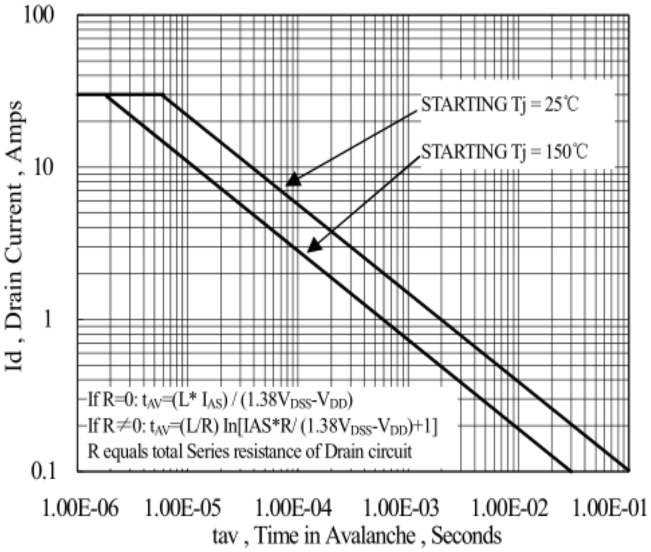
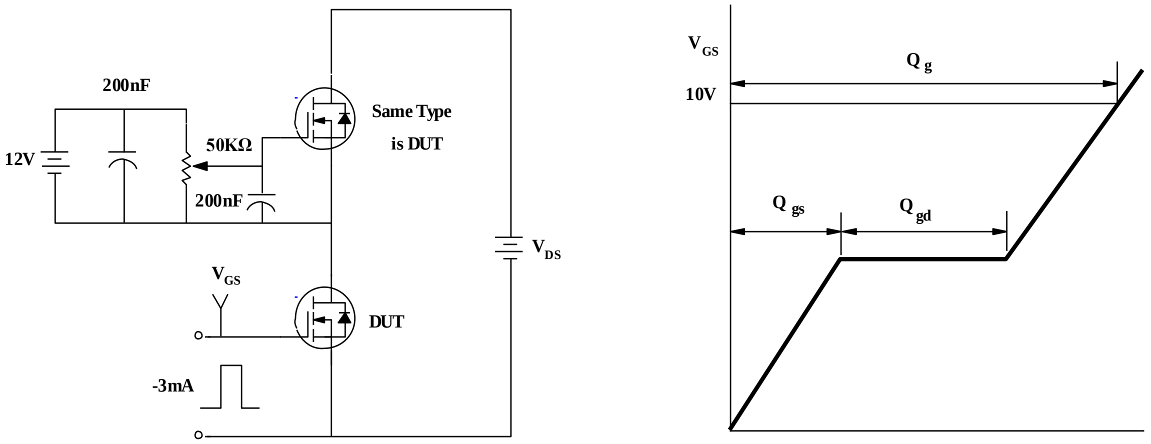
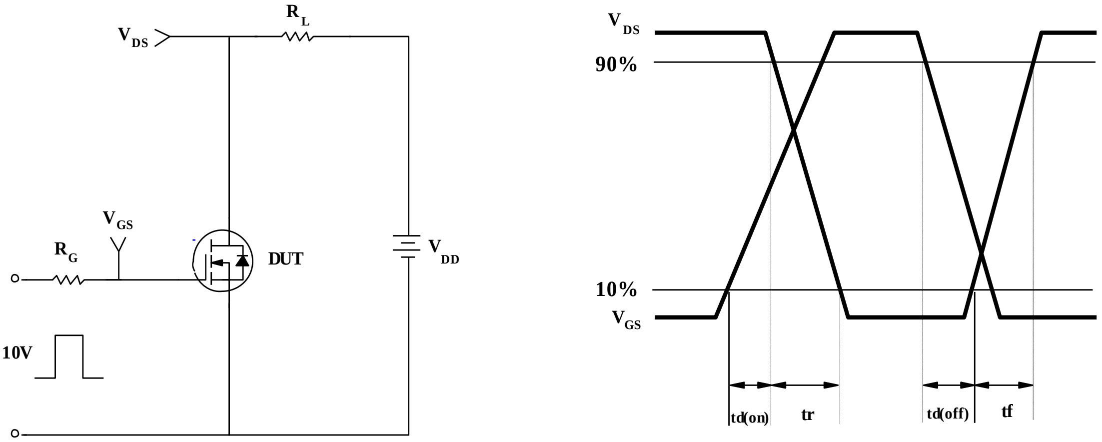


Figure 16 Unclamped Inductive Switching Capability

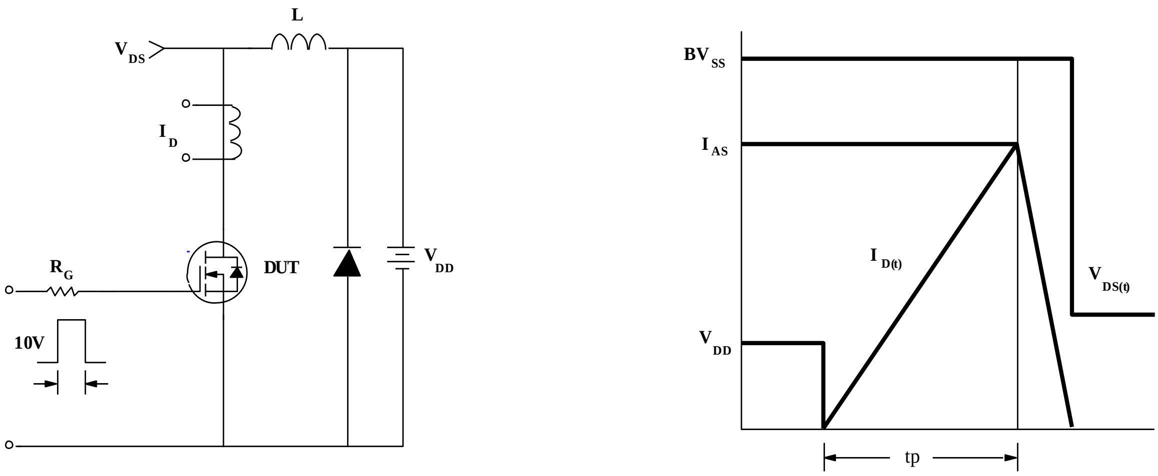
6 Typical Test Circuit and Waveform



1) Gate Charge Test Circuit & Waveform

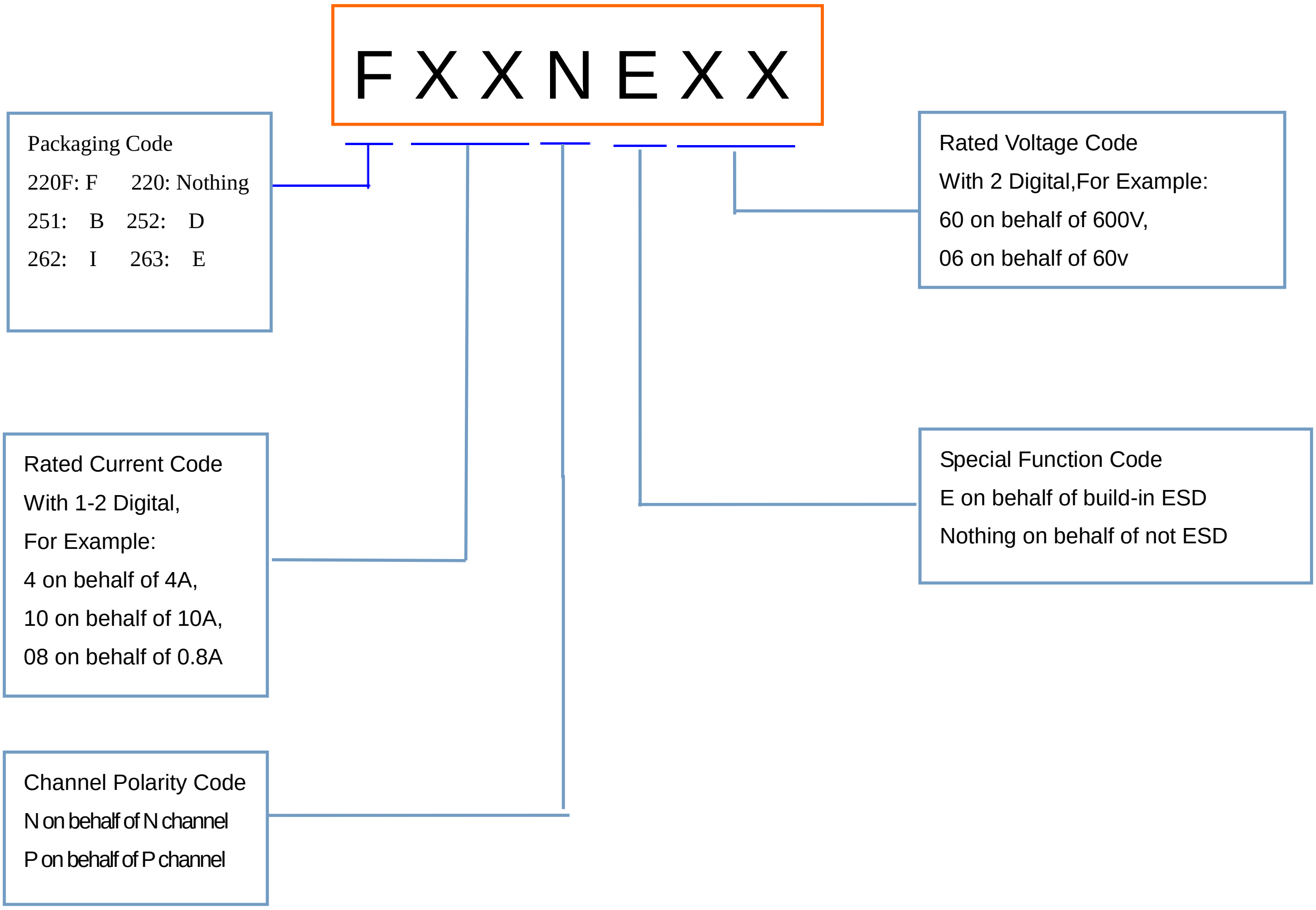


2) Switching Test Circuit & Waveforms



3) Unclamped Inductive Test Circuit & Waveforms

7 Product Names Rules



F X X N E X X

Packaging Code
220F: F 220: Nothing
251: B 252: D
262: I 263: E

Rated Voltage Code
With 2 Digital,For Example:
60 on behalf of 600V,
06 on behalf of 60v

Rated Current Code
With 1-2 Digital,
For Example:
4 on behalf of 4A,
10 on behalf of 10A,
08 on behalf of 0.8A

Special Function Code
E on behalf of build-in ESD
Nothing on behalf of not ESD

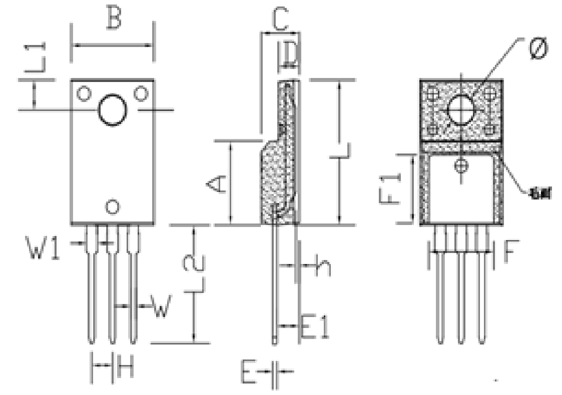
Channel Polarity Code
N on behalf of N channel
P on behalf of P channel

8 Product Specifications and Packaging Models

Product Model	Package Type	Mark Name	RoHS	Package	Quantity
7N80	TO-220C	7N80	Pb-free	Tube	1000/box
F7N80	TO-220F	F7N80	Pb-free	Tube	1000/box
I7N80	TO-262	I7N80	Pb-free	Tube	1000/box
E7N80	TO-263	E7N80	Pb-free	Tape ＆ Reel	800/box

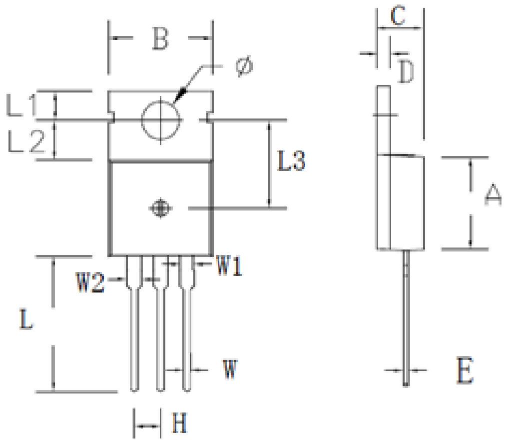
9 Dimensions

TO-220F PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	8.80	9.30	0.346	0.366
B	10.00	10.50	0.394	0.413
C	4.30	4.90	0.169	0.193
D	2.30	2.70	0.091	0.106
L	15.55	16.15	0.612	0.636
h	0.40	0.60	0.016	0.024
L1	3.15	3.55	0.124	0.140
L2	12.65	13.35	0.498	0.526
W	0.70	0.90	0.028	0.035
W1	1.15	1.55	0.045	0.061
H	2.54 TYP		0.100 TYP	
E	0.48	0.53	0.019	0.021
φ	2.90	3.40	0.114	0.134
E1	2.40	2.90	0.094	0.114
F	7.75	8.25	0.305	0.325
F1	7.35	7.85	0.289	0.309

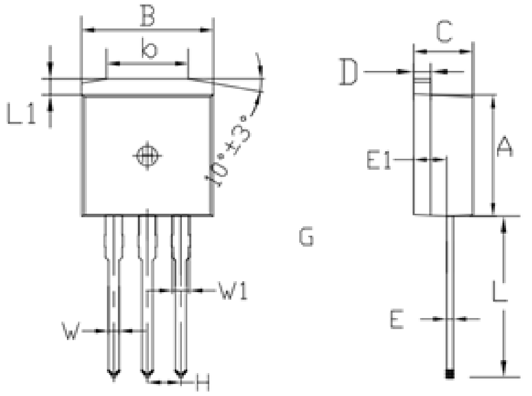
TO-220C PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	8.80	9.30	0.346	0.366
B	9.70	10.30	0.382	0.406
C	4.25	4.75	0.167	0.187
D	1.20	1.45	0.047	0.057
E	0.40	0.60	0.016	0.024
H	2.54 TYP		0.100 TYP	
W	0.60	0.95	0.024	0.037
W1	1.05	1.45	0.041	0.057
W2	1.20	1.60	0.047	0.063
L	12.60	13.40	0.496	0.528
L1	2.45	2.95	0.096	0.116
L2	3.45	3.95	0.136	0.156
L3	8.15	8.65	0.321	0.341
Φ	3.50	3.90	0.138	0.154

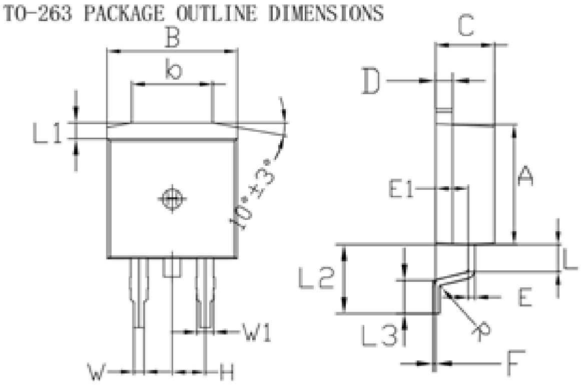
9 Dimensions(continues)

TO-262 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	8.80	9.30	0.346	0.366
B	9.70	10.30	0.382	0.406
C	4.25	4.75	0.167	0.187
D	1.20	1.45	0.047	0.057
E	0.40	0.60	0.016	0.024
L	12.25	13.75	0.482	0.541
L1	1.15	1.45	0.045	0.057
E1	2.4	2.6	0.0945	0.1024
W	0.80	0.82	0.0315	0.034
W1	1.20	1.30	0.047	0.051
H	2.54 TYP		0.200 TYP	
b	5.50	6.50	0.216	0.256

TO-263 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	min.	max.	min.	max.
A	8.80	9.30	0.346	0.366
B	9.70	10.30	0.382	0.406
C	4.25	4.75	0.167	0.187
D	1.20	1.45	0.047	0.057
E	0.40	0.60	0.016	0.024
L	1.90	2.30	0.075	0.091
L1	1.15	1.45	0.045	0.057
R	0.24	0.26	0.0095	0.0102
W	0.80	0.82	0.0315	0.0323
W1	1.20	1.30	0.047	0.051
H	2.54 TYP		0.200 TYP	
b	5.50	6.50	0.216	0.256
E1	2.4	2.6	0.0946	0.1024
L2	5.20	5.80	0.205	0.228
L3	2.20	3.20	0.087	0.126
F	0.03	0.23	0.0012	0.0091

10 Attentions

- ROUM Semiconductor Technology CO.,LTD. reserves the right to change the specification without prior notice! The customer should obtain the latest version of the information before making the order and verify that the information is complete and up to date.
- It is the responsibility of the purchaser for any failure or failure of any semiconductor product under certain conditions. It is the responsibility of the purchaser to comply with safety standards and to take safety measures in the system design and machine manufacturing of Roma products in order to avoid potential risk of failure. Injury or property damage.
- Product promotion is endless, our company will be dedicated to provide customers with better products.

11 Appendix

Revision history:

Date	REV.	Description	Page
2017.03.30	1.0	Original	