

## P-Channel 100 V (D-S) MOSFET

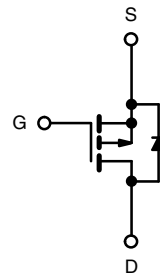
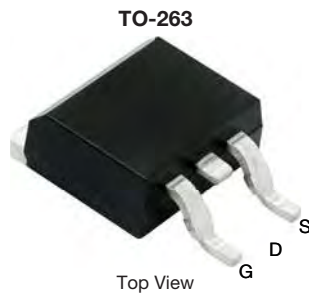
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
- 100	0.082 at V <sub>GS</sub> = - 10 V	- 30	70 nC
	0.092 at V <sub>GS</sub> = - 4.5 V	- 25	

### FEATURES

- Maximum 175 °C junction temperature
- 100 % R<sub>g</sub> and UIS tested
- DT-TrenchPower MOSFET



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	- 100	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>b</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	- 30	
		T <sub>C</sub> = 70 °C	- 26	
		T <sub>A</sub> = 25 °C	- 10 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	- 6.5 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	- 120	A	
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	T <sub>C</sub> = 25 °C		- 30 <sup>a</sup>
		T <sub>A</sub> = 25 °C		- 5.15 <sup>b, c</sup>
Avalanche Current	I <sub>AS</sub>	- 28		mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	415		
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	215	
		T <sub>C</sub> = 70 °C	159	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 10 s	18	22	°C/W
		Steady State	45	50	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.59	1.2		

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 50 °C/W.

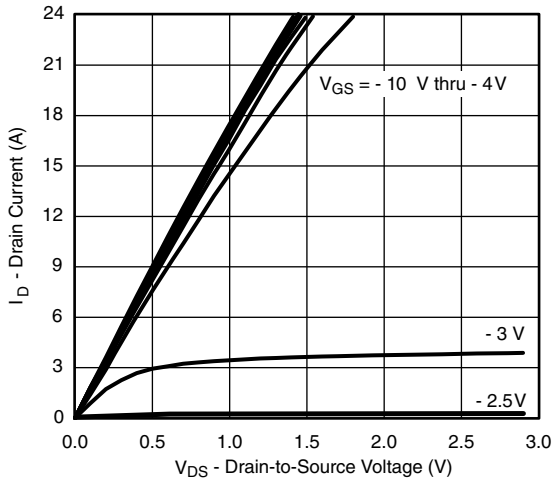
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-100			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-109		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.5		-3.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		0.082	0.099	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$		0.092	0.115	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -10\text{ A}$		16		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5260		pF
Output Capacitance	$C_{oss}$			710		
Reverse Transfer Capacitance	$C_{rss}$			79		
Total Gate Charge	$Q_g$	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		70	100	nC
				33	50	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -8\text{ A}$		15		
Gate-Drain Charge	$Q_{gd}$			23		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		5		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 6.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		26		ns
Rise Time	$t_r$			70		
Turn-Off Delay Time	$t_{d(off)}$			45		
Fall Time	$t_f$			39		
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			-30	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				-120	
Body Diode Voltage	$V_{SD}$	$I_S = -10\text{ A}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = -10\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		60	90	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			150	215	nC
Reverse Recovery Fall Time	$t_a$			48		ns
Reverse Recovery Rise Time	$t_b$			15		

Notes:

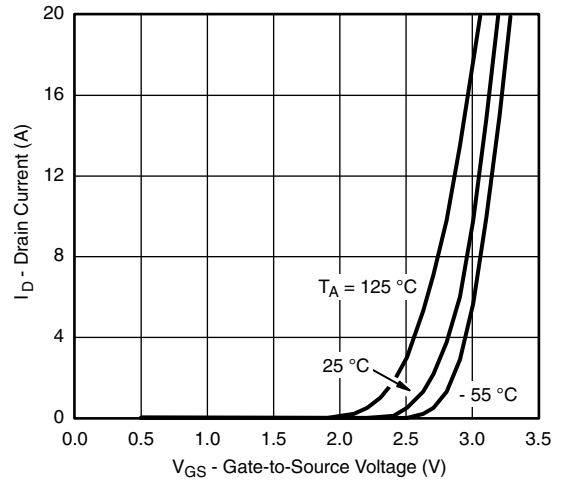
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

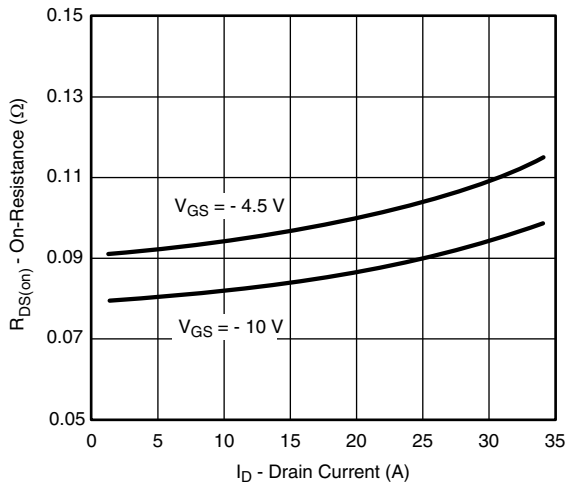
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



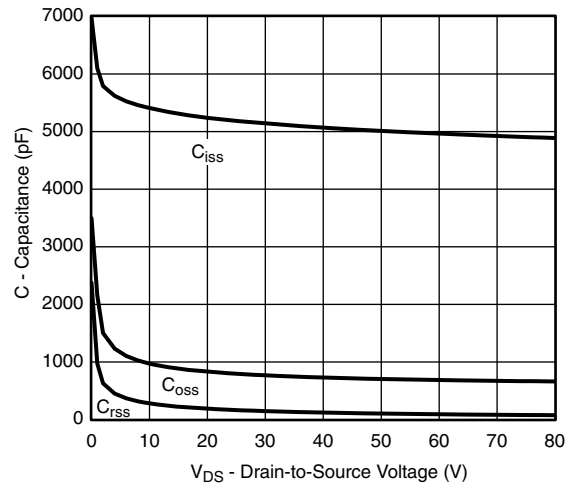
**Output Characteristics**



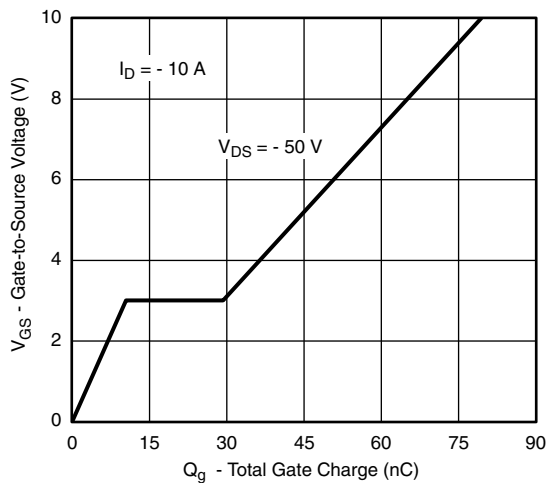
**Transfer Characteristics**



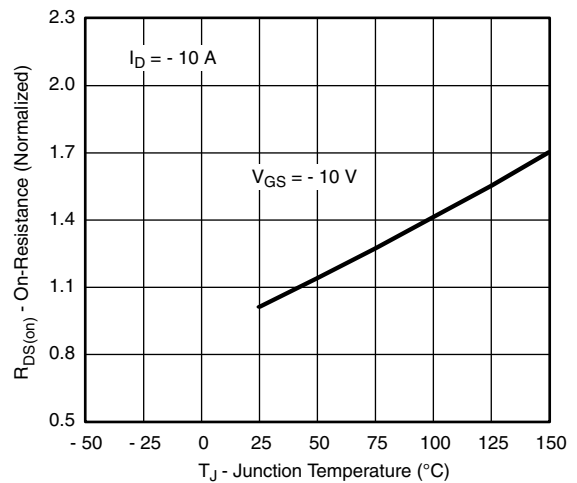
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

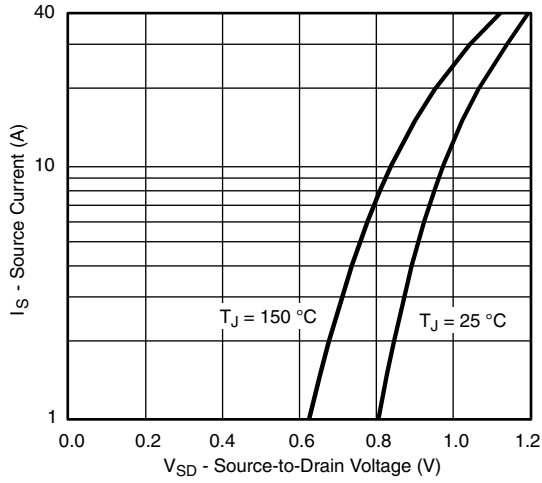


**Gate Charge**

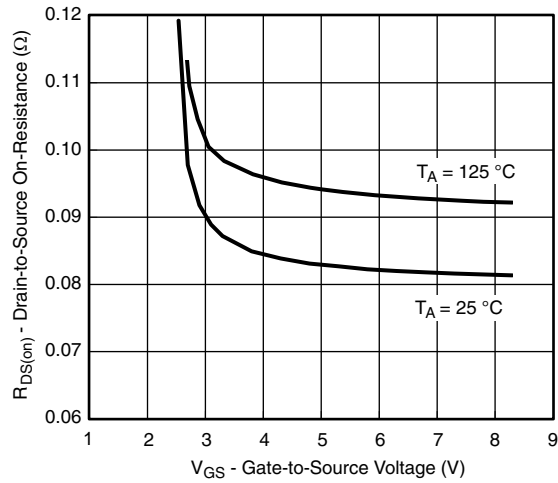


**On-Resistance vs. Junction Temperature**

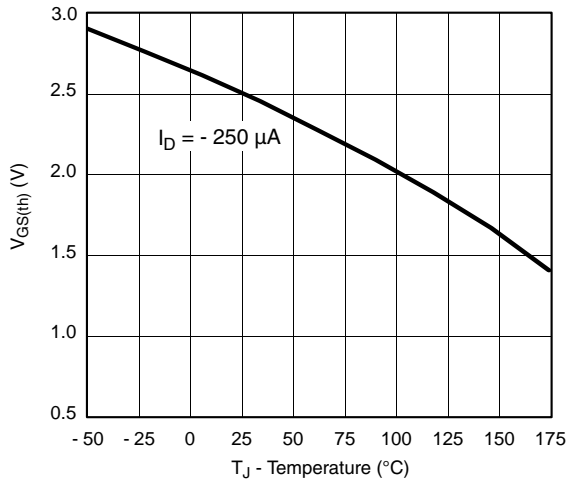
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



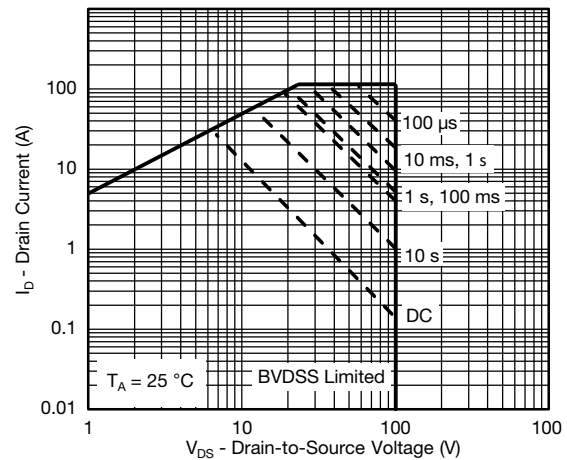
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

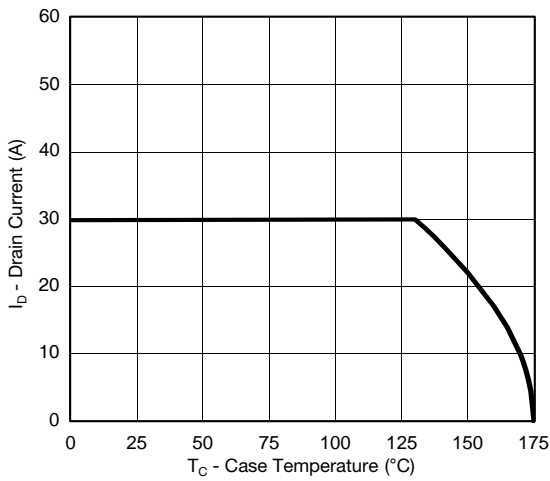


**Threshold Voltage**

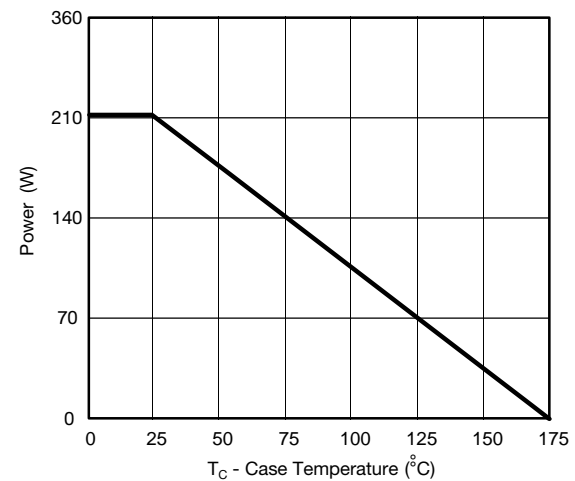


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

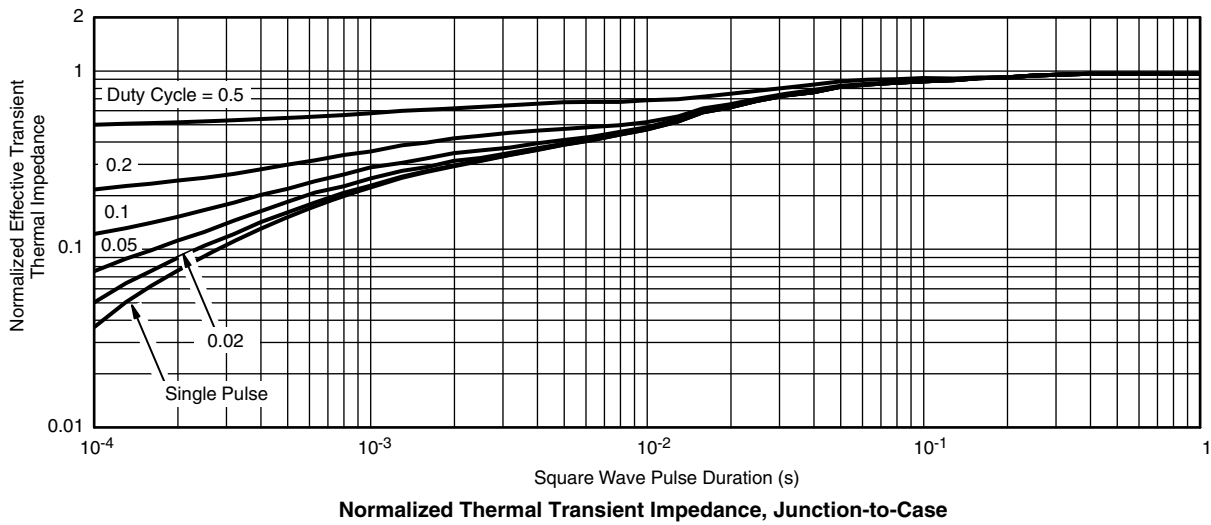
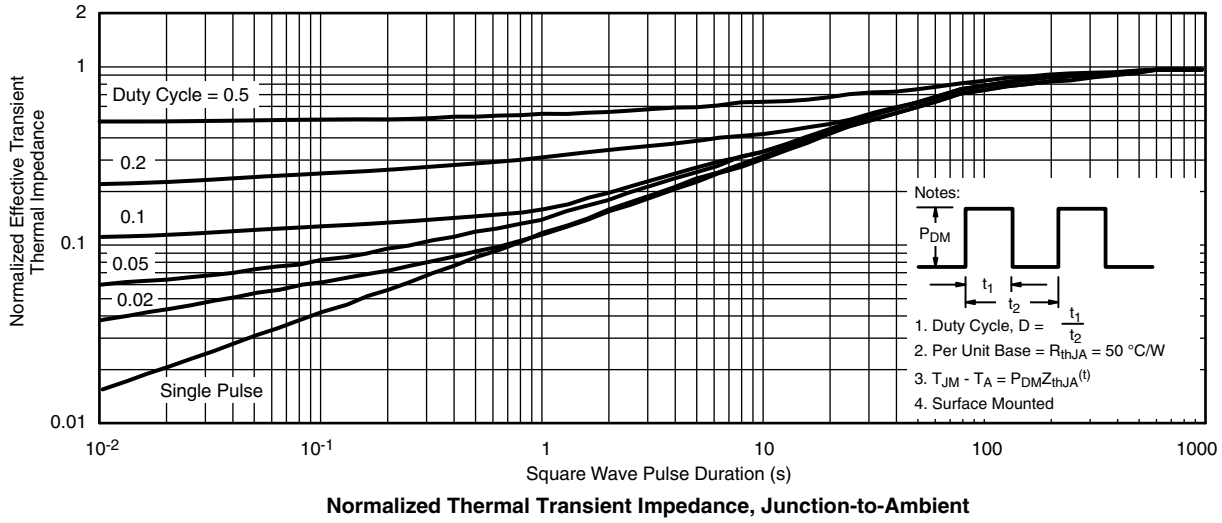


**Current Derating\***

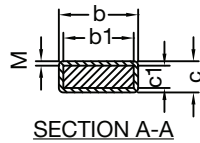
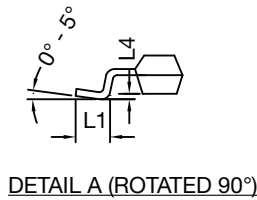
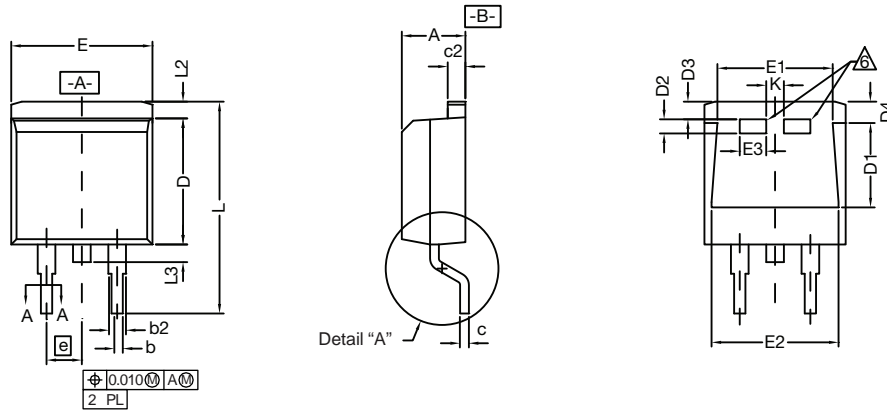


**Single Pulse Power, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



## TO-263 (D<sup>2</sup>PAK): 3-LEAD

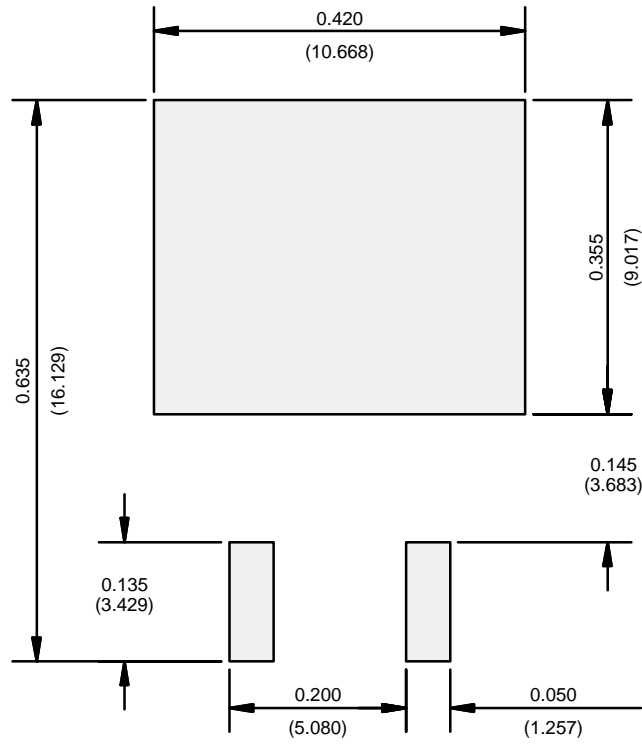


DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
<b>E3</b>	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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