

P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)
- 100	0.075 at V _{GS} = - 10 V	- 9	22
	0.08 at V _{GS} = - 4.5 V	- 8	

FEATURES

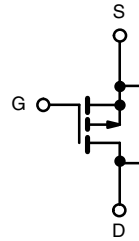
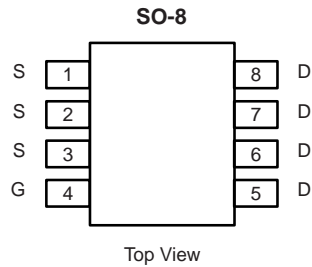
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- Networking
- LED Lighting Application
- Portable Equipment
- DC-DC Power Management



RoHS
COMPLIANT



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 9
		T _C = 70 °C	- 7.5
Pulsed Drain Current	I _{DM}	- 36	A
Avalanche Current	I _{AS}	- 8.8	
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	5.5 ^b
		T _C = 70 °C	3.5
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	45	°C/W
Junction-to-Case (Drain)	R _{thJC}	3.8	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

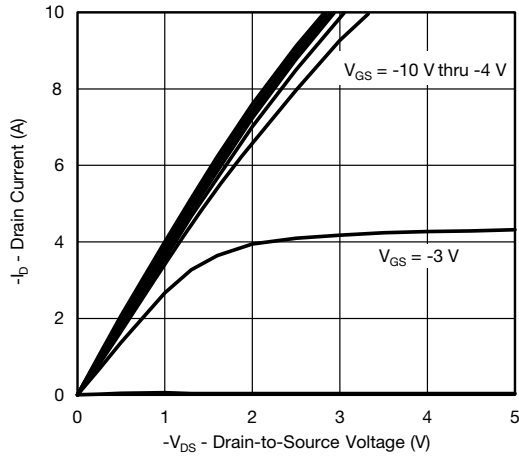
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	- 100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	- 1		- 3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			- 50	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -6\text{ A}$		0.075	0.095	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		0.08	0.110	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -20\text{ V}, I_D = -6\text{ A}$		15.5		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -50\text{ V}, f = 1\text{ MHz}$		3720		pF
Output Capacitance	C_{oss}			104		
Reverse Transfer Capacitance	C_{rss}			43		
Total Gate Charge ^c	Q_g	$V_{DS} = -50\text{ V}, V_{GS} = -10\text{ V}, I_D = -6\text{ A}$		53.5		nC
				22		
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = -50\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		14		
Gate-Drain Charge ^c	Q_{gd}			8.8		
Gate Resistance	R_g	$f = 1\text{ MHz}$		7.5		Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -50\text{ V}, R_L = 17.2\text{ }\Omega$ $I_D \equiv -6\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		10		ns
Rise Time ^c	t_r			22		
Turn-Off Delay Time ^c	$t_{d(off)}$			85		
Fall Time ^c	t_f			50		
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	I_S				- 9	A
Pulsed Current	I_{SM}				- 36	
Forward Voltage ^a	V_{SD}	$I_F = -2.9\text{ A}, V_{GS} = 0\text{ V}$		- 0.7	- 1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -2.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		26		ns
Reverse Recovery Charge	Q_{rr}				38	

Notes:

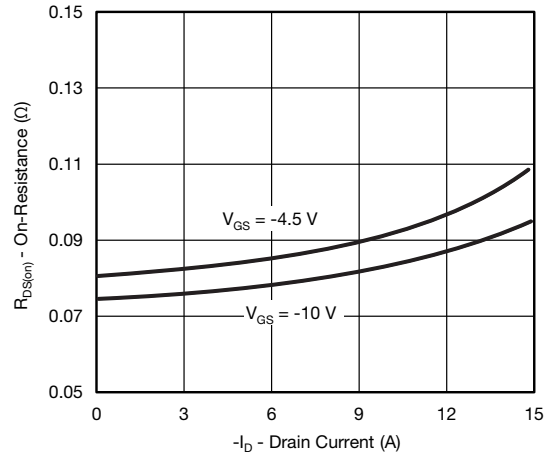
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

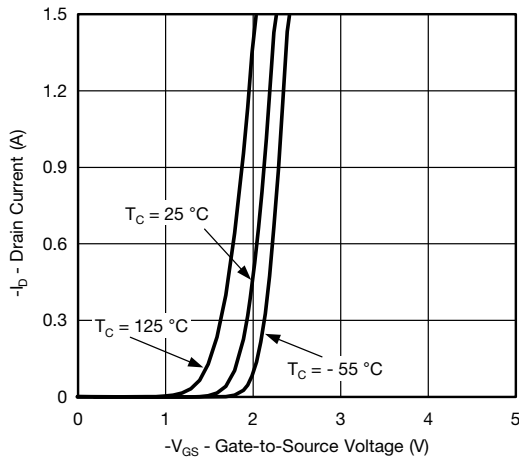
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



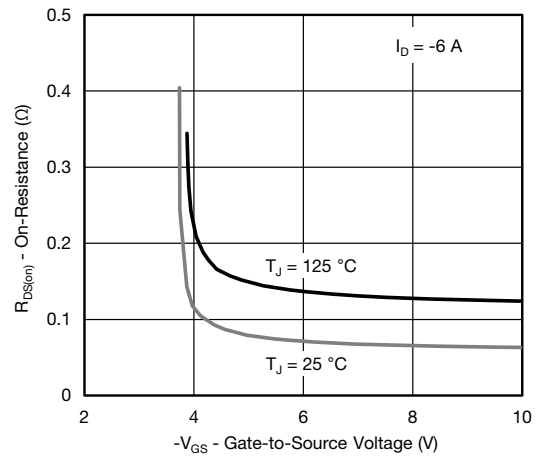
Output Characteristics



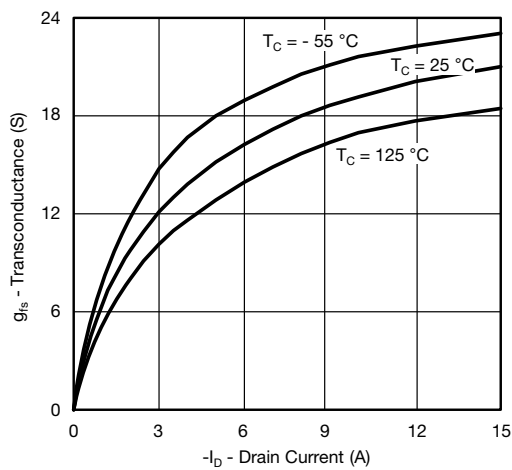
On-Resistance vs. Drain Current



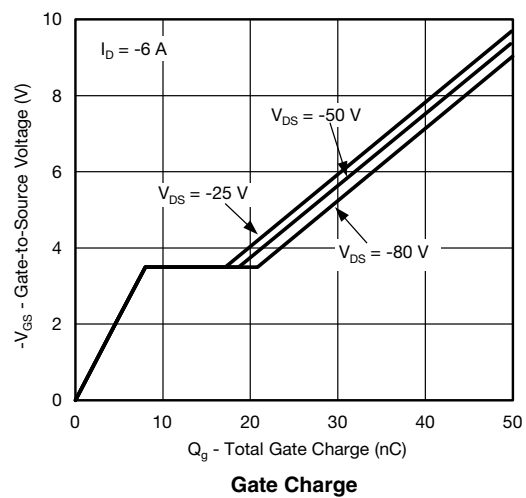
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

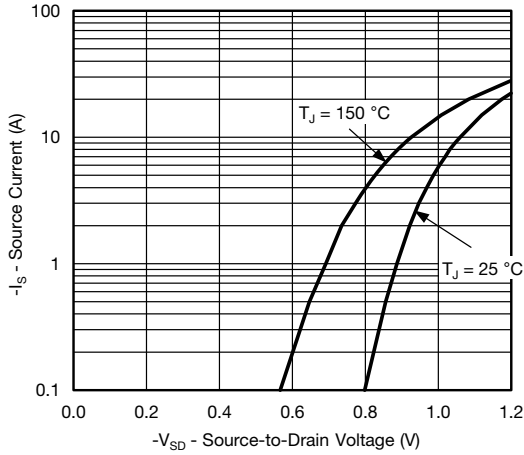


Transconductance

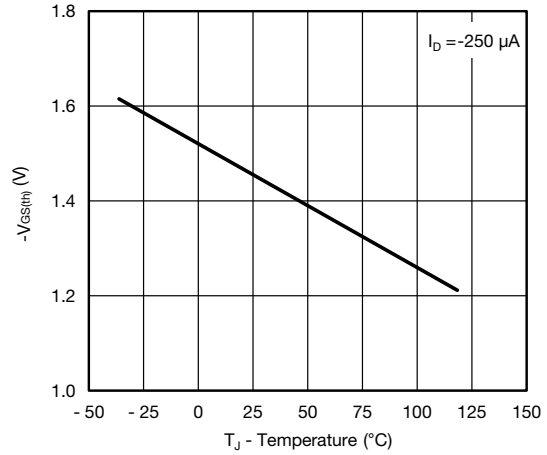


Gate Charge

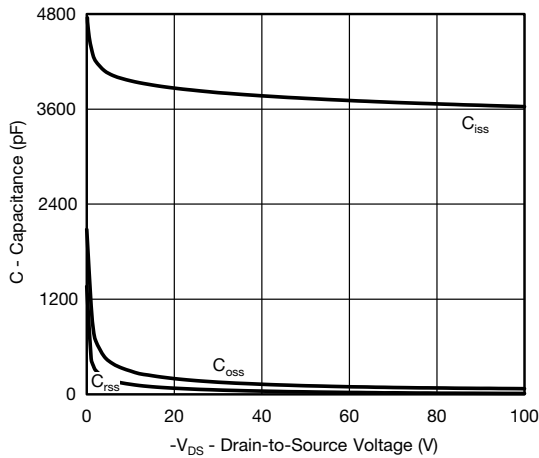
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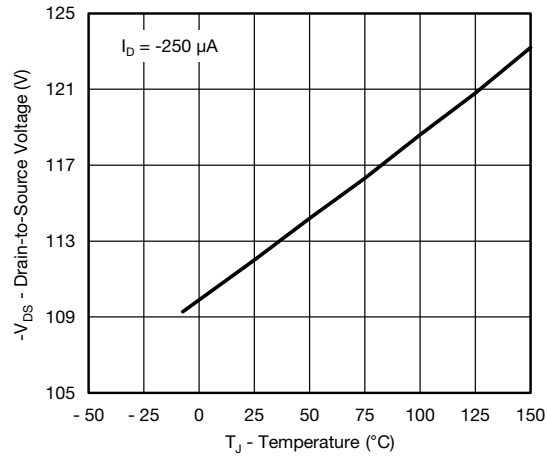
Source-Drain Diode Forward Voltage



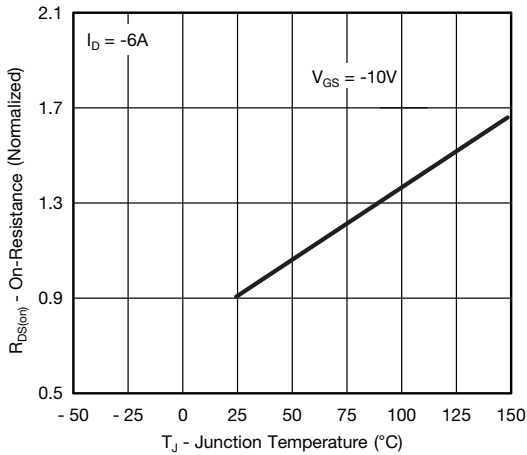
Threshold Voltage



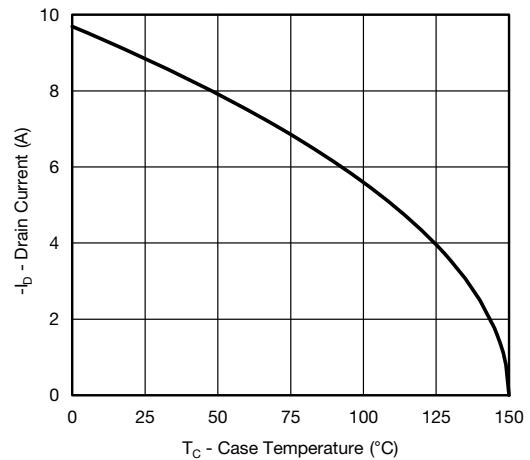
Capacitance



Drain Source Breakdown vs. Junction Temperature

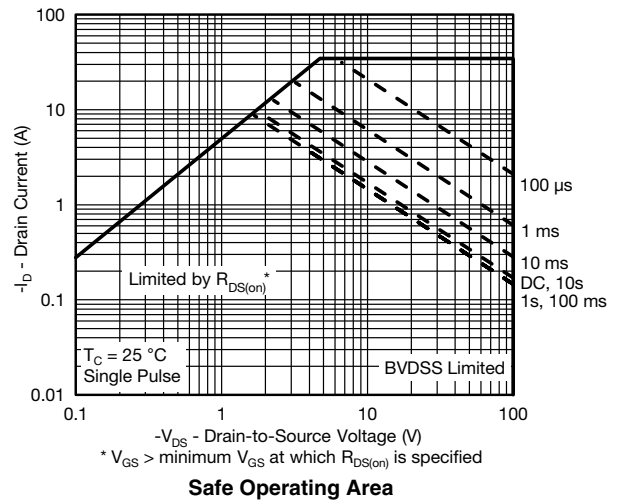
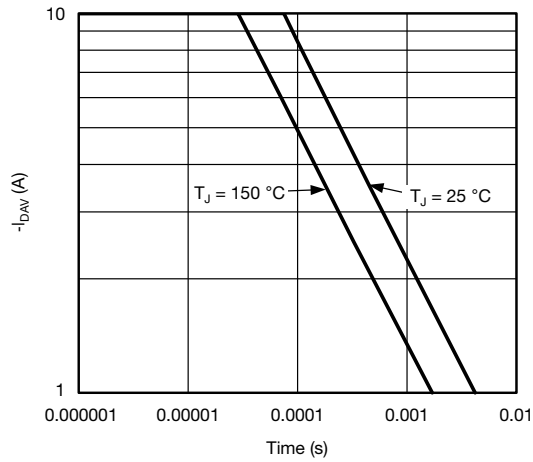


On-Resistance vs. Junction Temperature



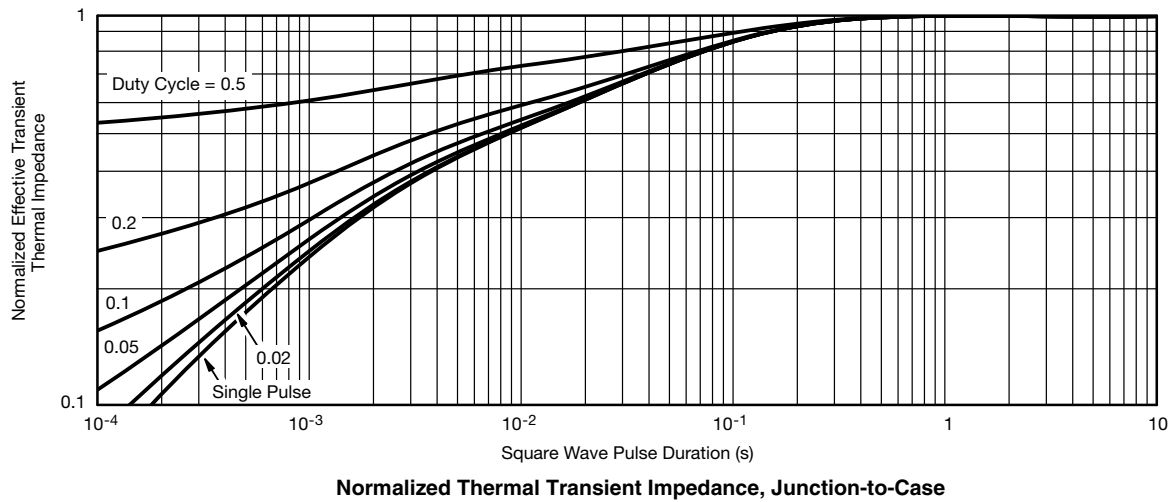
Current Derating

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



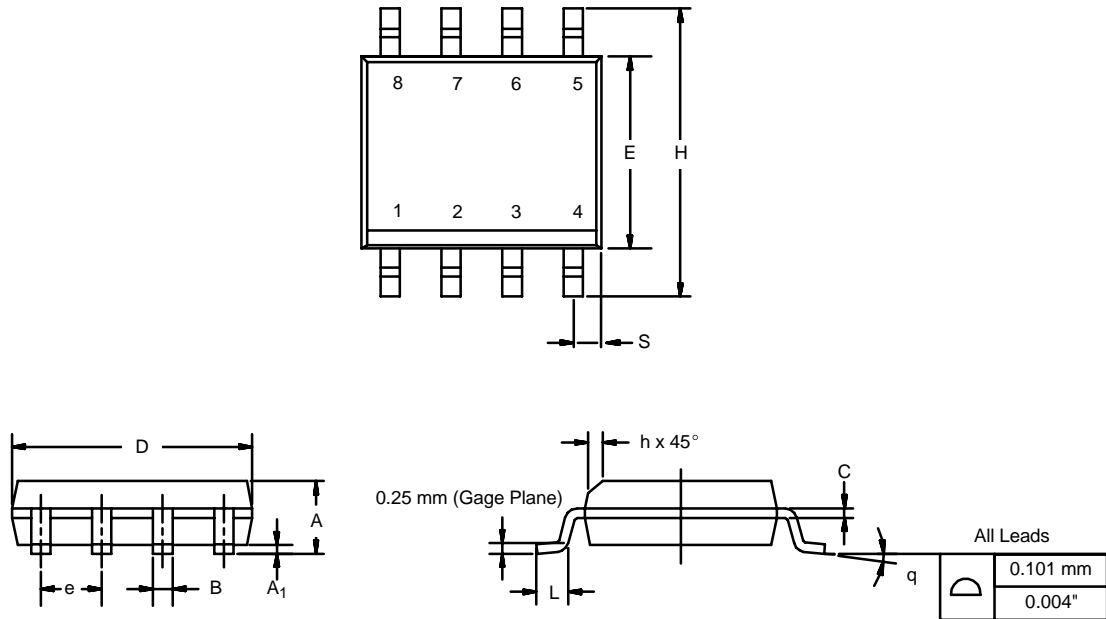
Single Pulse Avalanche Current Capability vs. Time

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

SOIC (NARROW): 8-LEAD



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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