

1200V N-Channel Silicon Carbide Power MOSFET

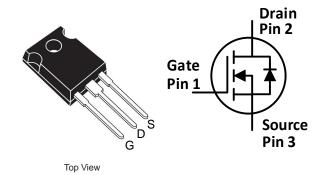
Features:

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode

Applications:

- Solar inverters
- UPS
- Motor drivers
- High voltage DC/DC converters
- Switch mode power supplies

Package:



Part Number	Package			
DTN19N120SC3	TO247-3			

Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note	
V _{DS}	Drain-Source voltage	1200	V	V _{GS} =0V, I _D =100μA		
V _{GS}	Gate-Source voltage	-5 to 20	V	Recommended maximum		
I _D	Drain current (continuous)	19	Α	V _{GS} =20V, T _C =25°C	Fig. 21	
ID		14	Α	V _{GS} =20V, T _C =100°C	Fig. 21	
I _{DM}	Drain current (pulsed)	48	Α	Pulse width limited by SOA	Fig. 24	
P _{TOT}	Total power dissipation	134	W	T _C =25°C	Fig. 22	
T_{stg}	Storage temperature range	-55 to 175	°C			
Tı	Operating junction temperature	-55 to 175	°C			
				Wave soldering only allowed		
T∟	Solder Temperature	260	°C	at leads, 1.6mm from case		
				for 10 s		

Thermal Data

Sy	Symbol Parameter		Value	Unit	Note
	$R_{\theta(J-C)}$	Thermal Resistance from Junction to Case	1.122	°C/W	Fig. 23

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Electrical Characteristics (Tc=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Тур.	Max.			
I _{DSS}	Zero gate voltage drain current		5	100	μΑ	V _{DS} =1200V, V _{GS} =0V	
I _{GSS}	Gate leakage current		1	<u>+</u> 100	nA	V _{DS} =0V, V _{GS} =-5~20V	
			2.9		V	V _{GS} =V _{DS} , I _D =1.9mA	
V_{TH}	Gate threshold voltage		1.9			$V_{GS}=V_{DS}, I_{D}=1.9 mA$ @ $T_{C}=175 ^{\circ} C$	Fig. 8, 9
D	Static drain-source on-		160	195	mΩ	V _{GS} =20V, I _D =10A @T _J =25°C	Fig. 4, 5, 6,
Ron	resistance		285		mΩ	V _{GS} =20V, I _D =10A @T _J =175°C	7
Ciss	Input capacitance		895		рF		
C_{oss}	Output capacitance		43		рF	V _{DS} =800V, V _{GS} =0V,	Fig. 16
C_{rss}	Reverse transfer capacitance		2		рF	f=1MHz, V _{AC} =25mV	
Eoss	Coss stored energy		4.2		μЈ	_	Fig. 17
Qg	Total gate charge		43		nC	\/ -000\/ -104	Fig. 18
Q_{gs}	Gate-source charge		9		nC	$V_{DS}=800V$, $I_{D}=10A$, $V_{GS}=-5$ to $20V$	
Q_{gd}	Gate-drain charge		19		nC	VGS=-3 tO 20V	
R_g	Gate input resistance		8.5		Ω	f=1MHz	
Eon	Turn-on switching energy		204		μЈ		
Eoff	Turn-off switching energy		34.4		μJ	V_{DS} =800V, I_{D} =10A,	
t _{d(on)}	Turn-on delay time		15.2			V_{GS} =-2 to 20V,	Fig. 19, 20
t r	Rise time		14.4		nc	$R_{G(ext)}=3.3\Omega$,	3, =1, =1
t _{d(off)}	Turn-off delay time		11.3		ns	L=450μH	
t _f	Fall time		13.1				

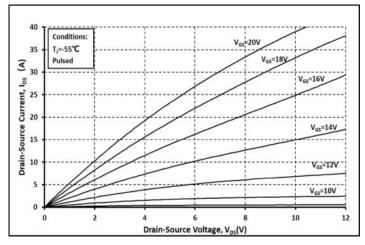


Reverse Diode Characteristics (T_c=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note	
		Min.	Тур.	Max.				
			4.1		V	I _{SD} =5A, V _{GS} =0V	Fig. 10,	
V_{SD}	Diode forward voltage		3.7		\/	I _{SD} =5A, V _{GS} =0V,	11g. 10, 11, 12	
			5.7		V	T _J =175°C	11, 12	
trr	Reverse recovery time		33.2		ns	$V_{GS} = -2V/+20V$,		
Qrr	Reverse recovery charge		101.5		nC	I _{SD} =10A, V _R =800V,		
Qrr	Reverse recovery charge		101.5		TIC	di/dt=1000A/us,		
I _{RRM}	Peak reverse recovery current		5.6		Α	$R_{G(ext)}=13\Omega$		



Typical Performance (curves)



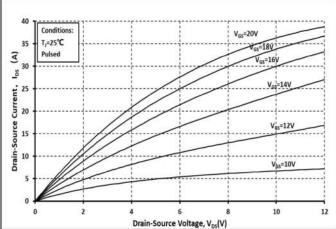
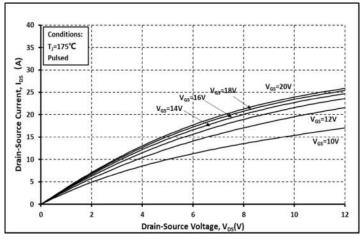


Fig. 1 Output Curve @ T₁=-55°C

Fig. 2 Output Curve @ T₁=25°C



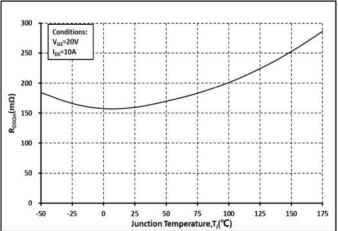
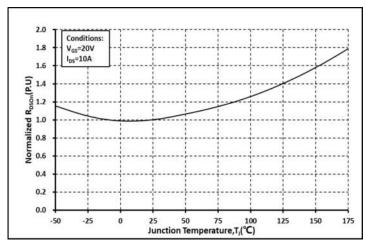


Fig. 3 Output Curve @ T,=175°C

Fig. 4 Ron vs. Temperature



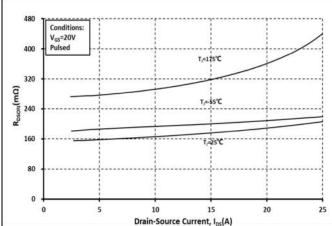
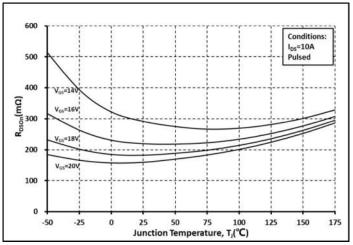


Fig. 5 Normalized Ron vs. Temperature

Fig. 6 Ron vs. IDS @ Various Temperature





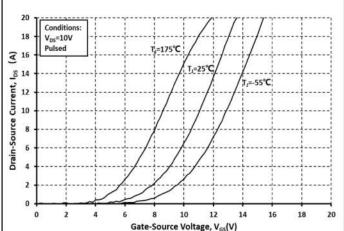
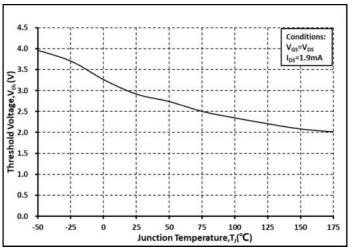


Fig. 7 Ron vs. Temperature @ Various V_{GS}

Fig. 8 Transfer Curves @ Various Temperature



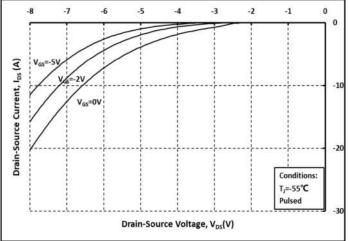
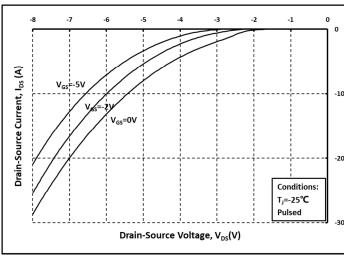


Fig. 9 Threshold Voltage vs. Temperature

Fig. 10 Body Diode Curves @ T₁=-55°C



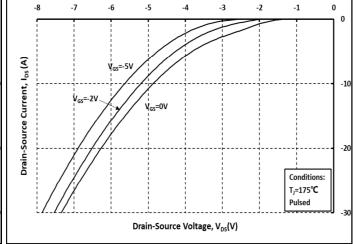
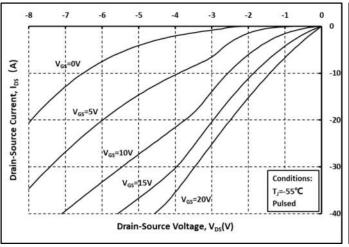


Fig. 11 Body Diode Curves @ T_J=25°C

Fig. 12 Body Diode Curves @ T₁=175°C





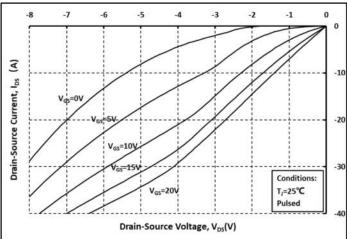
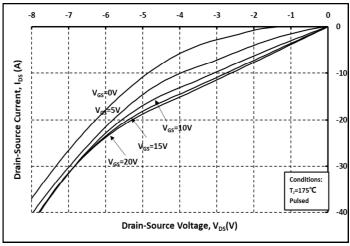


Fig. 13 3rd Quadrant Curves @ T_J=-55°C

Fig. 14 3rd Quadrant Curves @ T₁=25°C



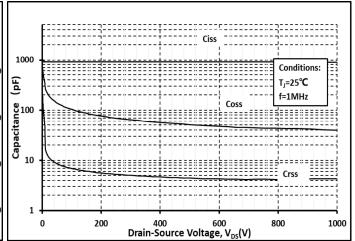
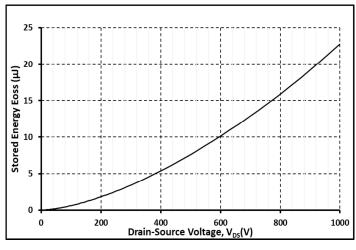


Fig. 15 3rd Quadrant Curves @ T₁=175°C

Fig. 16 Capacitance vs. V_{DS}



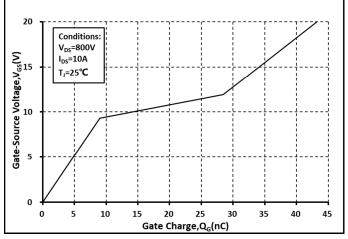
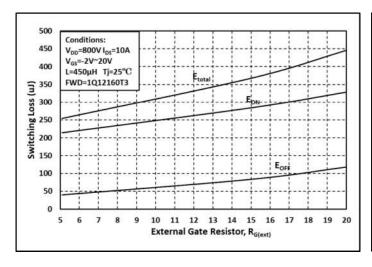


Fig. 17 Output Capacitor Stored Energy

Fig. 18 Gate Charge Characteristics





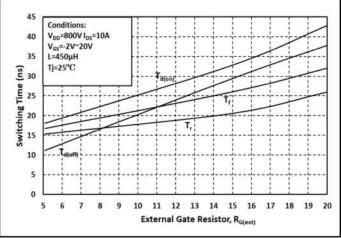
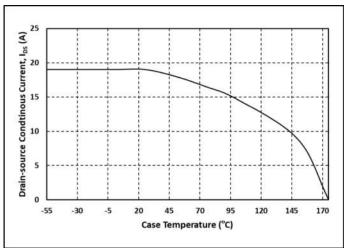
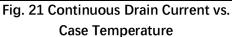


Fig. 19 Switching Energy vs. $R_{G(ext)}$

Fig. 20 Switching Times vs. R_{G(ext)}





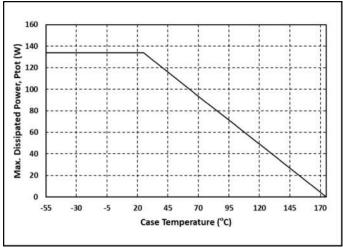


Fig. 22 Max. Power Dissipation Derating vs.

Case Temperature

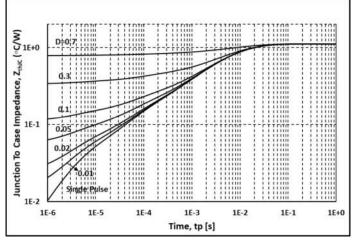


Fig. 23 Thermal Impedance

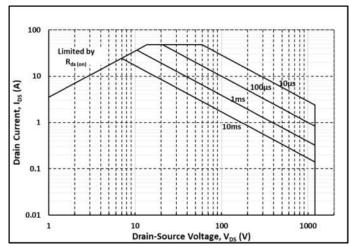
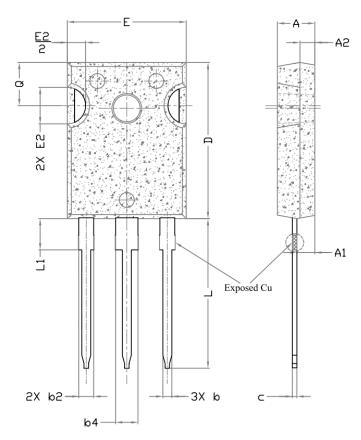


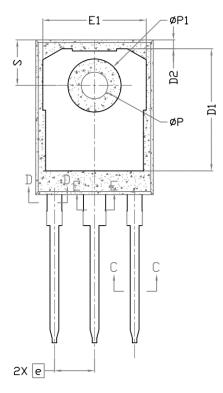
Fig. 24 Safe Operating Area

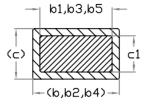


Package Dimensions



CYMPOL	С	NOTEC		
SYMBOL	MIN.	NOM.	MAX.	NOTES
Α	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
С	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
е				
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
ØP	3.56	3.61	3.65	7
ØP1				
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	





Section C--C,D--D,E-E

Note:

- 1. Package Reference: JEDEC TO247, Variation AD
- 2. All Dimensions are in mm
- 3. Slot Required, Notch May Be Rounded
- 4. Dimension D&E Do Not Include Mold Flash

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