

## C.Dual N-Channel 20-V (D-S) MOSFET



**RoHS**  
COMPLIANT

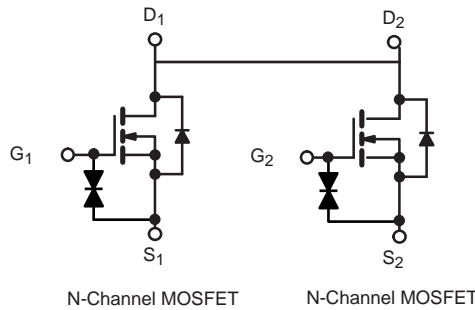
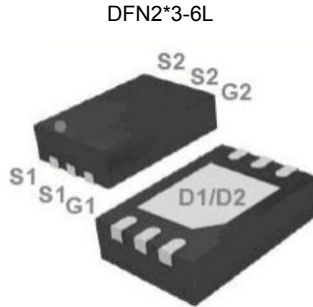
PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) MAX.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (TYP.)
20	0.0085 at V <sub>GS</sub> = 4.5V	25	14 nC
	0.012 at V <sub>GS</sub> = 2.5 V	22	

### FEATURES

- DT-Trench Power MOSFET
- 100 % R<sub>g</sub> and UIS tested
- ESD Protection Diode Embedded

### APPLICATIONS

- High power density DC/DC
- Synchronous rectification
- Embedded DC/DC



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	25
		T <sub>C</sub> = 70 °C	23
		T <sub>A</sub> = 25 °C	9.0 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	5.4 <sup>b, c</sup>
Pulsed Drain Current (t = 300 μs)	I <sub>DM</sub>	108	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	5.1 <sup>b, c</sup>
Single Pulse Avalanche Current	I <sub>AS</sub>	24	mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	10.3	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	24
		T <sub>C</sub> = 70 °C	15.3
		T <sub>A</sub> = 25 °C	3.1 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	1.9 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	R <sub>thJA</sub>	29	45	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	4	6	

### Notes

- Based on T<sub>C</sub> = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- The DFN3X3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

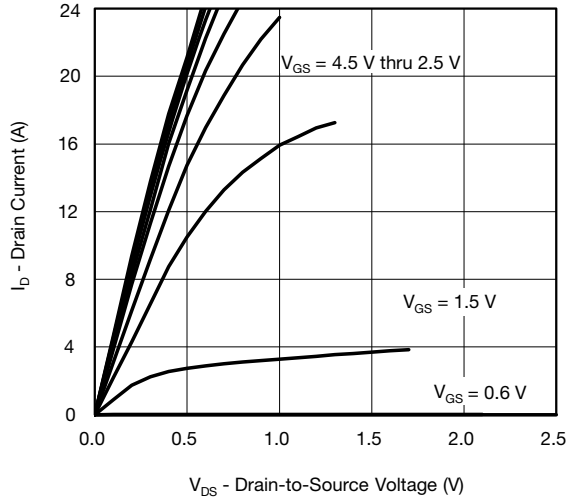
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20	-	-	V
Drain-Source Breakdown Voltage (transient) <sup>c</sup>	$V_{DS(t)}$	$V_{GS} = 0\text{ V}, I_{D(aval)} = 15\text{ A}, t_{\text{transient}} = 50\text{ ns}$	26	-	-	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	20	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-4.6	-	°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.5	-	1.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 12\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	25	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	0.0085	0.013	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 8\text{ A}$	-	0.012	0.018	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$	-	60	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	2050	-	$\mu\text{F}$
Output Capacitance	$C_{oss}$		-	210	-	
Reverse Transfer Capacitance	$C_{rss}$		-	33	-	
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	-	19	-	$\text{nC}$
		$V_{DS} = 10\text{ V}, V_{GS} = 2.5\text{ V}, I_D = 8\text{ A}$	-	10	-	
Gate-Source Charge	$Q_{gs}$		-	4	-	
Gate-Drain Charge	$Q_{gd}$		-	1.8	-	
Output Charge	$Q_{oss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$	-	12.5	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.4	1.60	3.3	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	-	9	18	$\text{ns}$
Rise Time	$t_r$		-	8	16	
Turn-Off Delay Time	$t_{d(off)}$		-	18	36	
Fall Time	$t_f$		-	8	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 8\text{ A}, V_{GEN} = 2.5\text{ V}, R_g = 1\text{ }\Omega$	-	15	30	
Rise Time	$t_r$		-	12	24	
Turn-Off Delay Time	$t_{d(off)}$		-	18	36	
Fall Time	$t_f$		-	9	18	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	25	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	108	
Body Diode Voltage	$V_{SD}$	$I_S = 3\text{ A}$	-	0.70	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	24	48	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	14	28	nC
Reverse Recovery Fall Time	$t_a$		-	12	-	ns
Reverse Recovery Rise Time	$t_b$		-	12	-	

**Notes**

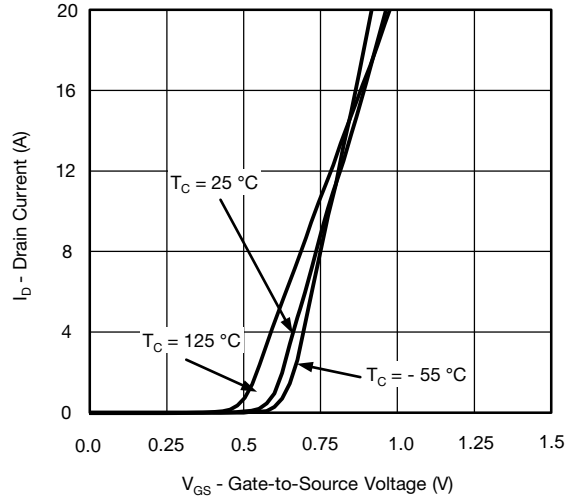
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c.  $T_{CASE} = 25\text{ }^\circ\text{C}$ . Expected voltage stress during 100% UIS test. Production datalog is not available.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

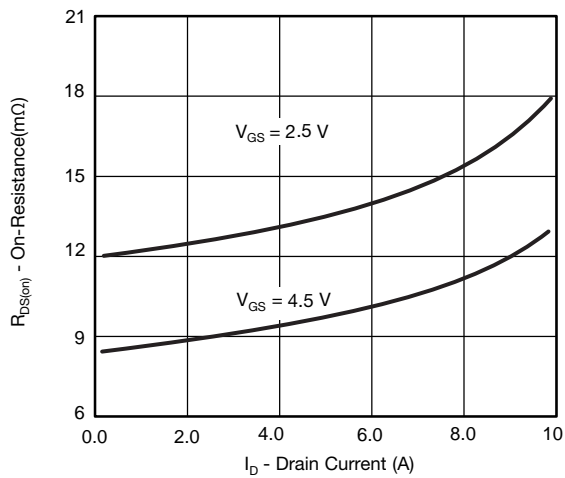
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



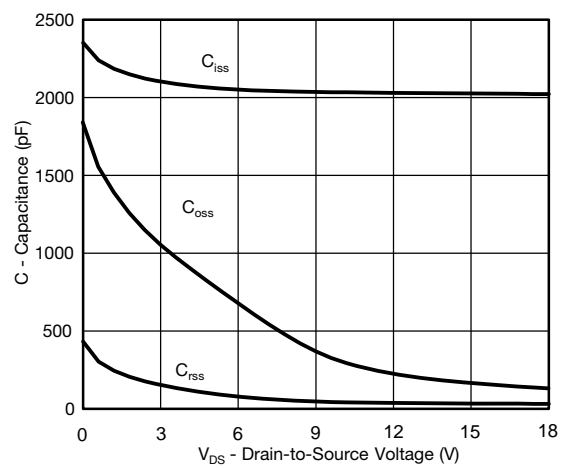
**Output Characteristics**



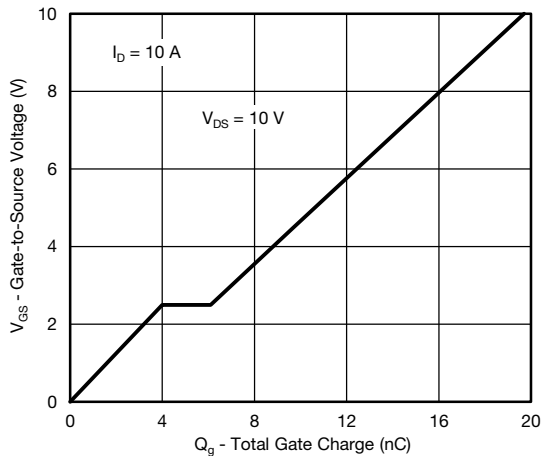
**Transfer Characteristics**



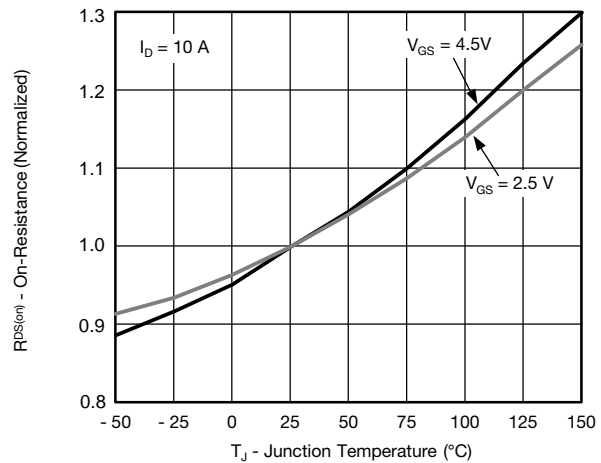
**On-Resistance vs. Drain Current**



**Capacitance**

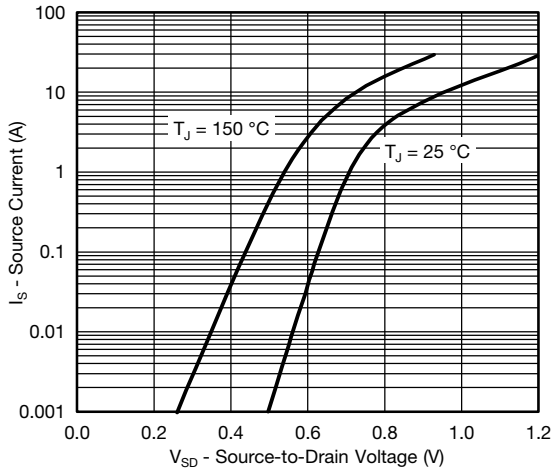


**Gate Charge**

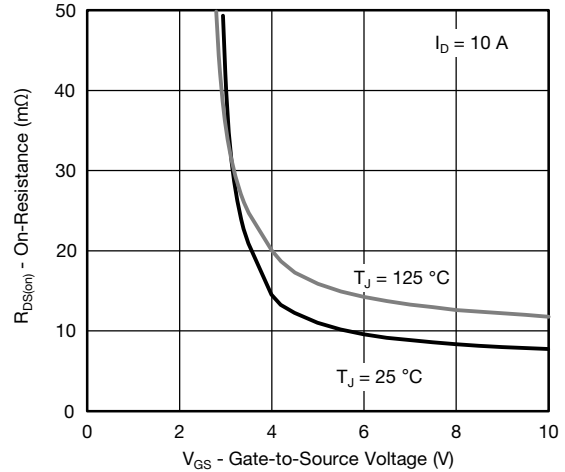


**On-Resistance vs. Junction Temperature**

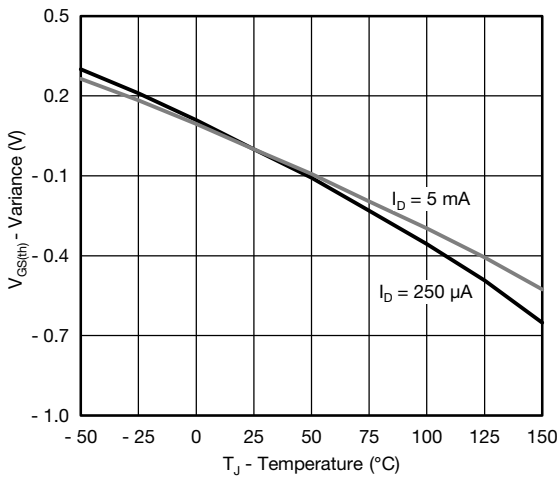
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



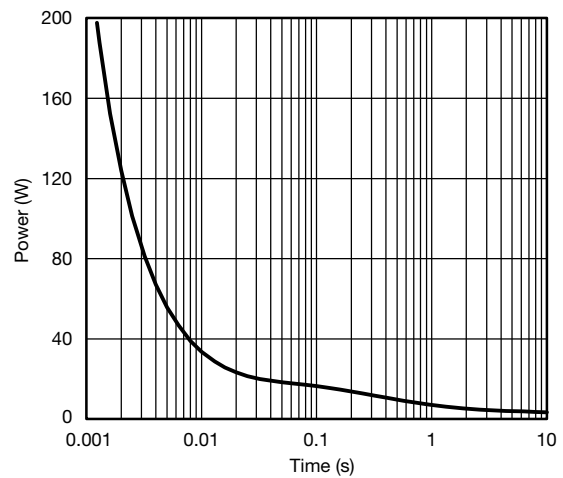
**Source-Drain Diode Forward Voltage**



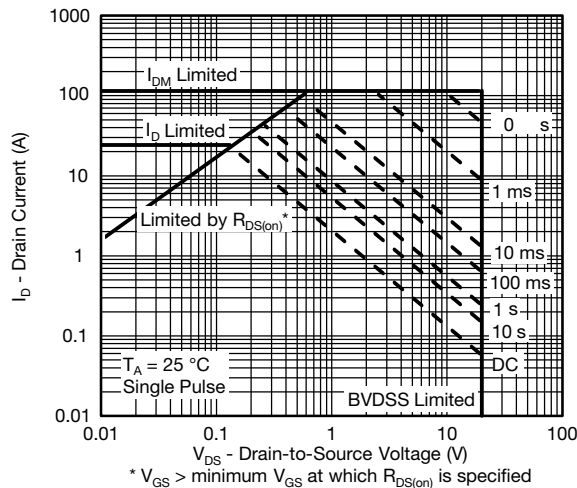
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**

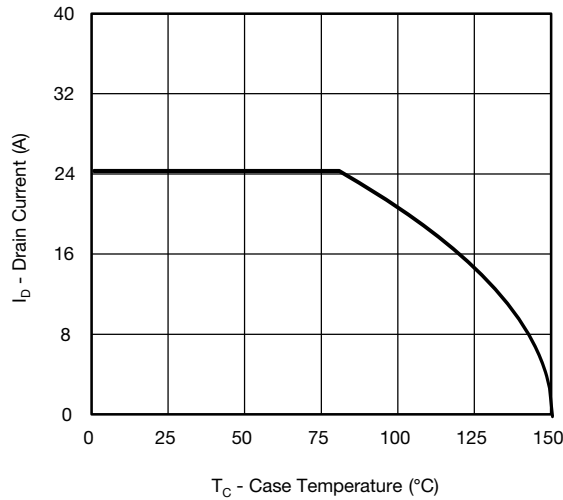


**Single Pulse Power, Junction-to-Ambient**

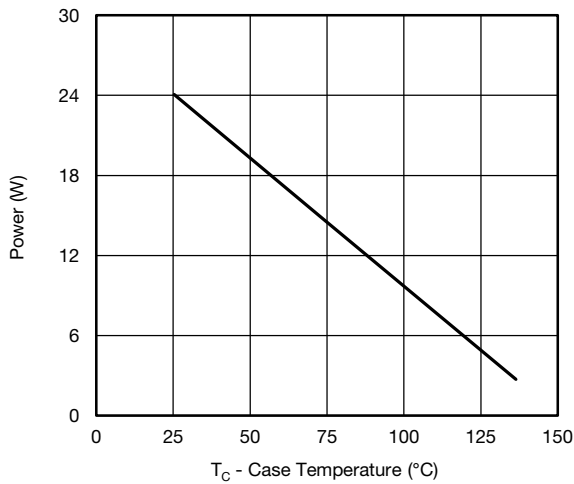


**Safe Operating Area**

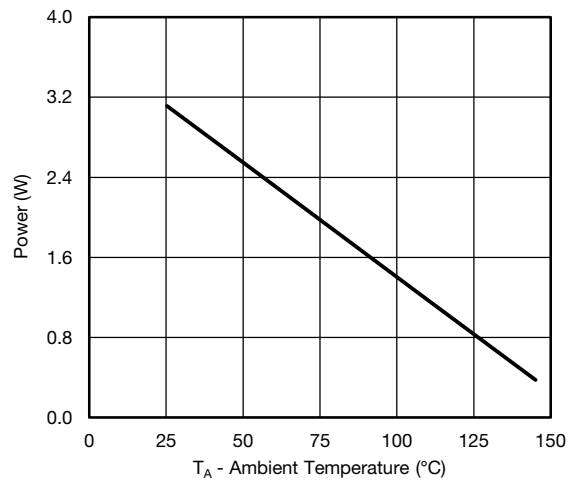
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



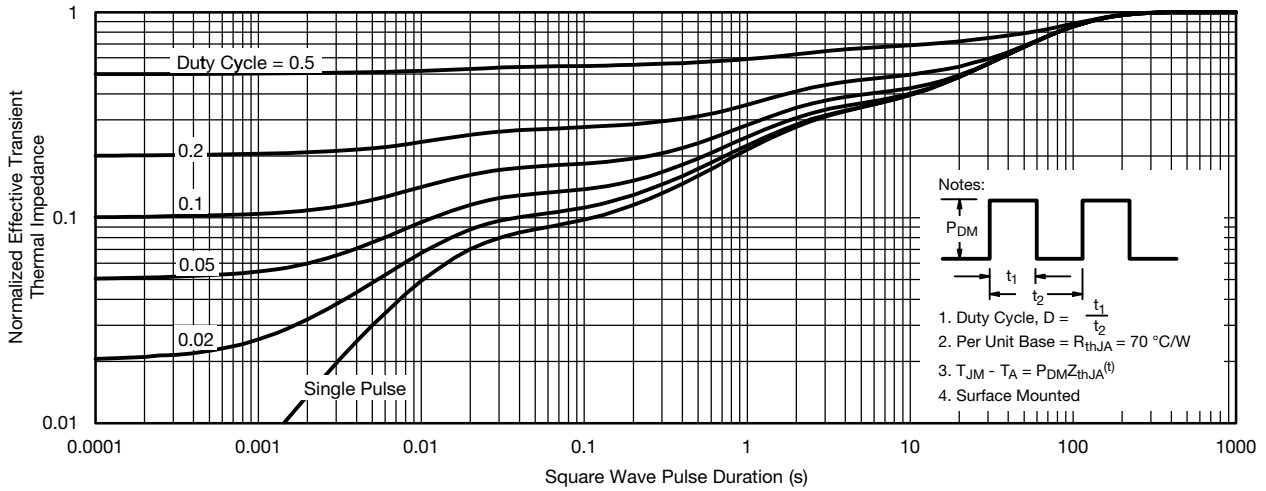
**Power, Junction-to-Case**



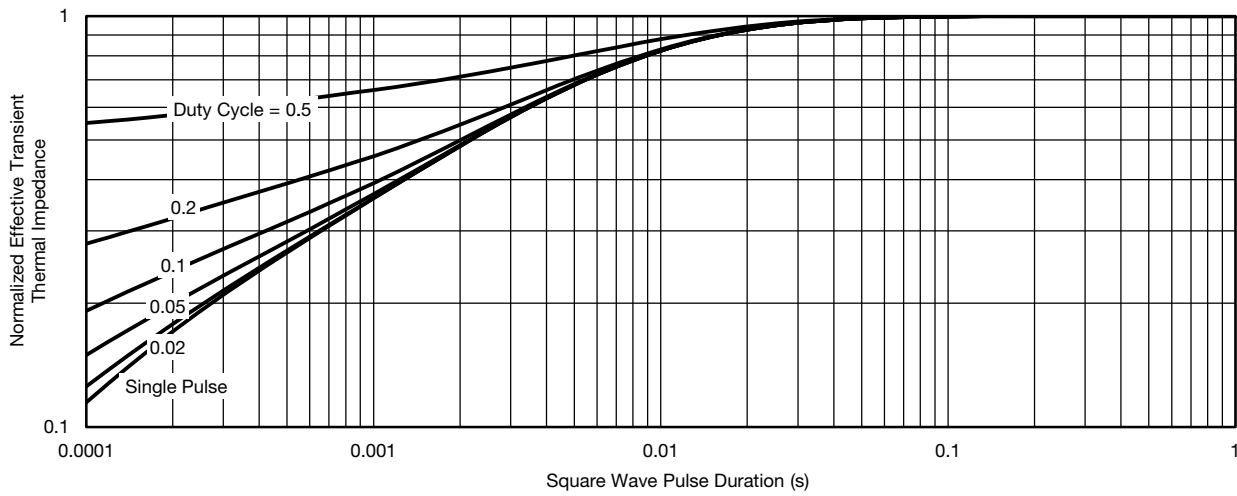
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

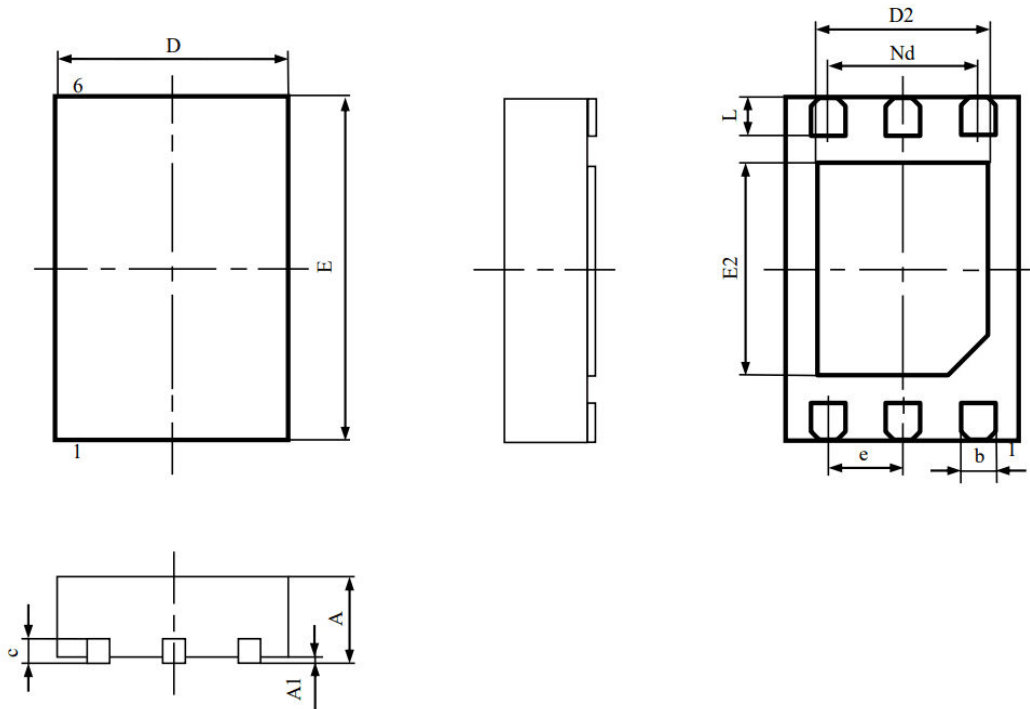


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

### DFN2X3 PACKAGE INFORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	0.800	0.700	0.031	0.028
A1	0.050	0.02typ.	0.002	0.001typ.
b	0.350	0.200	0.014	0.008
c	0.250	0.180	0.010	0.007
D	2.100	1.900	0.083	0.075
D2	1.600	1.400	0.063	0.055
e	0.5BSC		0.02BSC	
Nd	1.0BSC		0.04BSC	
E	3.100	2.900	0.122	0.114
E2	1.750	1.650	0.069	0.065
L	0.400	0.300	0.016	0.012

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