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P-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)		
-40	0.011 at V _{GS} = -10 V	-48		
	0.016 at V _{GS} = -4.5 V	-40		

FEATURES

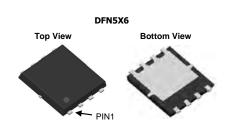
- DT-Trench Power MOSFET
- 100 % R_g and UIS Tested

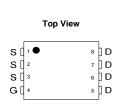
APPLICATIONS

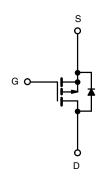
- Notebook
 - Load Switch



RoHS







P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	Limit	UNIT	
Drain-Source Voltage		V_{DS}	- 40	V	
Gate-Source Voltage		V_{GS}	± 20	7 v	
O	T _A = 25 °C	_	- 48		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C	I _D	- 35	7	
Pulsed Drain Current		I _{DM}	- 190	Α	
Continuous Source Current (Diode Conduction) ^a		I _S	- 48		
Avalanche Current	L = 0.1 mH	I _{AS}	- 35		
Single Pulse Avalanche Energy	L = 0.1 IIII	E _{AS}	113	mJ	
Maximum Power Dissipation ^a	T _A = 25 °C	D	39	w	
iviaximum rower Dissipation "	T _A = 70 °C	P _D	25	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) b, c			260		

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	20	25		
waximum Junction-to-Ambient ~	Steady State		25	35	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.1	3.3		

Notes

- a. Surface mounted on 1" x 1" FR4 board.
- b. TheDFN5x6isa leadlesspackage. The endof thelead terminalisexposed copper (not plated) as a result of the singulation process in manufacturing. A solderfillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				_		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$ -1 -			-3	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
Zava Cata Valtaga Dvain Couvent		V _{DS} = -32 V, V _{GS} = 0 V	$V_{DS} = -32 \text{ V}, V_{GS} = 0 \text{ V}$ -		-1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -32 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-10	μA
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	-60	-	-	Α
Dunin Course On State Projetones 3	В	$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	-	0.011	0.014	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -3 A	-	0.016	0.022	
Forward Transconductance ^a	9 _{fs}	V _{DS} = -15 V, I _D = -5 A	-	35	-	S
Diode Forward Voltage ^a	V_{SD}	I _S = -4.5 A, V _{GS} = 0 V	-	-0.7	-1.2	V
Dynamic ^b						
Input Capacitance	C _{iss}	$V_{GS} = 0 V$	-	2120	-	pF
Output Capacitance	C _{oss}	$V_{DS} = 100 \text{ V},$	-	230	-	
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz	-	180	-	
Total Gate Charge	Qg		-	121	-	
Gate-Source Charge	Q _{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	-	20	-	nC
Gate-Drain Charge	Q _{gd}		-	32	-	
Gate Resistance	R_g		-	1.5	-	Ω
Turn-On Delay Time	t _{d(on)}		_	21	-	
Rise Time	t _r	V_{DD} = -20 V, R_L = 30 Ω	-	20	-	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ -5 A, $V_{GEN}=$ -10 V, $R_g=6~\Omega$	-	55	-	ns
Fall Time	t _f		-	12	-	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -4.5 A, dI/dt = 100 A/μs	-	29	50	

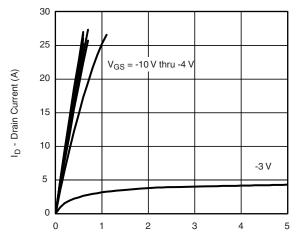
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

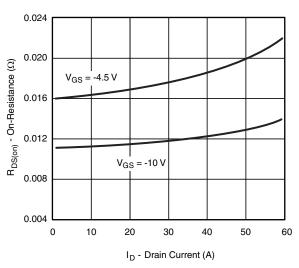


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

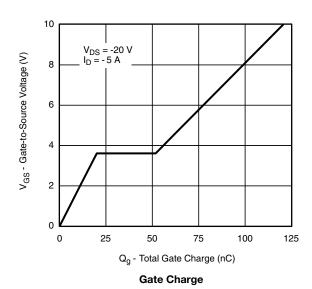


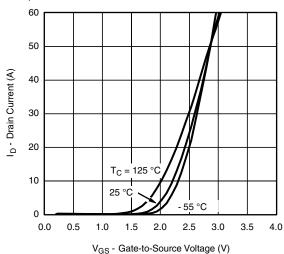
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics

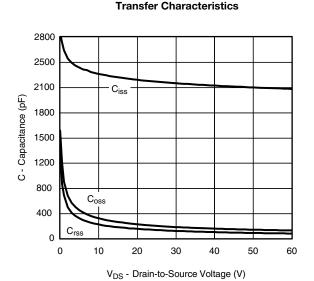


On-Resistance vs. Drain Current

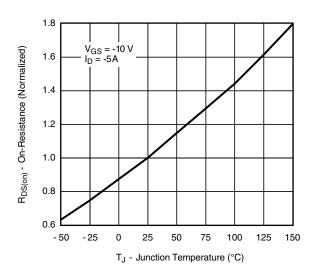




vas date to ocureo vertage (v)



Capacitance

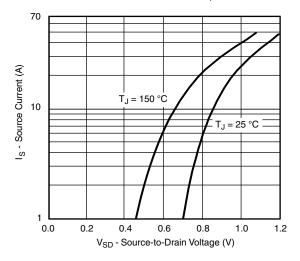


On-Resistance vs. Junction Temperature

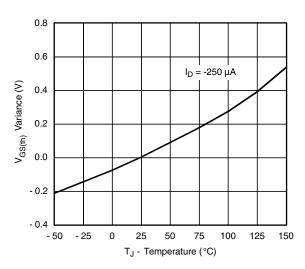




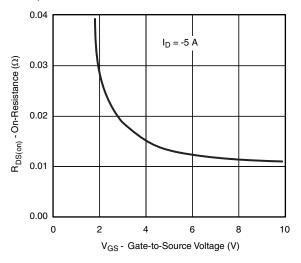
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



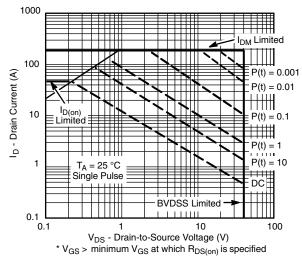
Source-Drain Diode Forward Voltage



Threshold Voltage



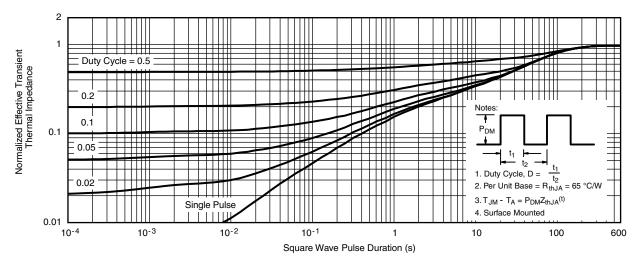
On-Resistance vs. Gate-to-Source Voltage



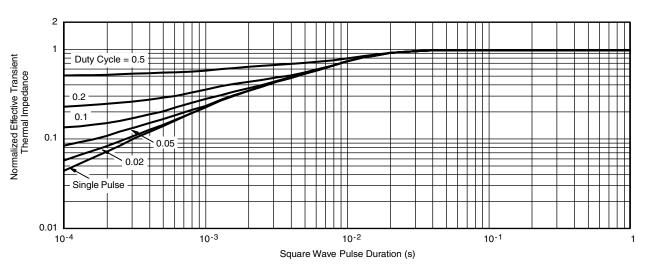
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



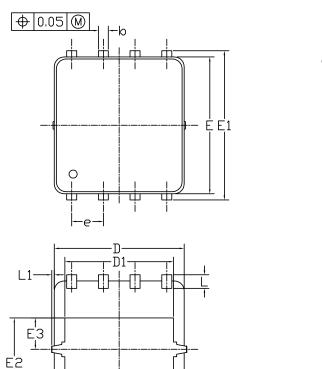
Normalized Thermal Transient Impedance, Junction-to-Ambient

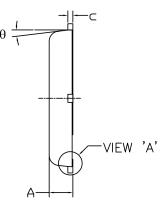


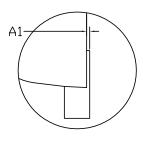
Normalized Thermal Transient Impedance, Junction-to-Case



DFN5x6_8L_EP1_P PACKAGE OUTLIN

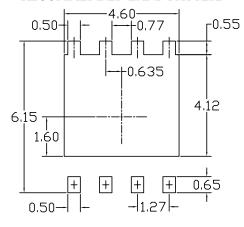






<u>VIEW 'A'</u> (SCALE 5:1)

RECOMMENDED LAND PATTERN



GVA (DOLG	SYMBOLS DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
31 MBOL3	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0. 95	1.00	0.033	0.037	0.039
Al	0.00		0.05	0.000		0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0. 15	0. 20	0. 25	0.006	0.008	0.010
D	4. 80	5. 20	5. 30	0. 201	0. 205	0. 209
D1	4. 25	4. 35	4. 45	0. 167	0. 171	0. 175
Е	5. 45	5. 55	5. 65	0. 215	0.219	0. 222
E1	5. 95	6.05	6. 15	0. 234	0. 238	0. 242
E2	3. 525	3.625	3. 725	0.139	0. 143	0. 147
E3	1. 175	1. 275	1.375	0.046	0.050	0.054
e	1. 27 BSC			0.050 BSC		
L	0.45	0. 55	0.65	0.018	0.022	0.026
L1	0		0. 15	0		0.006
L2	0.68 REF			0.027 REF		
θ	0°		10°	0°		10°

NOTE

- UNIT: mm
- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
- 2. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

BOTTOM VIEW





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