NIKO-SEM

Dual P-Channel Enhancement Mode Field Effect Transistor

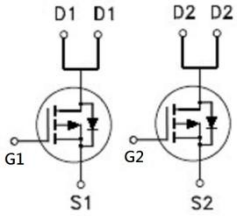
PV561DA

SOP-8

Halogen-free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	45mΩ	-5.2A



Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

G : GATE
D : DRAIN
S : SOURCE

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.

100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	-5.2	A
	T_A = 70 °C		-4.1	
Pulsed Drain Current[1]		I_{DM}	-20	
Avalanche Current		I_{AS}	-14	
Avalanche Energy	L = 0.1mH	E_{AS}	9.8	mJ
Power Dissipation[3]	T_A = 25 °C	P_D	2	W
	T_A = 70 °C		1.3	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$		60	°C / W
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$		92	
Junction-to-Case	Steady-State	$R_{\theta JC}$		40	

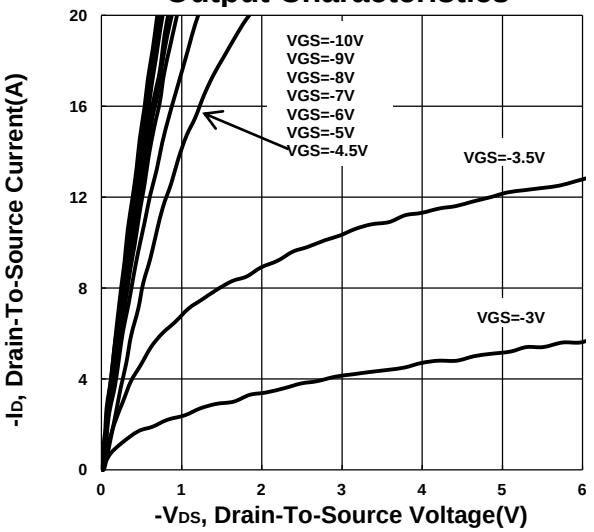
[1]Pulse width limited by maximum junction temperature.
[2] The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

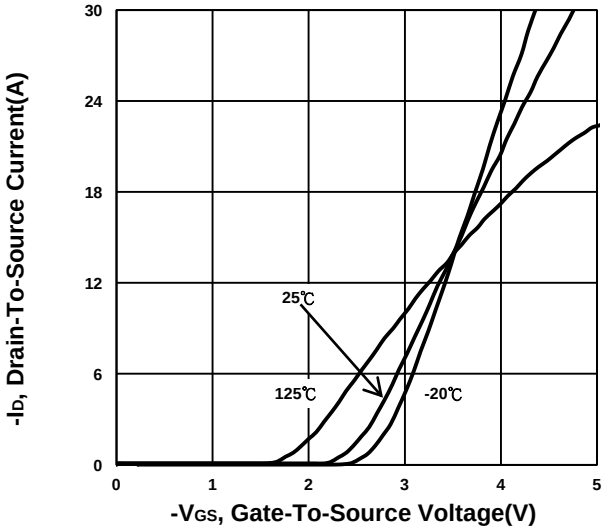
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.3	-1.75	-2.3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 55 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -5A		55	75	mΩ
		V_{GS} = -10V, I_D = -5A		33	45	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -5A		13		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		502		pF
Output Capacitance	C_{oss}			83		
Reverse Transfer Capacitance	C_{rss}			63		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		14.7		Ω
Total Gate Charge[2]	Q_g	V_{DS} = -15V , V_{GS} = -10V, I_D = -5A		10.5		nC
Gate-Source Charge[2]	Q_{gs}			1.7		
Gate-Drain Charge[2]	Q_{gd}			2.6		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = -15V $I_D \cong$ -5A, V_{GS} = -10V, R_{GEN} = 6Ω		11		nS
Rise Time[2]	t_r			33		
Turn-Off Delay Time[2]	$t_{d(off)}$			55		
Fall Time[2]	t_f			44		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-2	A
Forward Voltage[1]	V_{SD}	I_F = -5A, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -5A, dI/dt=100A/μs		10		nS
Reverse Recovery Charge	Q_{rr}			3		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

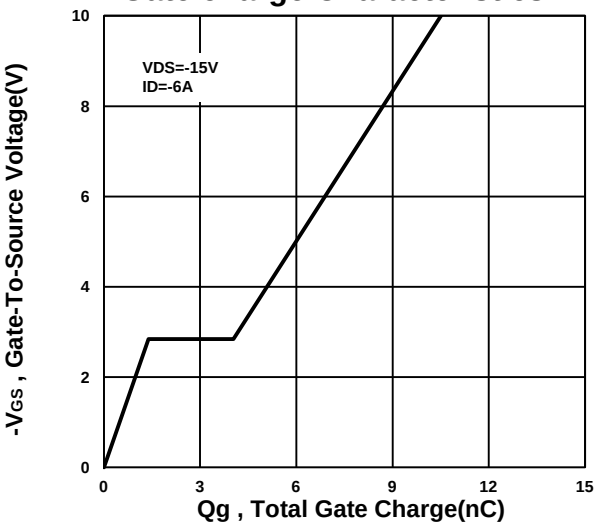
Output Characteristics



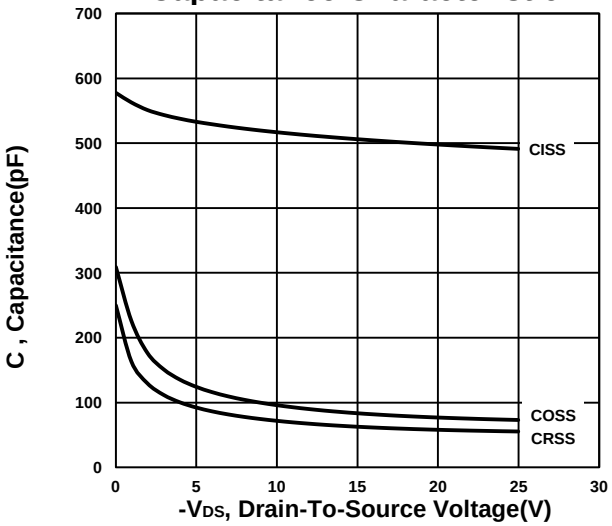
Transfer Characteristics



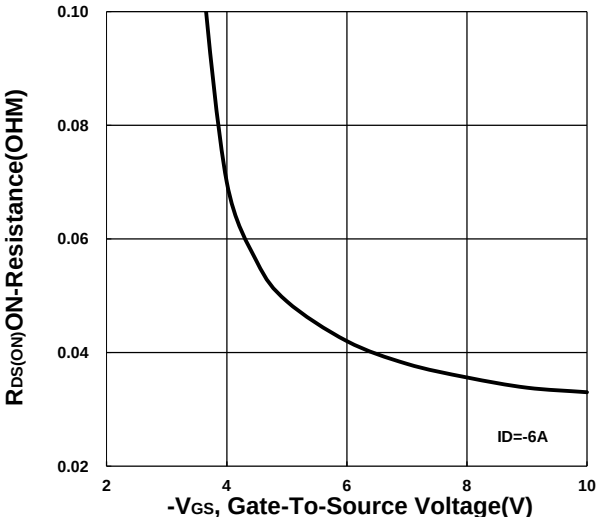
Gate charge Characteristics



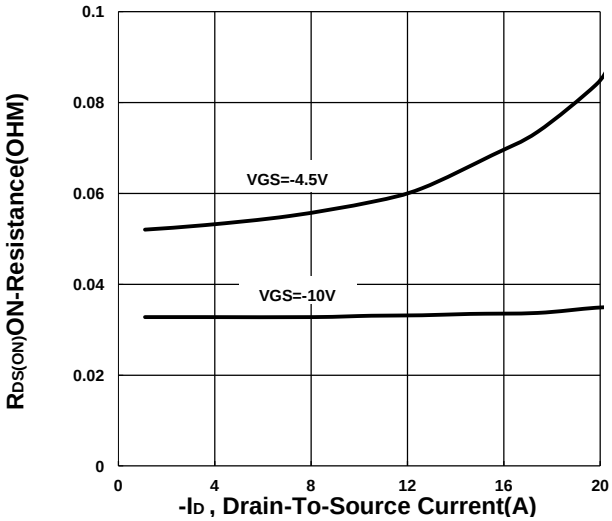
Capacitance Characteristic



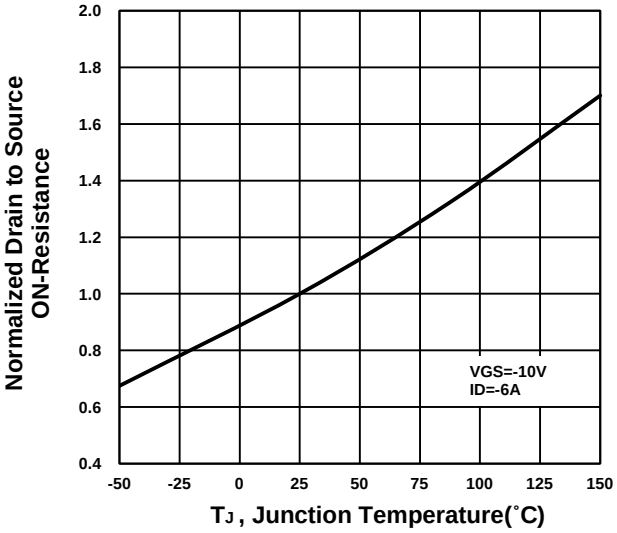
On-Resistance VS Gate-To-Source



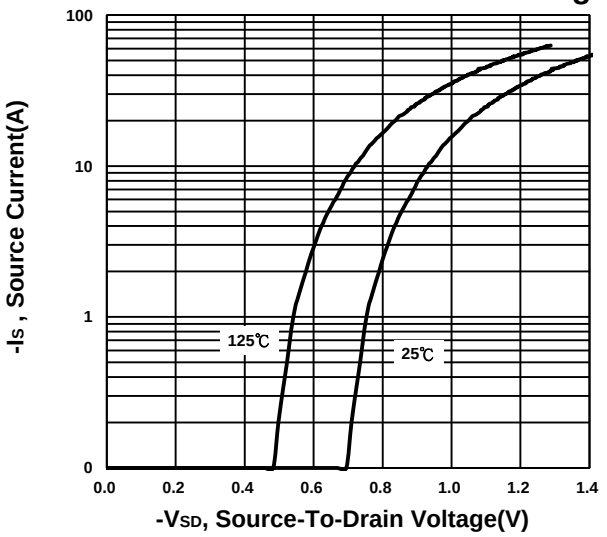
On-Resistance VS Drain Current



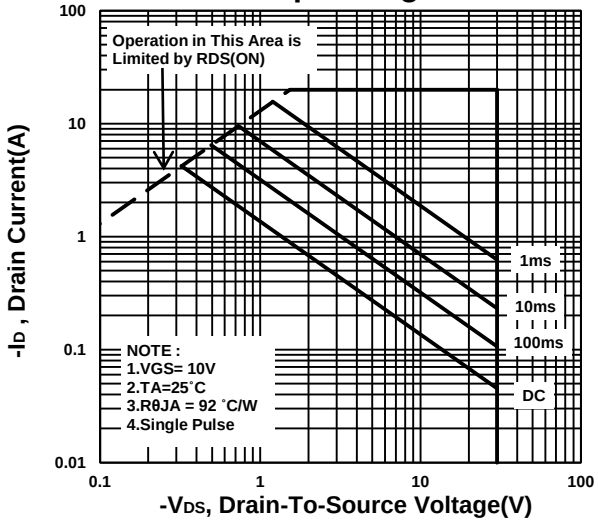
On-Resistance VS Temperature



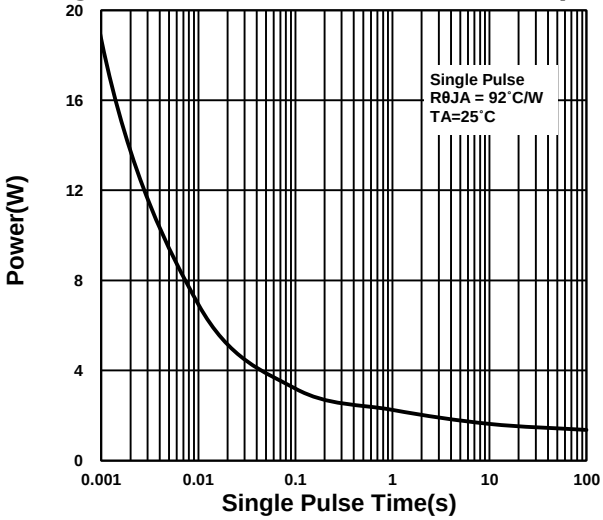
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve