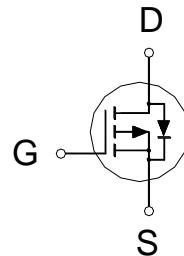


**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
Field Effect Transistor****PE597BA  
PDFN 3x3P  
Halogen-free & Lead-Free****PRODUCT SUMMARY**

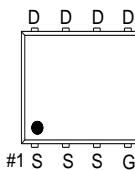
$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$
-20V	35mΩ	-17A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low  $R_{DS(on)}$  to Minimize Conduction Losses.
- Ohmic Region Good  $R_{DS(on)}$  Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

**Applications**

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G. GATE  
D. DRAIN  
S. SOURCE

100% UIS Tested  
100% Rg Tested

**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current <sup>4</sup>	$I_D$	-17	A
		-11	
		-7	
		-6	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-28	
Avalanche Current	$I_{AS}$	-14	
Avalanche Energy	$E_{AS}$	10	mJ
Power Dissipation <sup>3</sup>	$P_D$	16	W
		6	
		3	
		2	
Junction & Storage Temperature Range	$T_j, T_{stg}$	-55 to 150	°C

**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
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THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$t \leq 10s$	$R_{\theta JA}$		40	°C / W
Junction-to-Ambient <sup>2</sup>	Steady-State	$R_{\theta JA}$		75	
Junction-to-Case	Steady-State	$R_{\theta JC}$		8	

<sup>1</sup>Pulse width limited by maximum junction temperature.<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ C$ .<sup>3</sup>The Power dissipation is based on  $R_{\theta JA} t \leq 10s$  value.<sup>4</sup>Package limitation current is 36A.**ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ C$ , Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.7	-0.8	-1.3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 12V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16V, V_{GS} = 0V$			-1	$\mu A$
		$V_{DS} = -10V, V_{GS} = 0V, T_J = 55^\circ C$			-10	
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(\text{ON})}$	$V_{GS} = -4.5V, I_D = -3.5A$		22	35	$m\Omega$
		$V_{GS} = -2.5V, I_D = -3.5A$		32	55	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -3.5A$		16		S
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		767		$pF$
Output Capacitance	$C_{oss}$			117		
Reverse Transfer Capacitance	$C_{rss}$			93		
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		13		$\Omega$
Total Gate Charge <sup>2</sup>	$Q_{g(VGS=-4.5V)}$	$V_{DS} = -10V, I_D = -3.5A$		8.8		$nC$
	$Q_{g(VGS=-2.5V)}$			5.5		
Gate-Source Charge <sup>2</sup>	$Q_{gs}$			1		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$			2.6		

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Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	$V_{DD} = -10V$ $I_D \approx -3.5A, V_{GS} = -4.5V, R_{GEN} = 6\Omega$	19			nS
Rise Time <sup>2</sup>	$t_r$		30			
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$		55			
Fall Time <sup>2</sup>	$t_f$		20			
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_J = 25^\circ C</math>)</b>						
Continuous Current	$I_S$	$I_F = -3.5A, V_{GS} = 0V$ $I_F = -3.5A, dI/dt = 100A/\mu s$			-1	A
Forward Voltage <sup>1</sup>	$V_{SD}$				-1.3	V
Reverse Recovery Time	$t_{rr}$		9.5			nS
Reverse Recovery Charge	$Q_{rr}$		3			nC

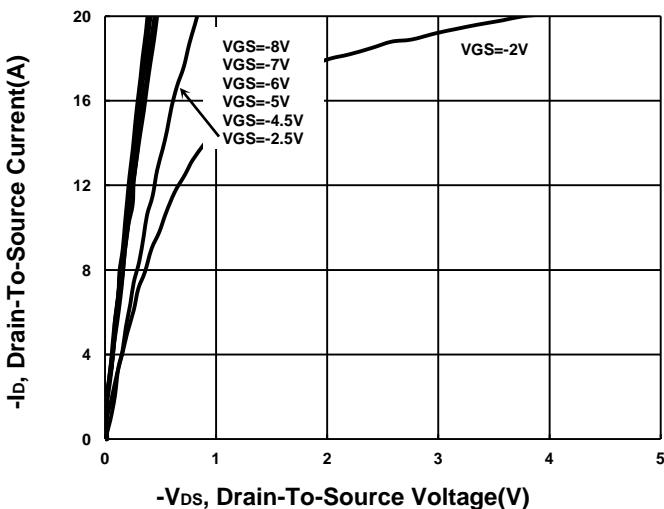
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .<sup>2</sup>Independent of operating temperature.

**NIKO-SEM**

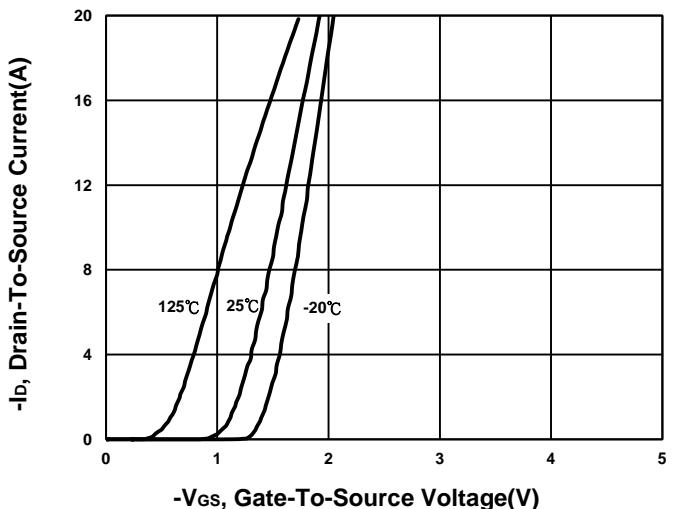
**P-Channel Logic Level Enhancement Mode  
Field Effect Transistor**

**PE597BA  
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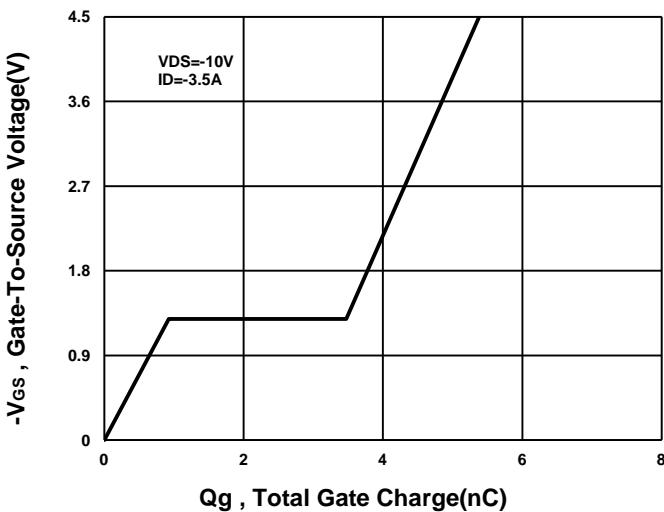
### Output Characteristics



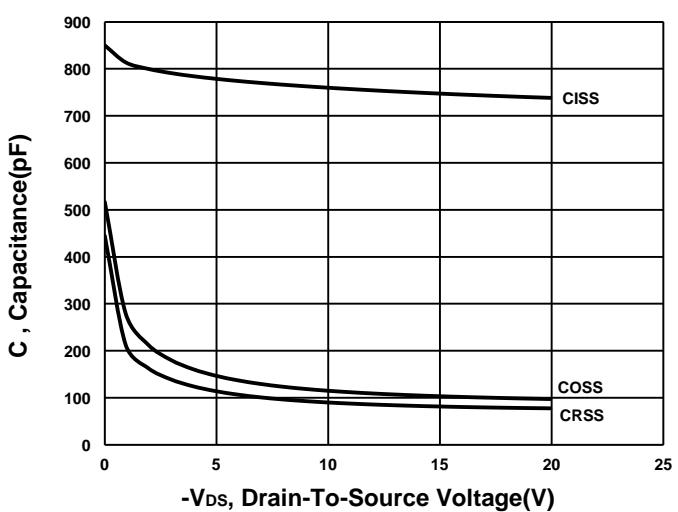
### Transfer Characteristics



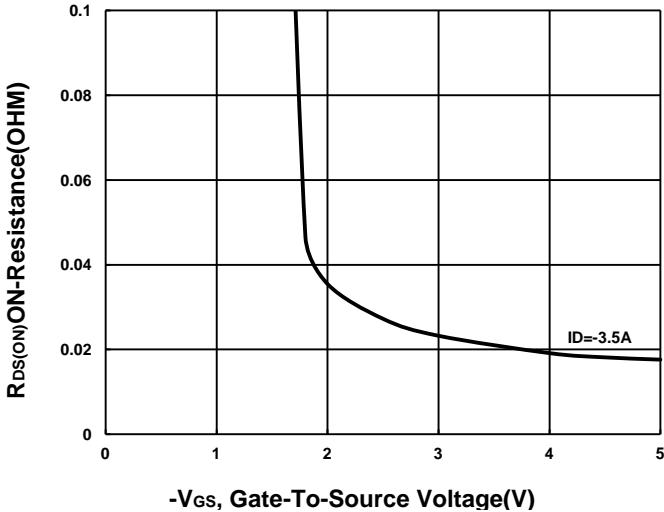
### Gate charge Characteristics



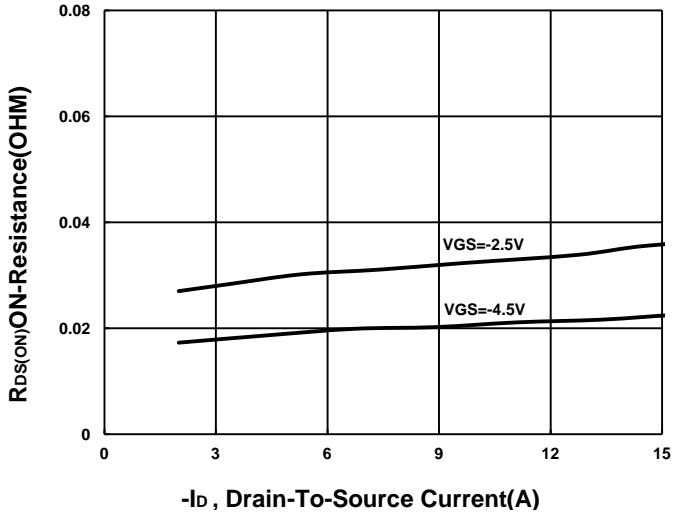
### Capacitance Characteristic

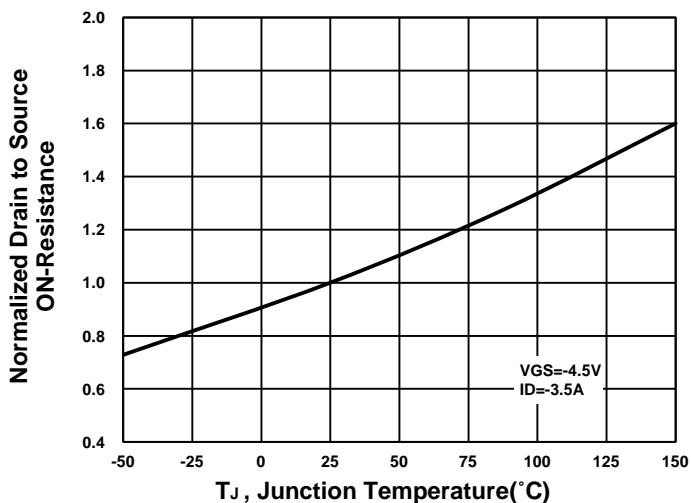
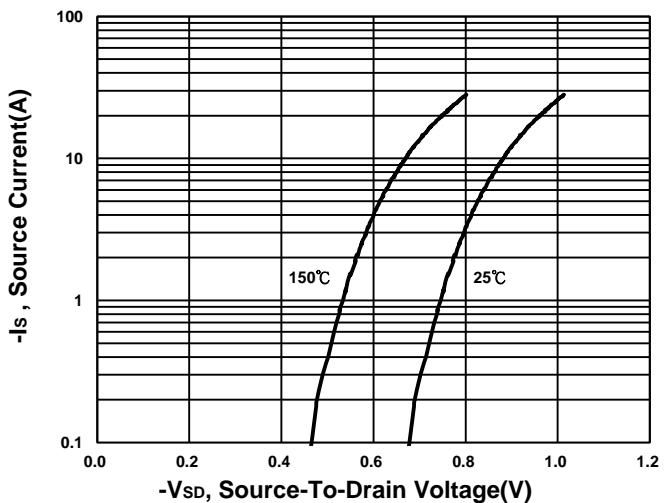
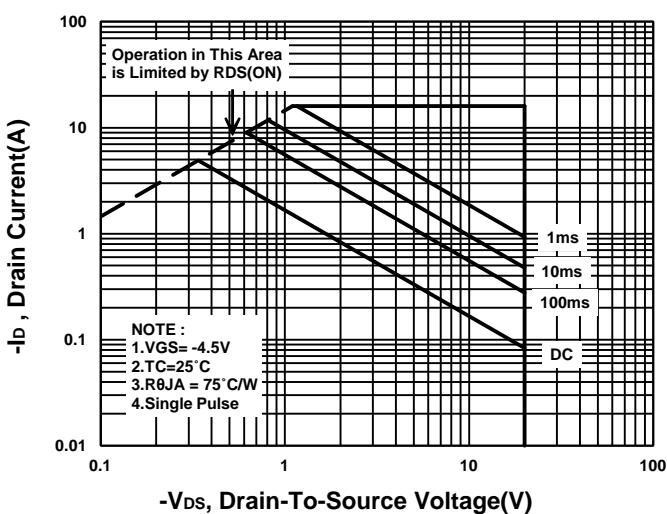
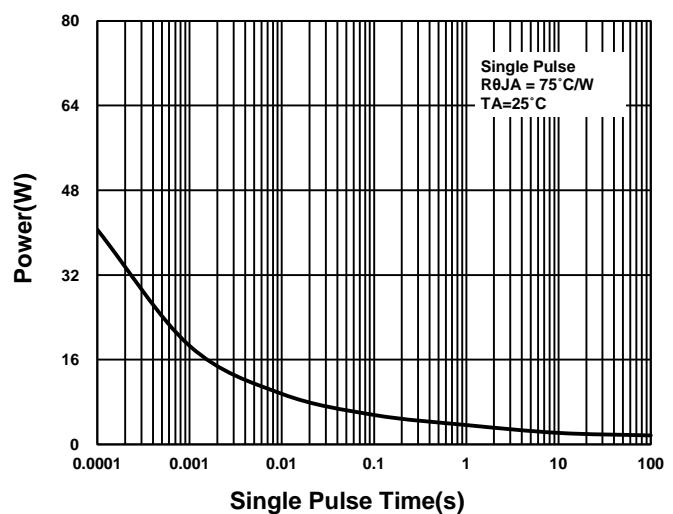


### On-Resistance VS Gate-To-Source



### On-Resistance VS Drain Current



**NIKO-SEM****P-Channel Logic Level Enhancement Mode  
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Halogen-free & Lead-Free****On-Resistance VS Temperature****Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**