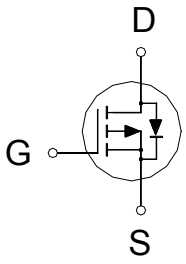
NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

PK5A1BA
PDFN 5x6P
Halogen-Free & Lead-Free

PRODUCT SUMMARY

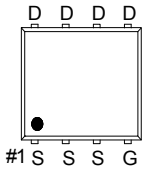
$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	6 mΩ	-48A



RoHS Compliant

Features
- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

Applications
- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G. GATE
D. DRAIN
S. SOURCE

100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current	T_C = 25 °C	I_D	-48	A
	T_C = 100 °C		-30	
	T_A = 25 °C		-18	
	T_A = 70 °C		-14.5	
Pulsed Drain Current[1]		I_{DM}	-100	
Avalanche Current		I_{AS}	-39	
Avalanche Energy	L = 0.1mH	E_{AS}	76	mJ
Power Dissipation[3]	T_C = 25 °C	P_D	25	W
	T_C = 100 °C		10	
	T_A = 25 °C		3.5	
	T_A = 70 °C		2.2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$		35	°C / W
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$		52	
Junction-to-Case	Steady-State	$R_{\theta JC}$		5	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

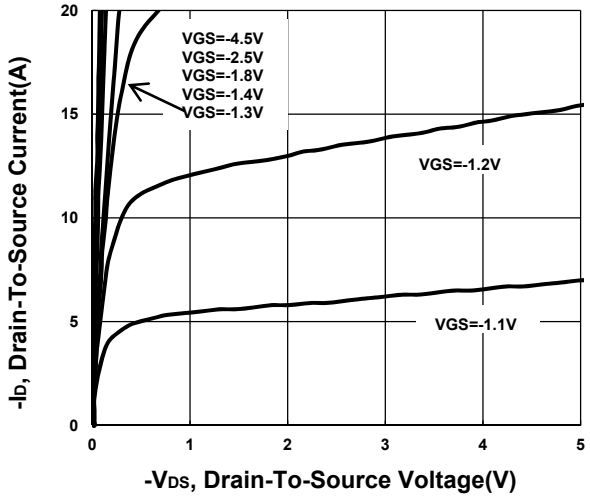
ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.45	-0.6	-0.9	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	uA
		V_{DS} = -10V, V_{GS} = 0V, T_J = 125 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -3.5A		4.7	6	mΩ
		V_{GS} = -2.5V, I_D = -3.5A		5.8	8	
		V_{GS} = -1.8V, I_D = -3.5A		7.4	11	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -3.5A		43		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		5731		pF
Output Capacitance	C_{oss}			542		
Reverse Transfer Capacitance	C_{rss}			420		
Gate Resistance	Rg	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		3		Ω
Total Gate Charge[2]	Q_g	V_{DS} = -10V, V_{GS} = -4.5V , I_D = -3.5A		64		nC
Gate-Source Charge[2]	Q_{gs}			6.5		
Gate-Drain Charge[2]	Q_{gd}			11.2		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -10V, I_D ≅ -3.5A, V_{GS} = -4.5V, R_{GS} = 6Ω		35		nS
Rise Time[2]	t_r			53		
Turn-Off Delay Time[2]	$t_{d(off)}$			187		
Fall Time[2]	t_f			105		

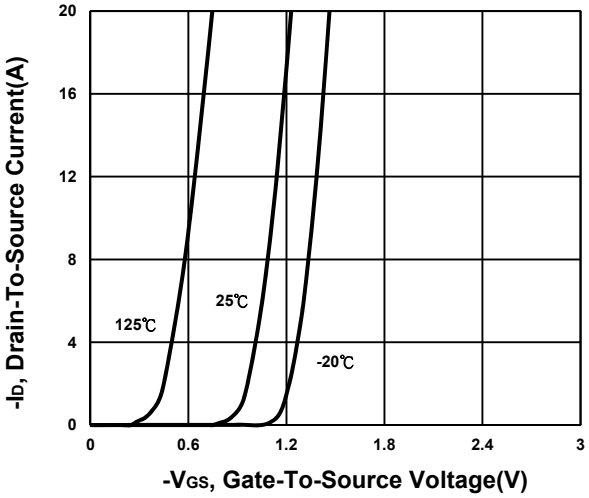
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-19	A
Forward Voltage[1]	V_{SD}	I_F = -3.5A, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -3.5A , dI_F/dt = 100 A / μS		41		nS
Reverse Recovery Charge	Q_{rr}			26		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

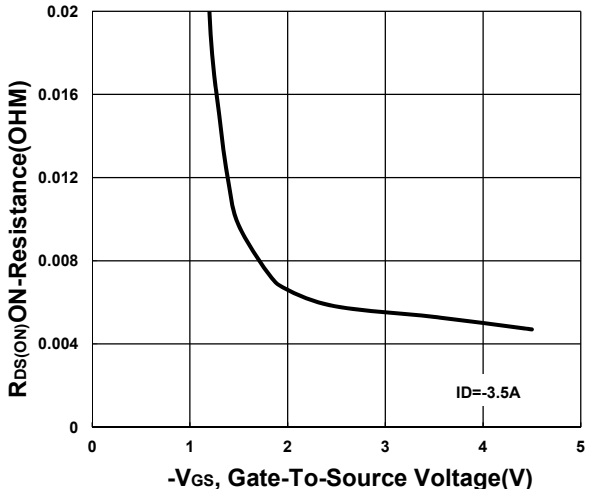
Output Characteristics



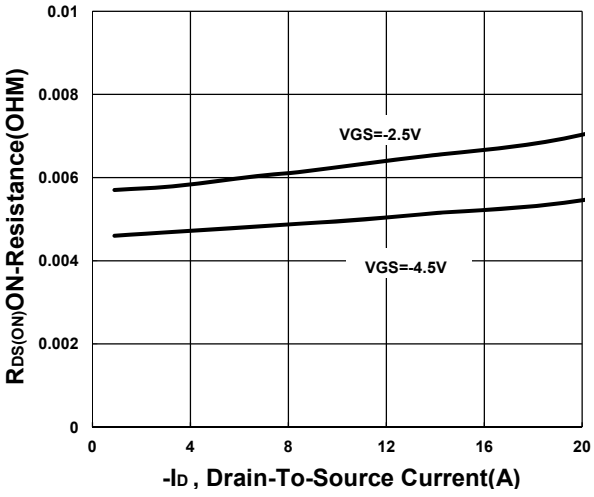
Transfer Characteristics



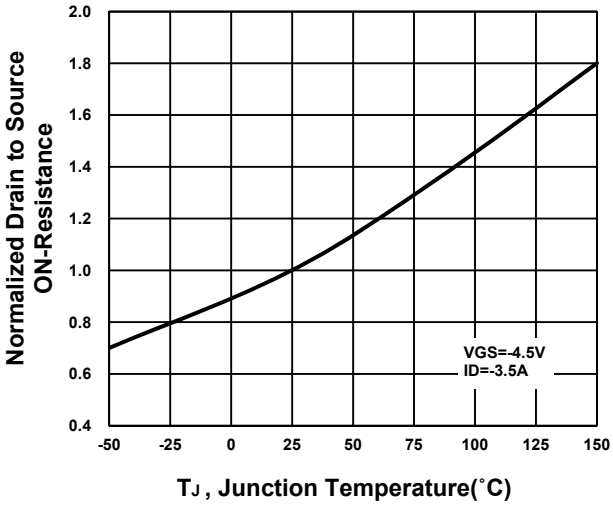
On-Resistance VS Gate-To-Source



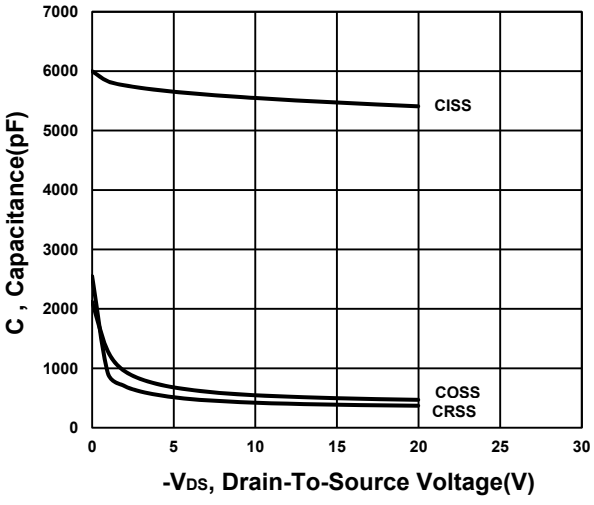
On-Resistance VS Drain Current



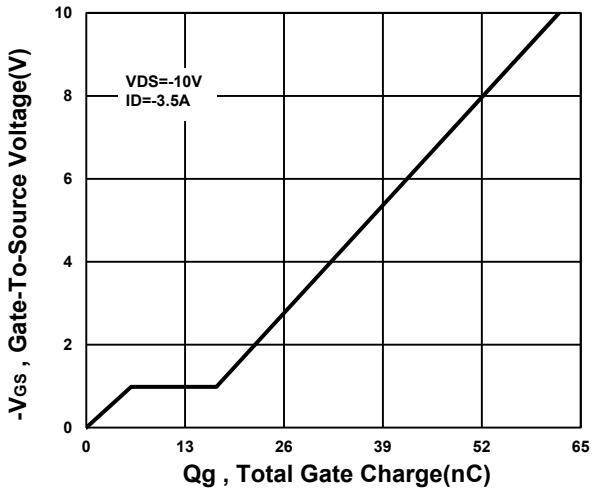
On-Resistance VS Temperature



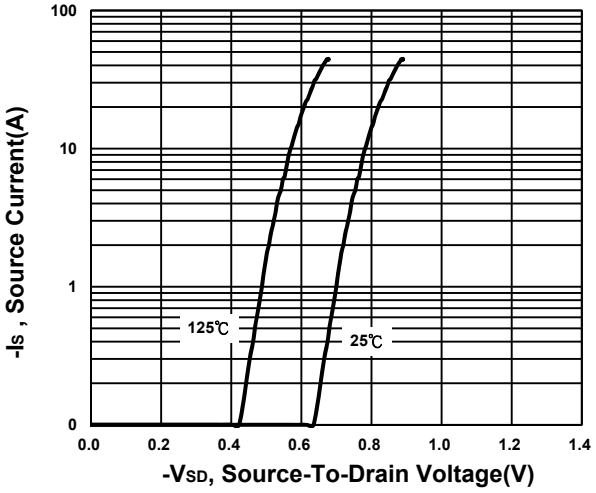
Capacitance Characteristic



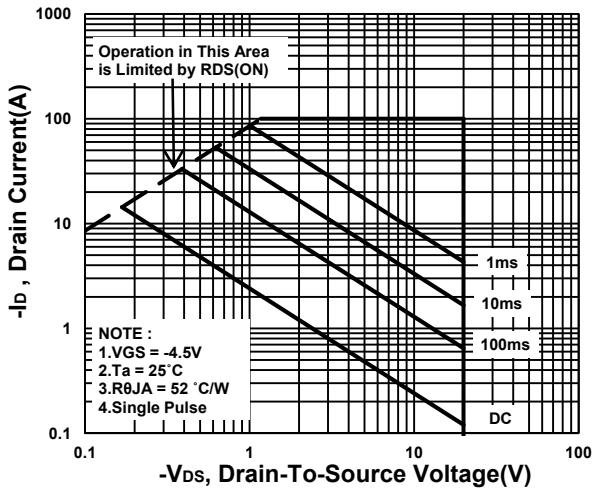
Gate charge Characteristics



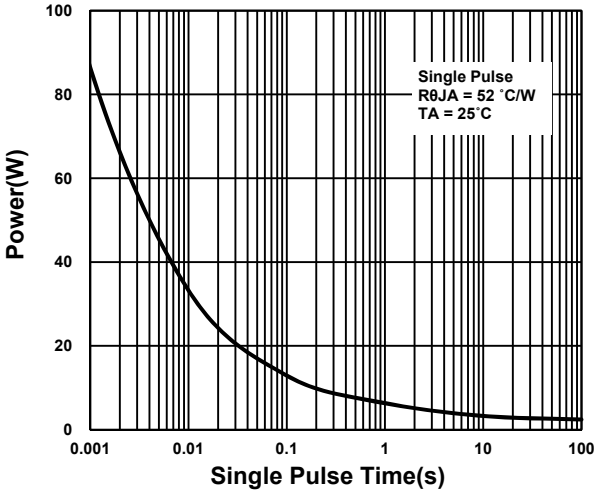
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve