NIKO-SEM

N- & P-Channel Enhancement Mode Field Effect Transistor

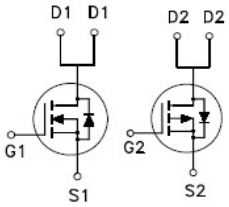
PK601CA

PDFN 5x6P

Halogen-Free & Lead-Free

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
Q2	-30V	28mΩ	-22A
Q1	30V	22mΩ	23A



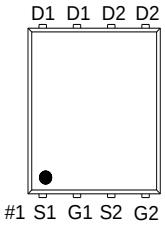
RoHS Compliant

Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.
- DC Motor for BLDC Applications.



G. GATE
D. DRAIN
S. SOURCE

100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	Q2	Q1	UNITS
Drain-Source Voltage		V_{DS}	-30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current[4]	T_C = 25 °C	I_D	-22	23	A
	T_C = 100 °C		-14	14	
Pulsed Drain Current[1]		I_{DM}	-45	50	
Continuous Drain Current	T_A = 25 °C	I_D	-7.8	8.6	
	T_A = 70 °C		-6.3	6.9	
Avalanche Current		I_{AS}	-19	12	
Avalanche Energy	L = 0.1mH	E_{AS}	18	7.3	mJ
Power Dissipation	T_C = 25 °C	P_D	25	22	W
	T_C = 100 °C		10	9	
Power Dissipation[3]	T_A = 25 °C	P_D	3	3	W
	T_A = 70 °C		2	2	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q2		40	°C / W
	Steady-State				57	
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q1		40	
	Steady-State				65	
Junction-to-Case		$R_{\theta JC}$	Q2		5	
		$R_{\theta JC}$	Q1		5.5	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.
[4]Package limitation current :Q1=10A,Q2=-10A

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

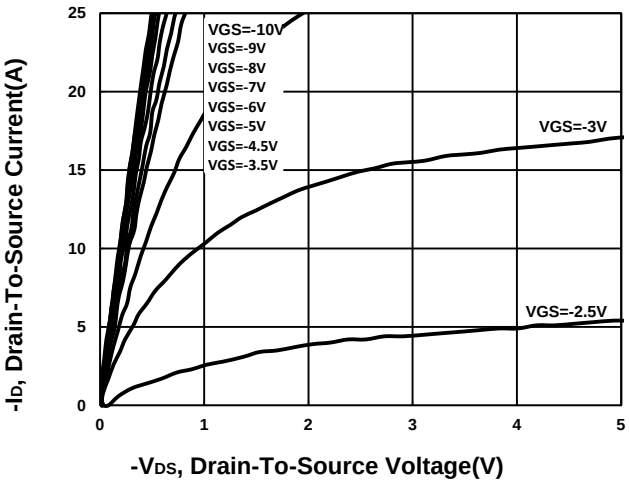
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	Q2	-30			V
		V_{GS} = 0V, I_D = 250μA	Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	Q2	-1	-1.5	-2.5	
		V_{DS} = V_{GS}, I_D = 250μA	Q1	1	1.6	2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q2			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V	Q2			-1	μA
		V_{DS} = 24V, V_{GS} = 0V	Q1			1	
		V_{DS} = -20V, V_{GS} = 0V, T_J = 55 °C	Q2			-10	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 55 °C	Q1			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -5A	Q2		30	45	mΩ
		V_{GS} = 4.5V, I_D = 6A	Q1		18	32	
		V_{GS} = -10V, I_D = -6A	Q2		20	28	
		V_{GS} = 10V, I_D = 7A	Q1		14	22	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -6A	Q2		18		S
		V_{DS} = 5V, I_D = 7A	Q1		27		

DYNAMIC							
Input Capacitance	C_{iss}	Q2 V_{GS} = 0V, V_{DS} = -15V, f = 1MHz Q1 V_{GS} = 0V, V_{DS} = 15V, f = 1MHz	Q2		929		pF
			Q1		341		
Output Capacitance	C_{oss}		Q2		145		
			Q1		84		
Reverse Transfer Capacitance	C_{rss}		Q2		122		
			Q1		48		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	Q2		12		Ω
			Q1		3		
Total Gate Charge[2]	Q_g VGS = 10V	Q2 V_{DS} = -15V , V_{GS} = -10V, I_D = -6A Q1 V_{DS} = 15V , V_{GS} = 10V, I_D = 7A	Q2		20.8		nC
			Q1		7.6		
	Q_g VGS = 4.5V		Q2		10.8		
			Q1		4.3		
Gate-Source Charge[2]	Q_{gs}		Q2		2		
			Q1		1		
Gate-Drain Charge[2]	Q_{gd}		Q2		5		
			Q1		2		
Turn-On Delay Time[2]	$t_{d(on)}$	Q2 , V_{DS} = -15V , $I_D \cong$ -6A, V_{GS} = -10V, R_{GEN} =6Ω Q1 , V_{DS} = 15V , $I_D \cong$ 7A, V_{GS} = 10V, R_{GEN} =6Ω	Q2		15		nS
			Q1		15		
Rise Time[2]	t_r		Q2		30		
			Q1		30		
Turn-Off Delay Time[2]	$t_{d(off)}$		Q2		50		
			Q1		20		
Fall Time[2]	t_f		Q2		41		
			Q1		13		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current[3]	I_S		Q2			-25	A
			Q1			20	
Forward Voltage[1]	V_{SD}	I_F = -6A, V_{GS} = 0V	Q2			-1	V
		I_F = 7A, V_{GS} = 0V	Q1			1.1	
Reverse Recovery Time	t_{rr}	Q2 I_F = -6A, dI_F/dt = 100A / μS Q1 I_F = 7A, dI_F/dt = 100A / μS	Q2		12.6		nS
			Q1		7.9		
Reverse Recovery Charge	Q_{rr}		Q2		4.2		nC
			Q1		1.2		

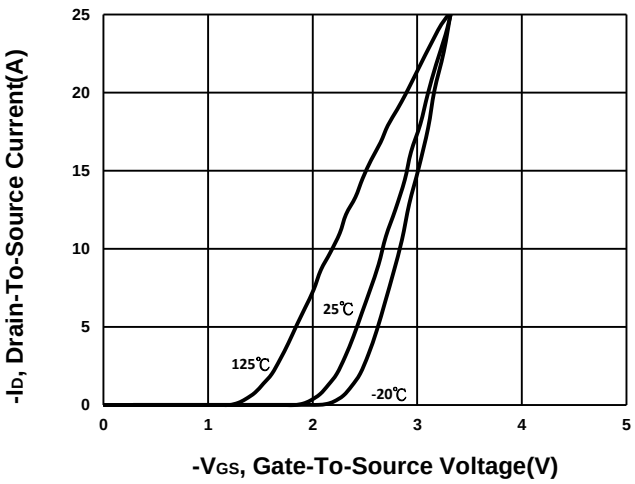
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Package limitation current :Q1=10A,Q2=-10A

TYPICAL PERFORMANCE CHARACTERISTICS
Q2 P-CHANNEL

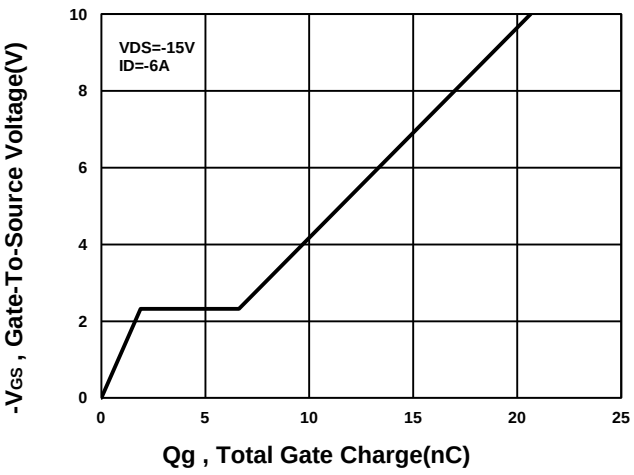
Output Characteristics



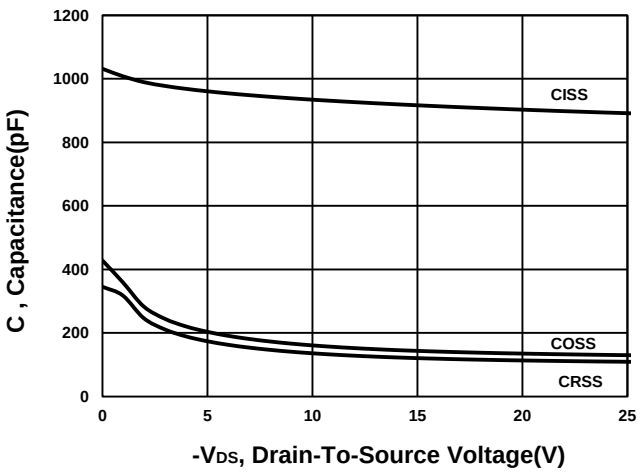
Transfer Characteristics



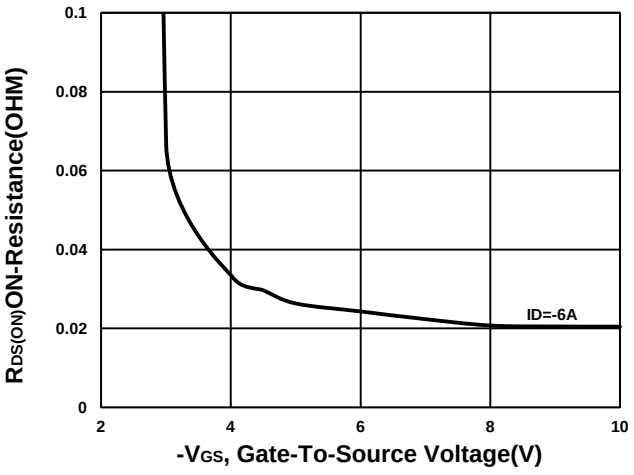
Gate charge Characteristics



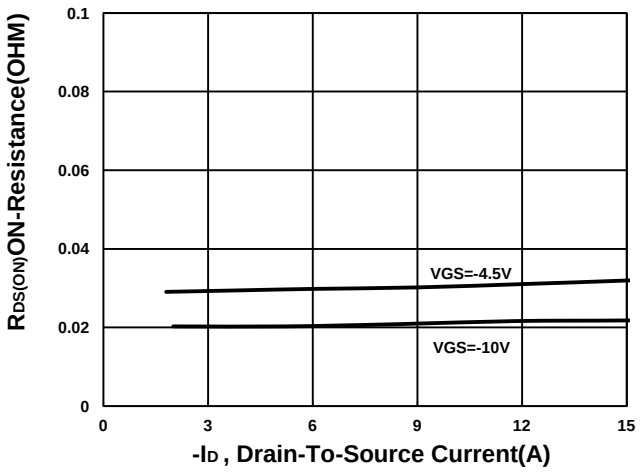
Capacitance Characteristic



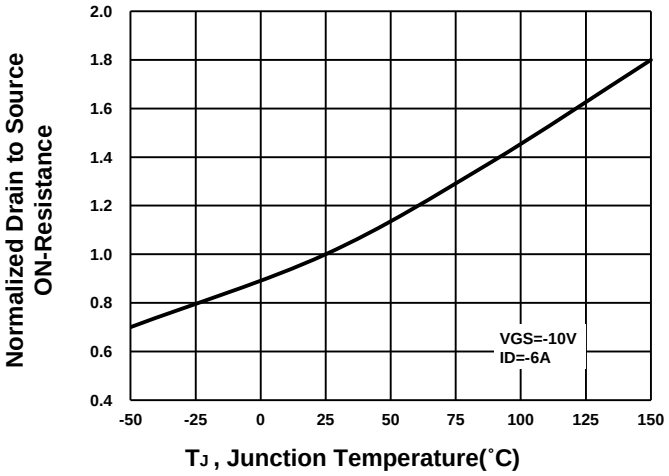
On-Resistance VS Gate-To-Source



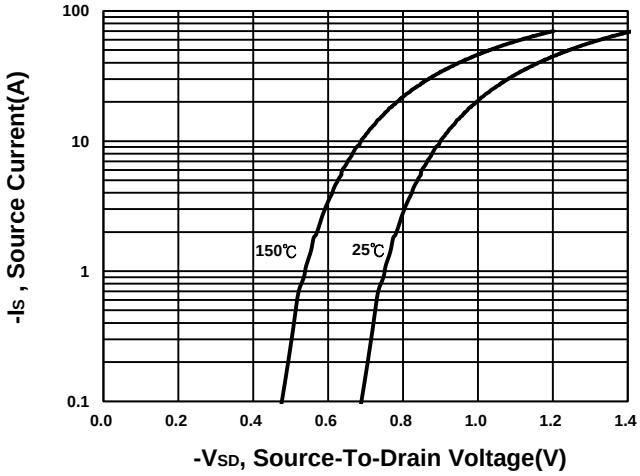
On-Resistance VS Drain Current



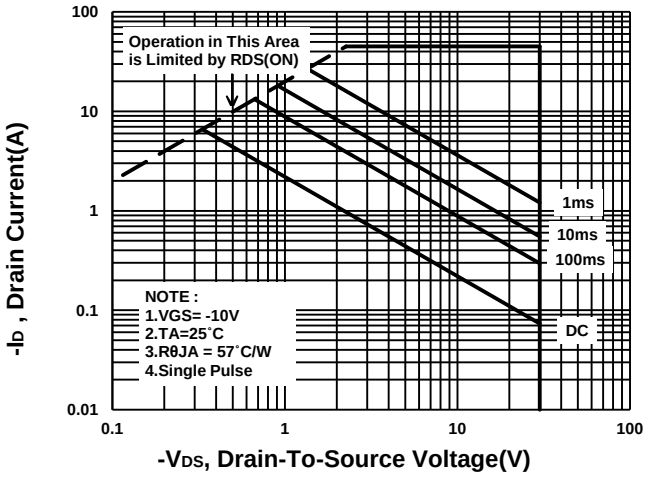
On-Resistance VS Temperature



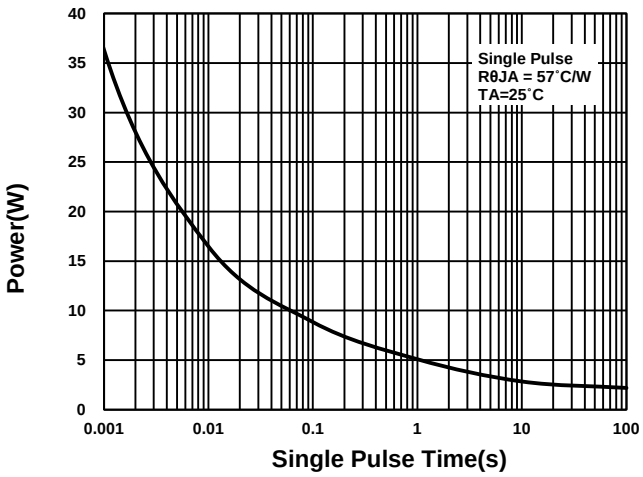
Source-Drain Diode Forward Voltage



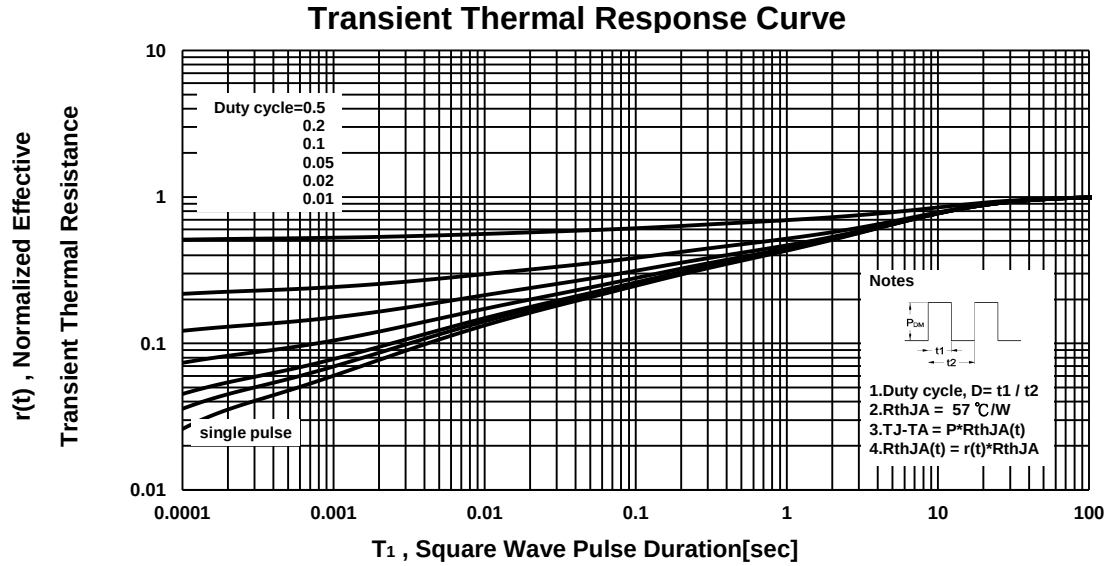
Safe Operating Area



Single Pulse Maximum Power Dissipation

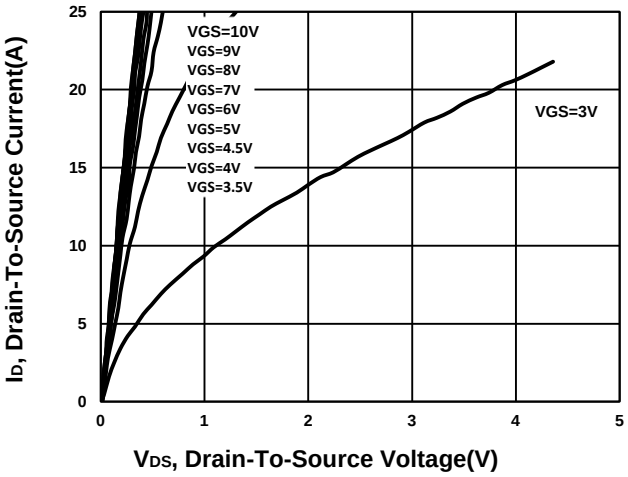


Transient Thermal Response Curve

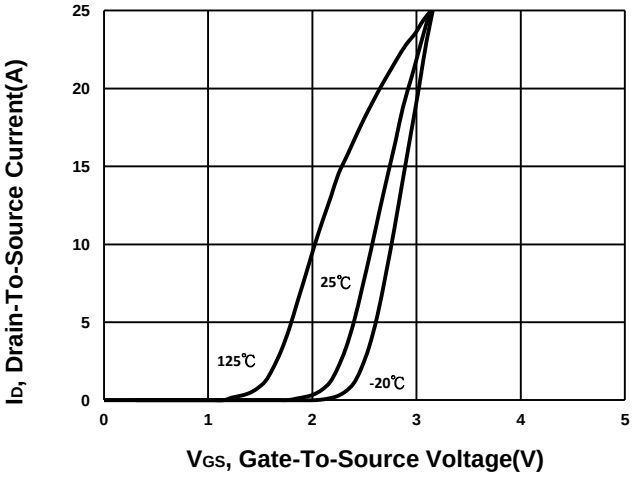


Q1 N-CHANNEL

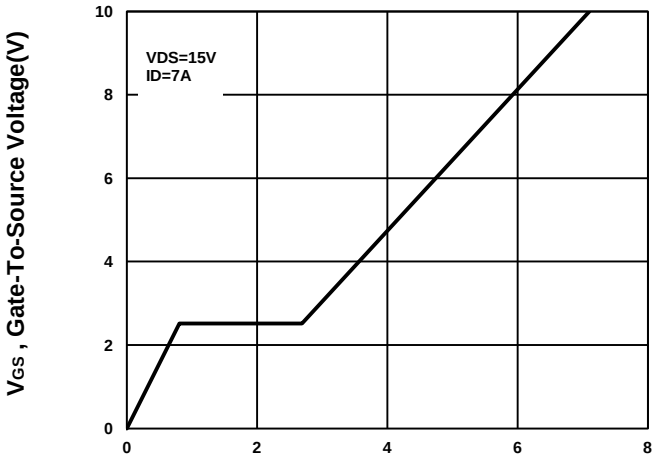
Output Characteristics



Transfer Characteristics



Gate charge Characteristics



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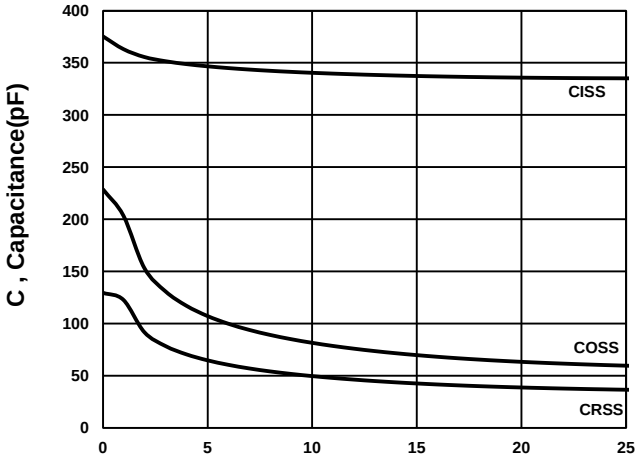
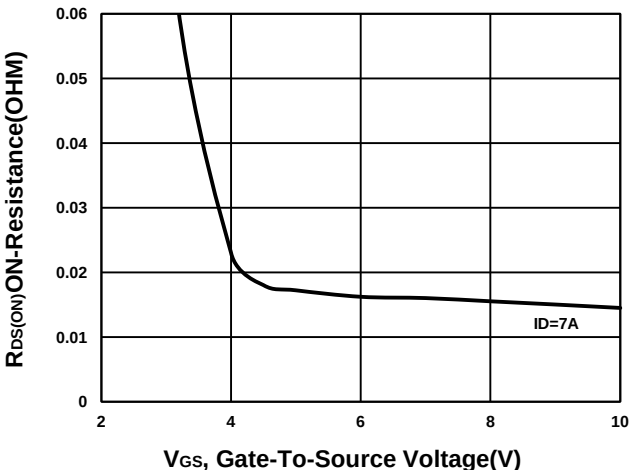
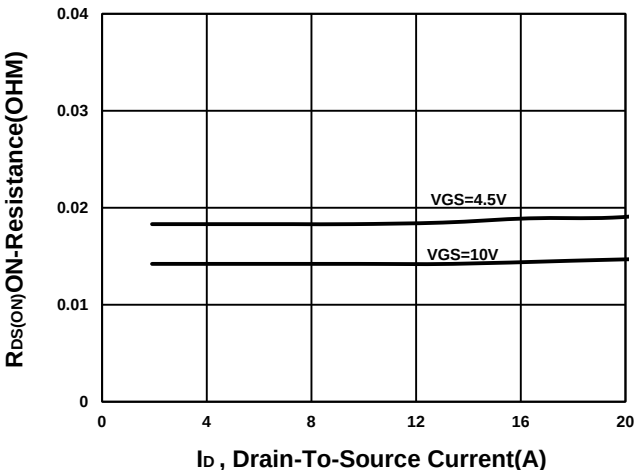


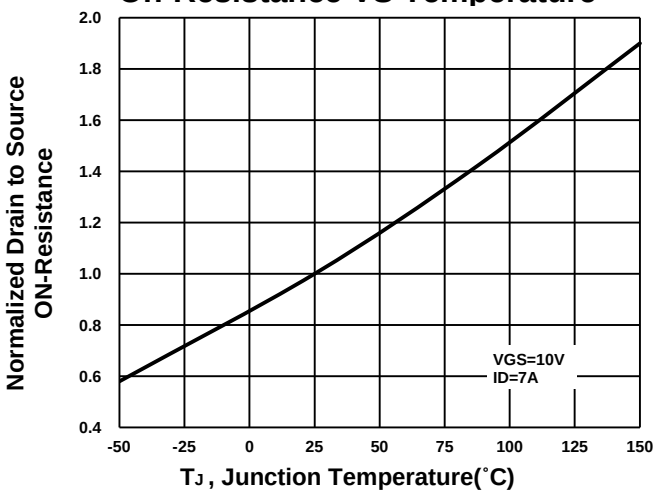
On-Resistance VS Gate-To-Source



On-Resistance VS Drain Current



On-Resistance VS Temperature



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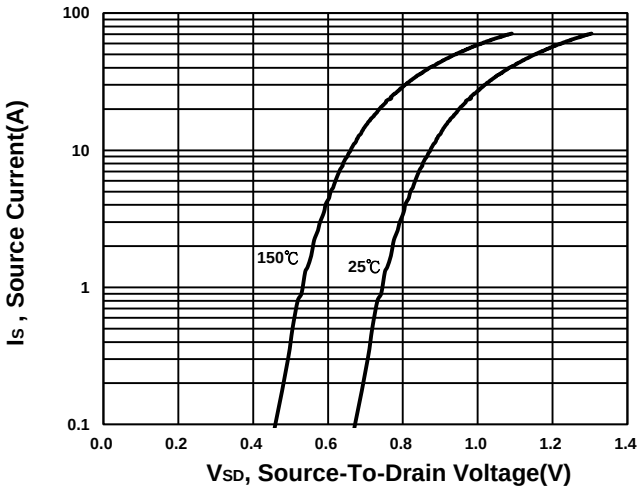

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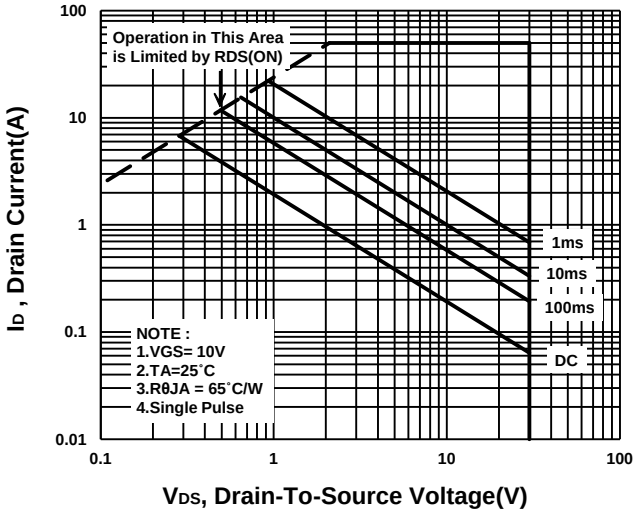

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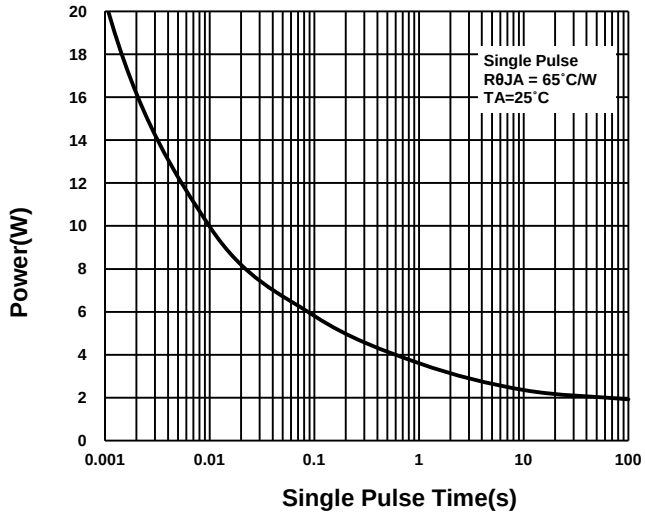

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