

N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{(BR)DSS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)			
100	0.018 at V _{GS} = 10 V	65 ^a			

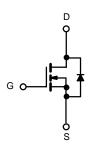
FEATURES

- DT-Trench Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 % R_g and UIS tested



APPLICATIONS

• Isolated DC/DC Converters



N-Channel MOSFET

D ² PAK (TO-263)
G D S
Top View

ABSOLUTE MAXIMUM RATINGS	T _C = 25 °C, unless oth	erwise noted		
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	100	V
Gate-Source Voltage		V _{GS}	± 20	V
Continuous Drain Current (T _{.1} = 175 °C)	T _C = 25 °C	1-	65 ^a	
Continuous Drain Current (1) = 173 C)	T _C = 125 °C	I _D	37 ^a	
Pulsed Drain Current		I _{DM}	195	^
Avalanche Current L = 0.1 mH		I _{AS}	35	
Single Pulse Avalanche Energy ^b	L = U. I IIII	E _{AS}	61	mJ
Mariana Brasinata h	T _C = 25 °C	D D	375 ^c	14/
Maximum Power Dissipation ^b	T _A = 25 °C ^d	P_{D}	3.75	W
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	PCB Mount (TO-263) ^d	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)		R _{thJC}	0.4	C/VV	

Notes:

- a. Package limited.
- b. Duty cycle \leq 1 %.
- c. See SOA curve for voltage derating.
- d. When Mounted on 1" square PCB (FR-4 material).

Rev. 1.0





Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	100			١/	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
		V _{DS} = 80 V , V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V, T _J = 125 °C			50	μΑ	
		$V_{DS} = 80 \text{ V} , V_{GS} = 0 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	65			Α	
		V _{GS} = 10 V, I _D = 20 A		0.018	0.025		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 15 A, T _J = 125 °C		0.021	0.029	Ω	
		V _{GS} = 10 V, I _D = 10 A, T _J = 175 °C		0.024	0.033		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 80 V, I _D = 20 A		110		S	
Dynamic ^b	1			•			
Input Capacitance	C _{iss}			1298		pF	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		280			
Reverse Transfer Capacitance	C _{rss}			960			
Total Gate Charge ^c	Q_g			90	130		
Gate-Source Charge ^c	Q_{gs}	$V_{DS} = 80 \text{ V}, \ \ V_{GS} = 10 \text{ V}, \ I_{D} = 20 \text{ A}$		23		nC	
Gate-Drain Charge ^c	Q_{gd}			34			
Gate Resistance	R _g		0.5	1.7	3.3	Ω	
Turn-On Delay Time ^c	t _{d(on)}			24	35		
Rise Time ^c	t _r	$V_{DD} = 80 \text{ V}, R_{L} = 1.5 \Omega$		220	330		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		45	70	ns	
Fall Time ^c	t _f			200	300		
Source-Drain Diode Ratings and Cha	aracteristics 7	C _C = 25 °C ^b		•			
Continuous Current	Is				65	^	
Pulsed Current	I _{SM}				195	A	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			130	200	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 20 A, di/dt = 100 A/μs		8	12	Α	
Reverse Recovery Charge	Q _{rr}			0.52	1.2	μC	

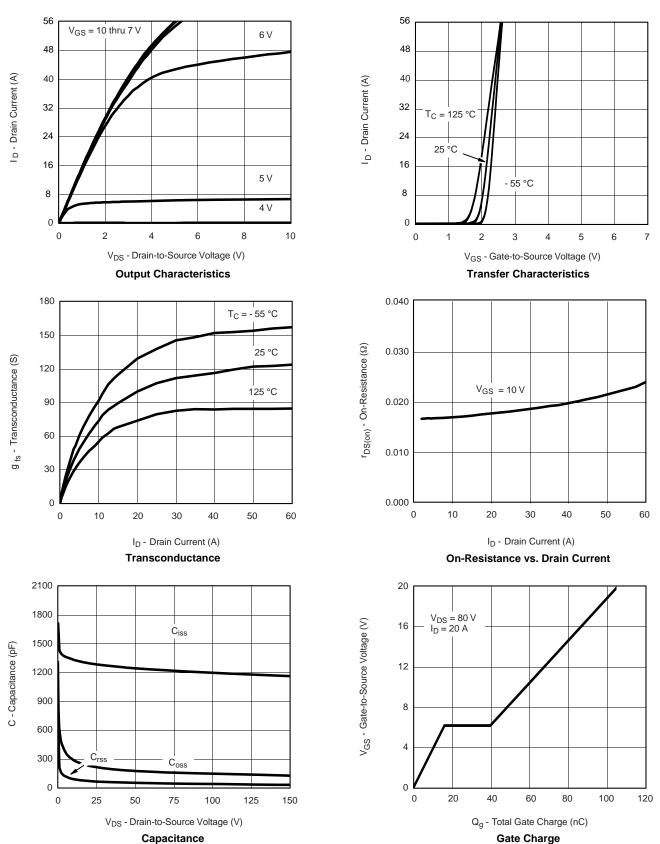
Notes:

- a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

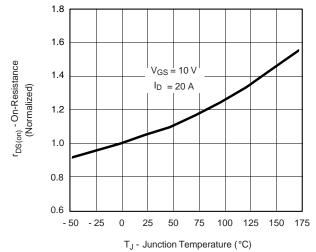


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

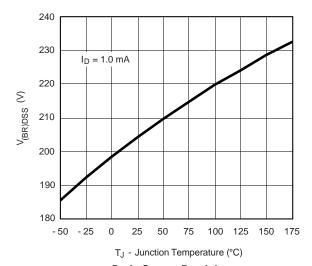




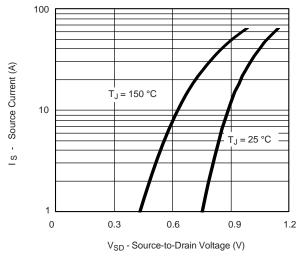
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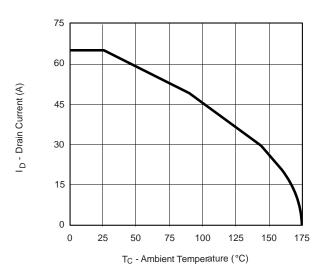
On-Resistance vs. Junction Temperature



Drain Source Breakdown vs. Junction Temperature



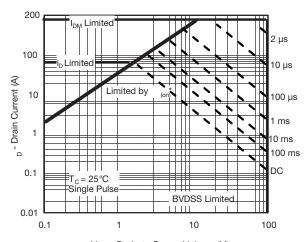
Source-Drain Diode Forward Voltage



Maximum Avalanche and Drain Current vs. Case Temperature

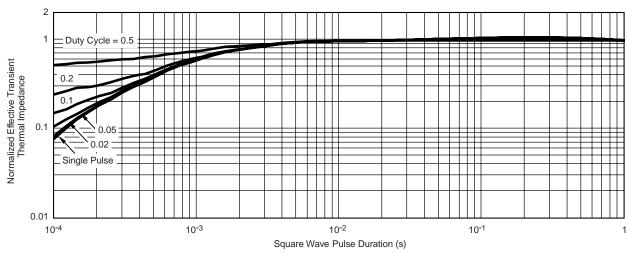


THERMAL RATINGS



 $\label{eq:VDS} $$V_{DS}$ - Drain-to-SourceVoltage (V) $$^*V_{GS} > minimum\,V_{GS}$ at which $r_{DS(on)}$ is specified$

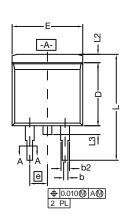
Safe Operating Area

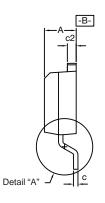


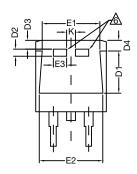
Normalized Thermal Transient Impedance, Junction-to-Case



TO-263 (D²PAK): 3-LEAD

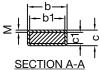








DETAIL A (ROTATED 90°)



b b1		1
<u> </u>	<u>.</u>	C)
	f	Ŧ

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement. This feature is for thick lead.

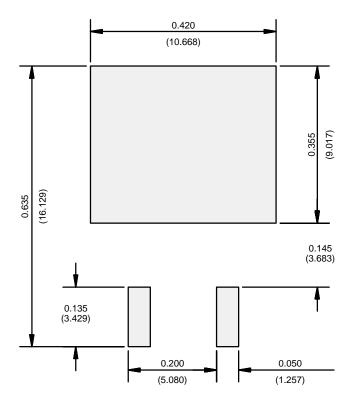
		INC	CHES	MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
	Thick lead	0.023	0.028	0.584	0.711	
с1	Thin lead	0.013	0.017	0.330	0.431	
01	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829 1.981		
	е	0.100 BSC		2.54 BSC		
	K	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K. 30-Sep-13						

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DWG: 5843



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)





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