

# N-Channel 150 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)			
150	0.241 at V <sub>GS</sub> = 10 V	6			
	0.250 at V <sub>GS</sub> = 4.5 V	4			

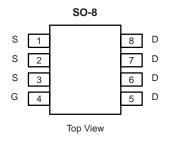
#### FEATURES

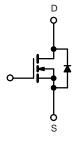
- DT-Trench Power MOSFET
- 175 °C Junction Temperature
- 100 % R<sub>g</sub> Tested



#### **APPLICATIONS**

• Primary Side Switch





N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V <sub>DS</sub>	150	- v			
Gate-Source Voltage	V <sub>GS</sub>	± 20				
Continuous Drain Current $(T_1 = 175 \ ^{\circ}C)^{b}$	T <sub>C</sub> = 25 °C T <sub>C</sub> = 125 °C	1_	6			
Commuous Drain Current $(T_j = 175 \text{ C})^2$	T <sub>C</sub> = 125 °C	I <sub>D</sub>	4.7			
Pulsed Drain Current	I <sub>DM</sub>	25	А			
Continuous Source Current (Diode Conduction)	۱ <sub>S</sub>	5.2	1			
Avalanche Current	I <sub>AR</sub>	4.5	7			
Repetitive Avalanche Energy (Duty Cycle $\leq$ 1 %)	L = 0.1 mH	E <sub>AR</sub>	11.3	mJ		
Manimum David Disain ation	T <sub>C</sub> = 25 °C	P	62 <sup>b</sup>	W		
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.7 <sup>a</sup>	V		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
hungtion to Ambienta	t ≤ 10 s	- R <sub>thJA</sub>	16	20	°C/W		
Junction-to-Ambient <sup>a</sup>	Steady State		45	55			
Junction-to-Case		R <sub>thJC</sub>	2	2.4			

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

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Parameter	Symbol	Test Conditions Min		Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	150			V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2			V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1	μA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50		
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	1	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 V, V_{GS} = 10 V$	15			А	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A		0.241	0.263	Ω	
- ·	Р	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A, T <sub>J</sub> = 125 °C		0.249	0.273		
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A, T <sub>J</sub> = 175 °C		0.280	0.302		
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 2 \text{ A}$		0.250	0.275		
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2 A		25		S	
Dynamic <sup>a</sup>		·					
Input Capacitance	C <sub>iss</sub>			900		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		115			
Reverse Transfer Capacitance	C <sub>rss</sub>			70			
Total Gate Charge <sup>c</sup>	Qg			20	25		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS} = 75 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 2 \text{ A}$		5.5		nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			7			
Gate Resistance	Rg		1		3.2	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			8	12		
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 75 V, $R_L$ = 5 $\Omega$		35	55		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 2 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{G}} = 2.5$		17	25	ns	
Fall Time <sup>c</sup>	t <sub>f</sub>	Ω		30	45		
Source-Drain Diode Ratings and Cha	racteristic (T	<sub>C</sub> = 25 °C)					
Pulsed Current	I <sub>SM</sub>				6	А	
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 2 A, V <sub>GS</sub> = 0 V		0.9	1.5	V	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2 A, dl/dt = 100 A/µs		55	85	ns	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

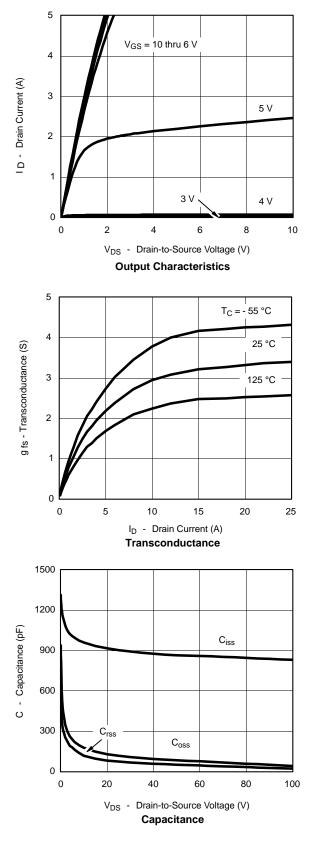
c. Independent of operating temperature.

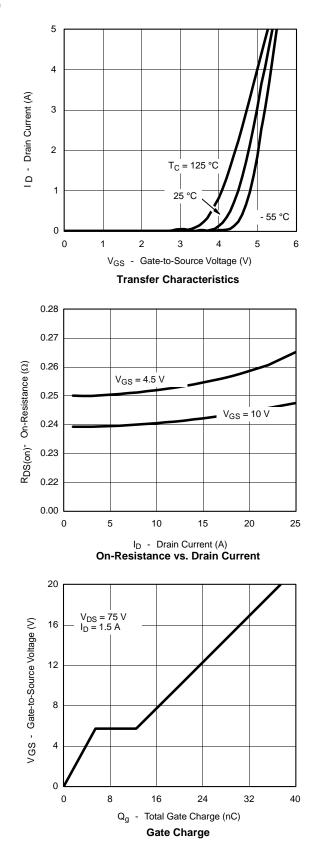
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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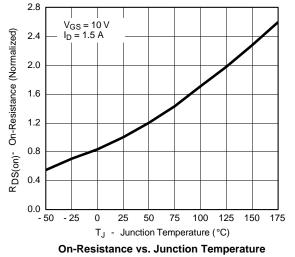
#### TYPICAL CHARACTERISTICS (25 °C unless noted)





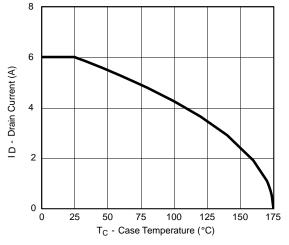
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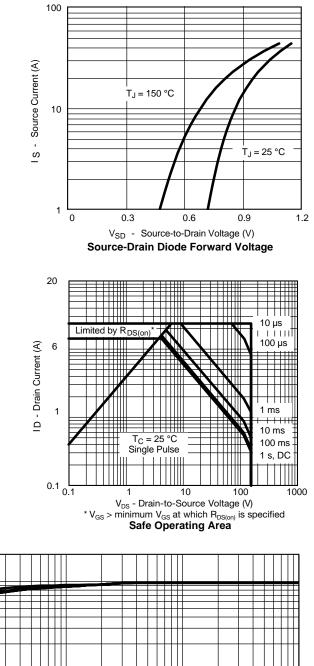


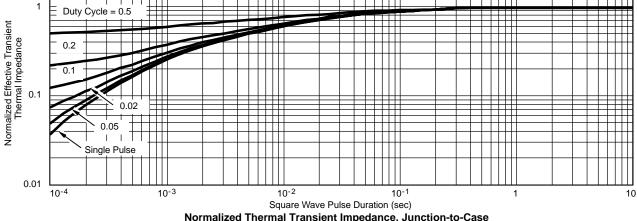
**THERMAL RATINGS** 

2



**Maximum Avalanche Drain Current** vs. Case Temperature





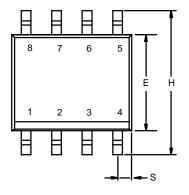
Normalized Thermal Transient Impedance, Junction-to-Case

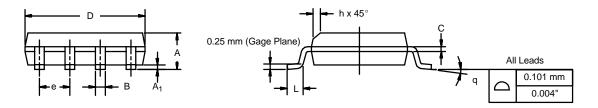


# Package Information www.din-tek.jp

### SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIM	IETERS	INC	IES		
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



#### **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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