

NIKO-SEM

P-Channel Enhancement Mode Field Effect Transistor

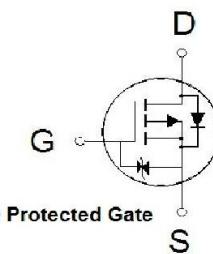
PD5G3EA
TO-252
Halogen-Free & Lead-Free

PRODUCT SUMMARY

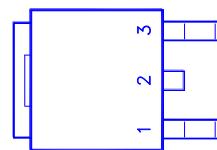
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30V	8mΩ	-81A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected.

**Applications**

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-81	A
		-51	
Pulsed Drain Current ¹	I_{DM}	-240	
Avalanche Current	I_{AS}	-69	
Avalanche Energy	E_{AS}	238	mJ
Power Dissipation	P_D	89	W
		35	
Junction & Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$	1.4	62.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$			

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.3	-1.84	-2.3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±10	uA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	μA
		V _{DS} = -30V, V _{GS} = 0V, T _J = 125 °C			-10	
Drain-Source On-State Resistance ²	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -20A		9.1	13.8	mΩ
		V _{GS} = -10V, I _D = -20A		5.1	8	
Forward Transconductance ²	g _f	V _{DS} = -5V, I _D = -20A	42			S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		5370		pF
Output Capacitance	C _{oss}			800		
Reverse Transfer Capacitance	C _{rss}			688		
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		1.9		Ω
Total Gate Charge ³	Q _g (V _{GS} =-10V)	V _{DS} = -15V, V _{GS} = -10V, I _D = -20A		117		nC
	Q _g (V _{GS} =-4.5V)			57		
Gate-Source Charge ³	Q _{gs}			18		
Gate-Drain Charge ³	Q _{gd}			27		
Turn-On Delay Time ³	t _{d(on)}	V _{DS} = -15V, I _D ≈ -20A, V _{GS} = -10V, R _{GEN} = 6Ω		24		nS
Rise Time ³	t _r			92		
Turn-Off Delay Time ³	t _{d(off)}			150		
Fall Time ³	t _f			122		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I _S				-68	A
Forward Voltage ²	V _{SD}	I _F = -20A, V _{GS} = 0V			-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -20A, dI _F /dt = 100A / μS		27		nS
Reverse Recovery Charge	Q _{rr}			22		nC

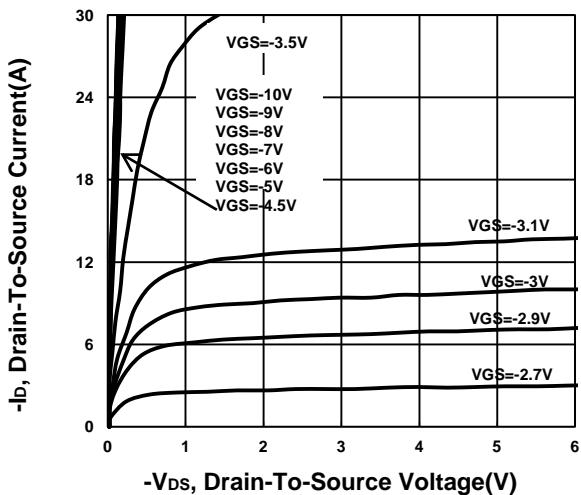
¹Pulse width limited by maximum junction temperature.²Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.³Independent of operating temperature.

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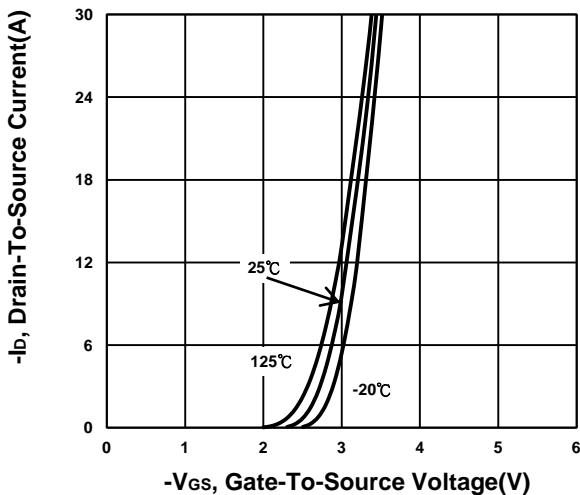
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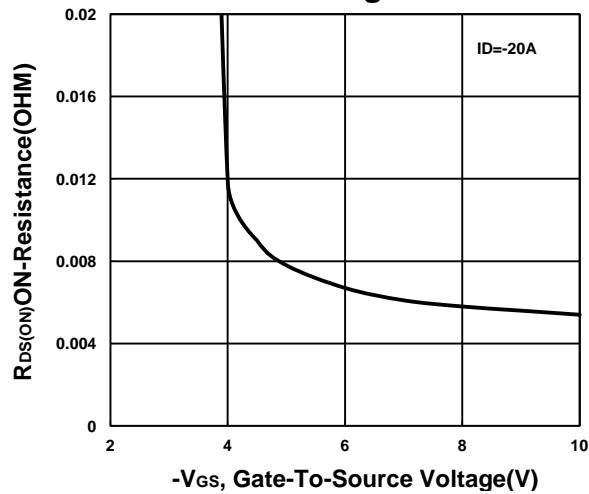
Output Characteristics



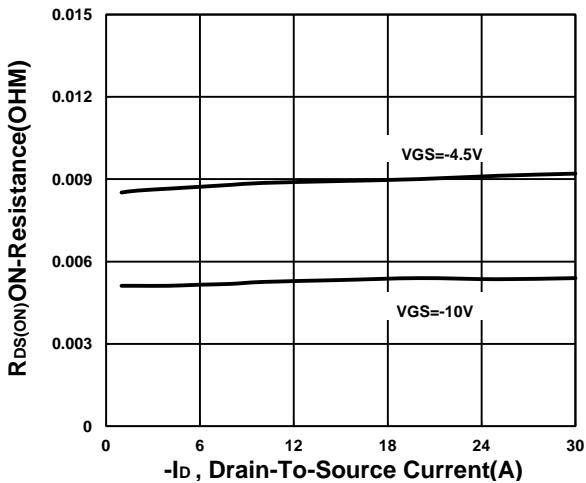
Transfer Characteristics



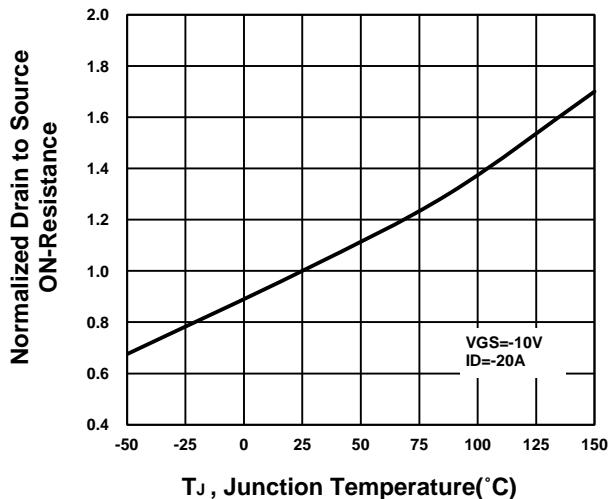
On-Resistance VS Gate-To-Source Voltage



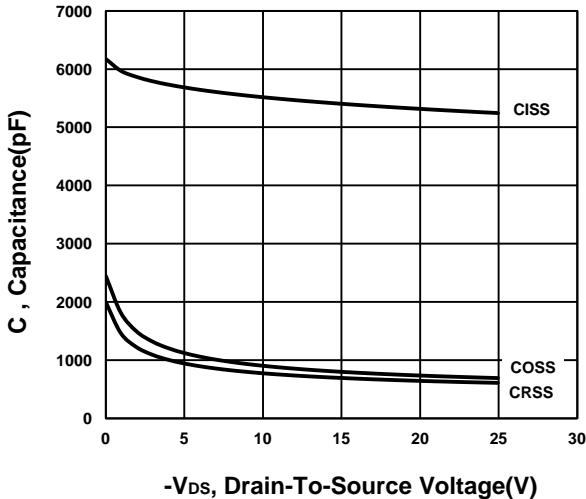
On-Resistance VS Drain Current



On-Resistance VS Temperature



Capacitance Characteristic

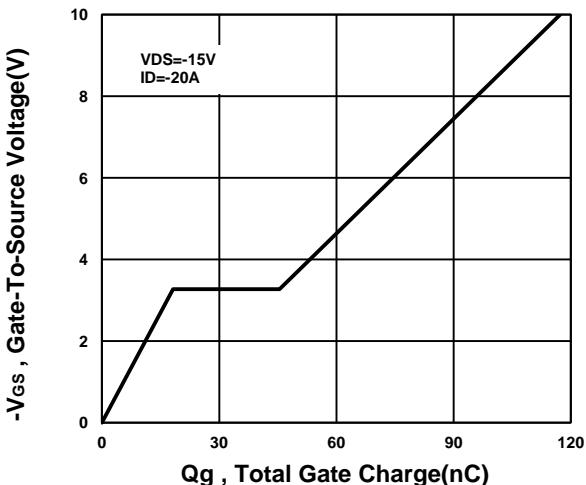


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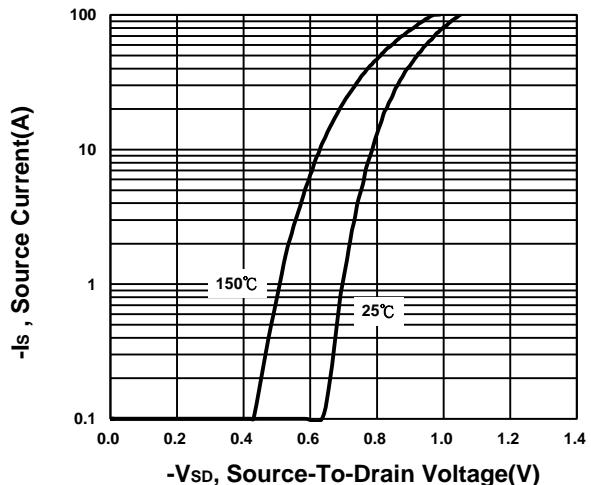
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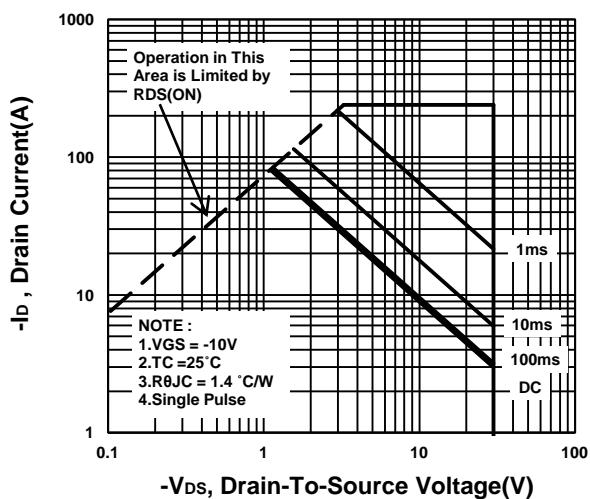
Gate charge Characteristics



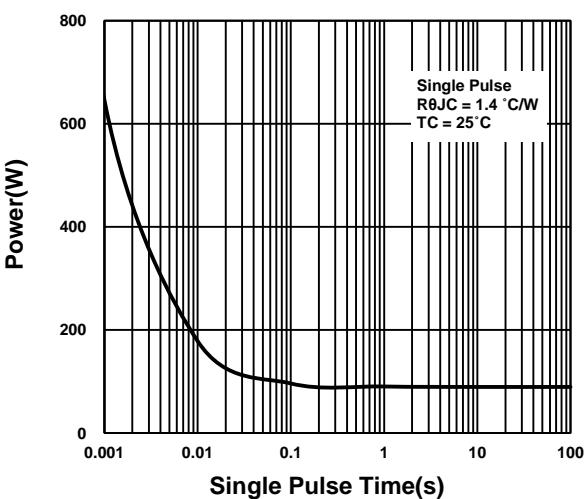
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

