NIKO-SEM

N-Channel Enhancement Mode Field Effect Transistor

PD5P8BA

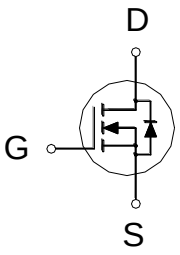
TO-252

Halogen-Free & Lead-Free

RoHS Compliant

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
20V	12mΩ	34A

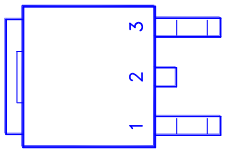


Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



1. GATE
2. DRAIN
3. SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_C = 25 °C	I_D	34	A
	T_C = 100 °C		21	
Pulsed Drain Current[1]		I_{DM}	70	
Avalanche Current		I_{AS}	17.8	
Avalanche Energy	L = 0.1mH	E_{AS}	15.8	mJ
Power Dissipation	T_C = 25 °C	P_D	25	W
	T_C = 100 °C		10	
Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		62.5	

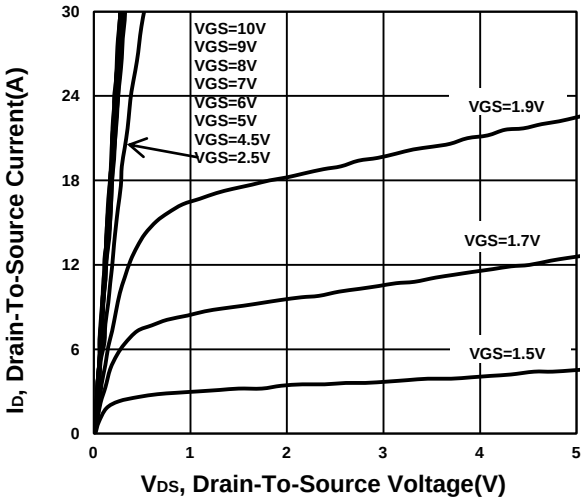
[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

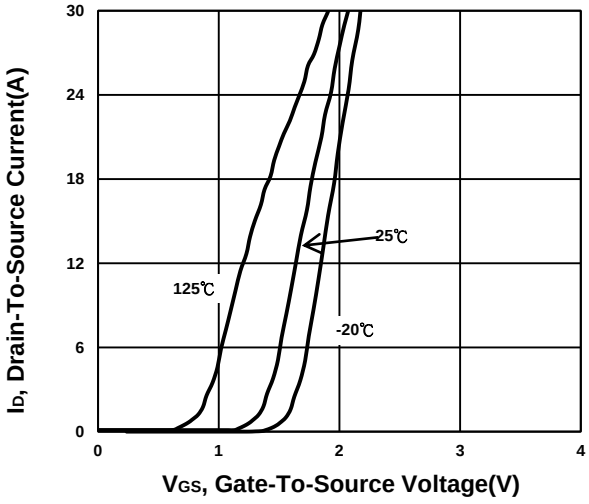
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.45	0.8	1.25	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 10V, V_{GS} = 0V, T_J = 125 °C			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V , I_D = 20A		7.9	12	mΩ
		V_{GS} = 4.5V, I_D = 18A		9.3	14	
		V_{GS} = 2.5V, I_D = 9A		13.4	28	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 20A		36		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		718		pF
Output Capacitance	C_{oss}			149		
Reverse Transfer Capacitance	C_{rss}			122		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz		2.2		Ω
Total Gate Charge[2]	$Q_{g(VGS=10V)}$	V_{DS} = 10V , I_D = 20A		19		nC
	$Q_{g(VGS=4.5V)}$			10		
Gate-Source Charge[2]	Q_{gs}			1.1		
Gate-Drain Charge[2]	Q_{gd}			4.3		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = 10V $I_D \cong$ 20A, V_{GS} = 10V, R_{GEN} =6Ω		8.8		nS
Rise Time[2]	t_r			112		
Turn-Off Delay Time[2]	$t_{d(off)}$			38		
Fall Time[2]	t_f			132		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				19	A
Forward Voltage[1]	V_{SD}	I_F = 10A, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 10A, dI_F/dt = 100A / μS		10		nS
Reverse Recovery Charge	Q_{rr}			3.1		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

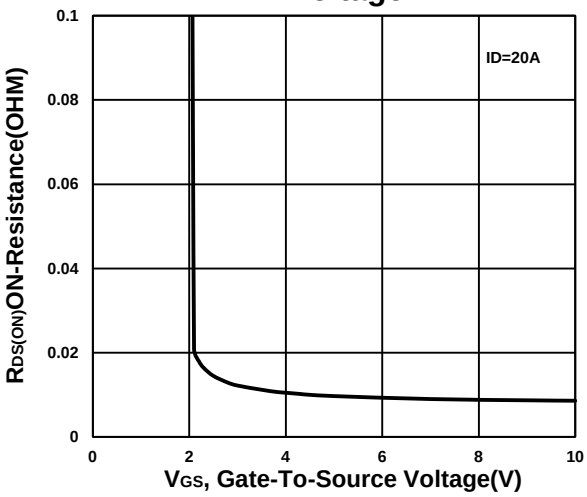
Output Characteristics



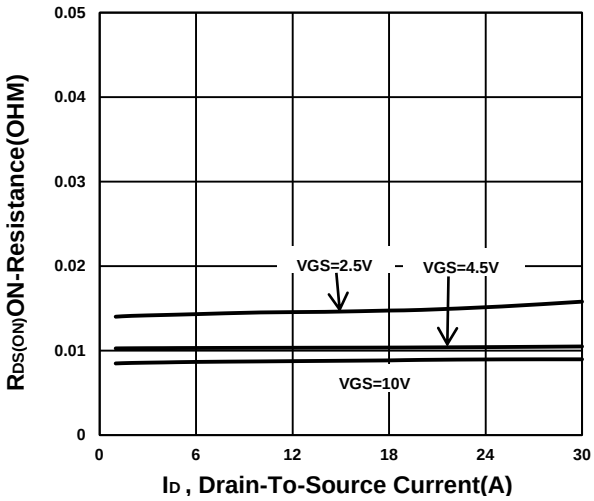
Transfer Characteristics



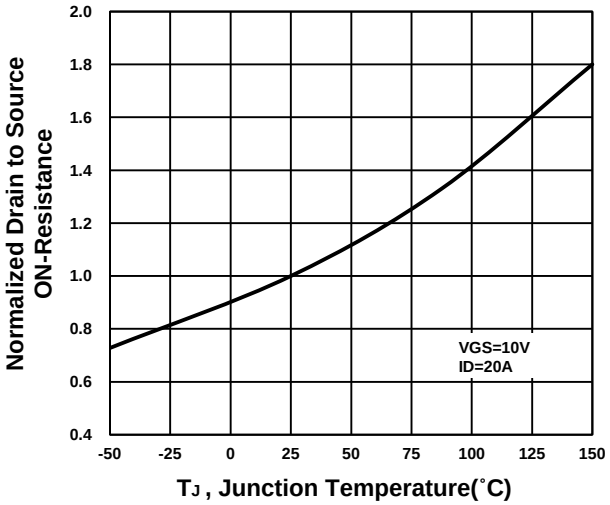
On-Resistance VS Gate-To-Source Voltage



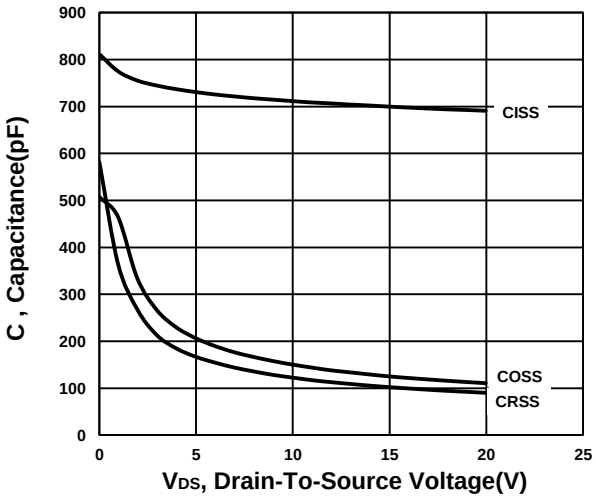
On-Resistance VS Drain Current



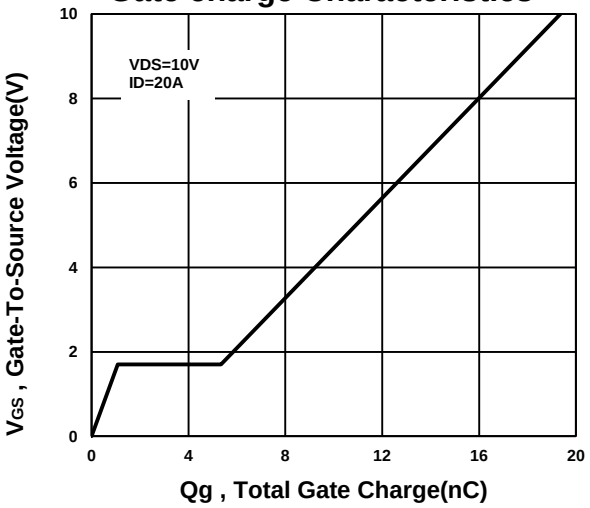
On-Resistance VS Temperature



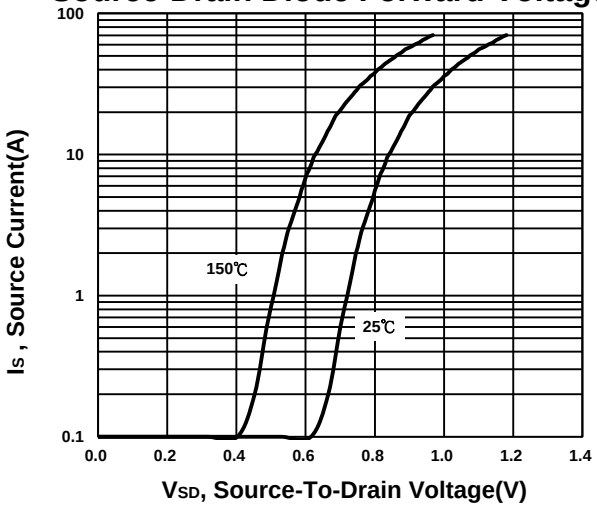
Capacitance Characteristic



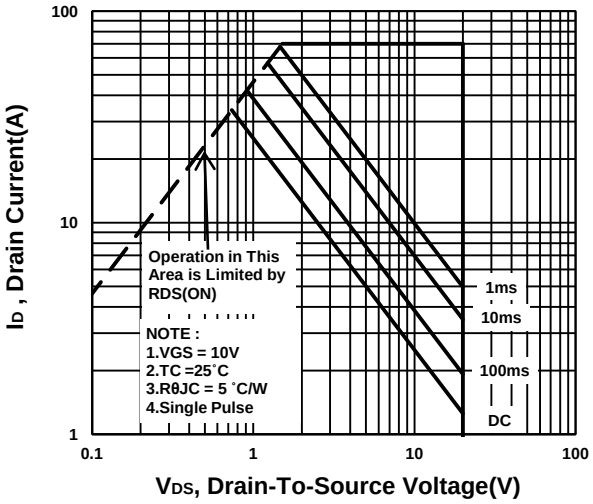
Gate charge Characteristics



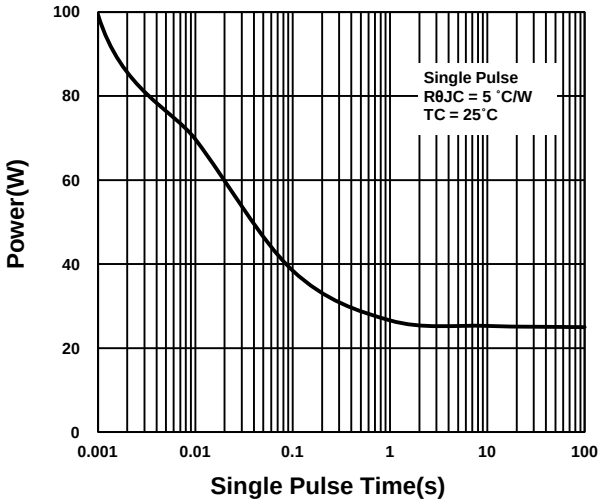
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve