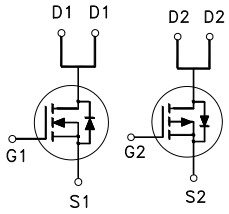
NIKO-SEM

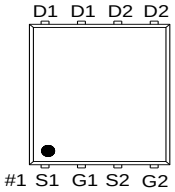
N- & P-Channel Enhancement Mode Field Effect Transistor

PE609CA
PDFN 3x3P
Halogen-Free & Lead-Free

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
N-Channel	40V	25mΩ	18A
P-Channel	-40V	60mΩ	-12A





G. GATE
D. DRAIN
S. SOURCE

100% UIS Tested
100% Rg Tested

Features
- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.

Applications
- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.
- DC Motor for BLDC Applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	N-Channel	P-Channel	UNITS
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current[4]	T_C = 25 °C	I_D	18	-12	A
	T_C = 100 °C		11	-7.4	
	T_A = 25 °C		7.4	-4.9	
	T_A = 70 °C		5.9	-3.9	
Pulsed Drain Current[1]		I_{DM}	53	-44	
Avalanche Current		I_{AS}	14	-21	
Avalanche Energy	L = 0.1mH	E_{AS}	10	22	mJ
Power Dissipation	T_C = 25 °C	P_D	15	16	W
	T_C = 100 °C		6.2	6.4	
Power Dissipation[3]	T_A = 25 °C		2.7	2.7	
	T_A = 70 °C		1.7	1.7	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	N-ch		45	°C / W
			P-ch		45	
Junction-to-Ambient[2]	Steady-State		N-ch		87	
			P-ch		84	
Junction-to-Case	Steady-State	$R_{\theta JC}$	N-ch		8	
			P-ch		7.8	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.
[4]Package limitation current is N-Ch=9A, P-Ch=-9A.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	N-Ch	40			V
		V_{GS} = 0V, I_D = -250μA	P-Ch	-40			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	N-Ch	1.3	1.7	2.3	
		V_{DS} = V_{GS}, I_D = -250μA	P-Ch	-1.3	-1.9	-2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	N-Ch			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS} = 0V	N-Ch			1	μA
		V_{DS} = -32V, V_{GS} = 0V	P-Ch			-1	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 55 °C	N-Ch			10	
		V_{DS} = -30V, V_{GS} = 0V, T_J = 55 °C	P-Ch			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 6A	N-Ch		22	35	mΩ
		V_{GS} = -4.5V, I_D = -4A	P-Ch		57	90	
		V_{GS} = 10V, I_D = 6A	N-Ch		18	25	
		V_{GS} = -10V, I_D = -4A	P-Ch		36	60	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10V, I_D = 6A	N-Ch		30		S
		V_{DS} = -10V, I_D = -4A	P-Ch		10		

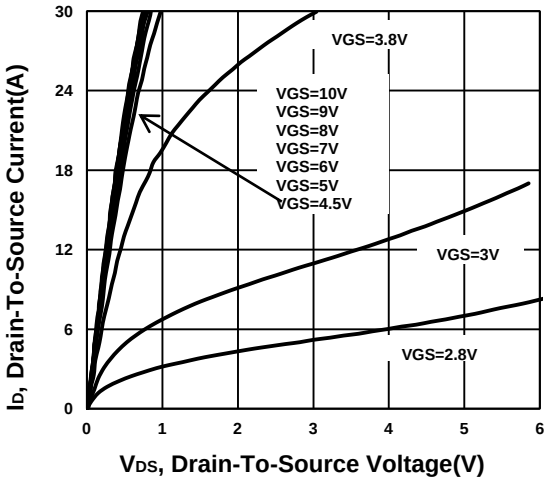
DYNAMIC							
Input Capacitance	C_{iss}	N-Channel V_{GS} = 0V, V_{DS} = 20V, f = 1MHz P-Channel V_{GS} = 0V, V_{DS} = -20V, f = 1MHz	N-Ch P-Ch		453 549		pF
Output Capacitance	C_{oss}		N-Ch P-Ch		64 123		
Reverse Transfer Capacitance	C_{rss}		N-Ch P-Ch		41 73		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	N-Ch P-Ch		4.4 15		Ω
Total Gate Charge[2]	Q_g	N-Channel V_{DS} = 20V , V_{GS} = 10V, I_D = 6A P-Channel V_{DS} = -20V , V_{GS} = -10V, I_D = -4A	N-Ch P-Ch		10 11.7		nC
Gate-Source Charge[2]	Q_{gs}		N-Ch P-Ch		1.2 1.5		
Gate-Drain Charge[2]	Q_{gd}		N-Ch P-Ch		2.7 3.3		
Turn-On Delay Time[2]	$t_{d(on)}$	N-Channel V_{DS} = 20V, $I_D \cong$ 6A, V_{GS} = 10V, R_{GEN} = 6Ω P-Channel V_{DS} = -20V, $I_D \cong$ -4A, V_{GS} = -10V, R_{GEN} = 6Ω	N-Ch P-Ch		9.9 11.4		nS
Rise Time[2]	t_r		N-Ch P-Ch		31 21.5		
Turn-Off Delay Time[2]	$t_{d(off)}$		N-Ch P-Ch		25 58		
Fall Time[2]	t_f		N-Ch P-Ch		39 46		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current[3]	I_S		N-Ch P-Ch			12.5 -13	A
Forward Voltage[1]	V_{SD}	I_F = 6A, V_{GS} = 0V I_F = -4A, V_{GS} = 0V	N-Ch P-Ch			1.2 -1.2	V
Reverse Recovery Time	t_{rr}	I_F = 6A, dI_F/dt = 100A / µS	N-Ch P-Ch		7.9 13.5		nS
Reverse Recovery Charge	Q_{rr}	I_F = -4A, dI_F/dt = 100A / µS	N-Ch P-Ch		1.7 3.1		nC

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Package limitation current is N-Ch=9A, P-Ch=-9A.

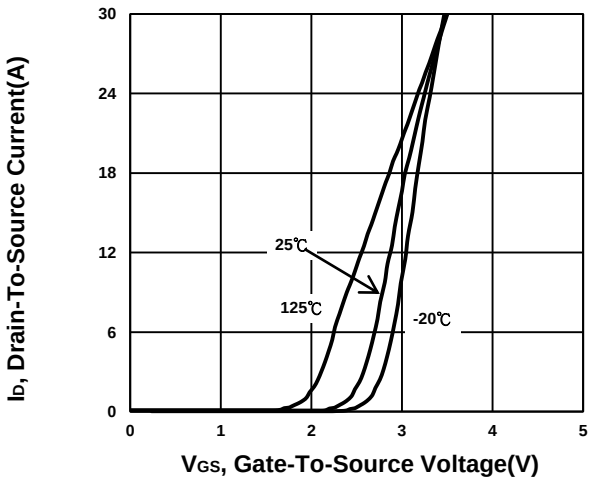
TYPICAL PERFORMANCE CHARACTERISTICS

N-CHANNEL

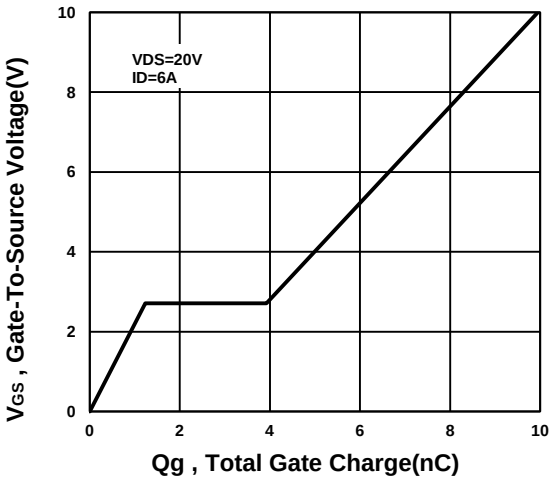
Output Characteristics



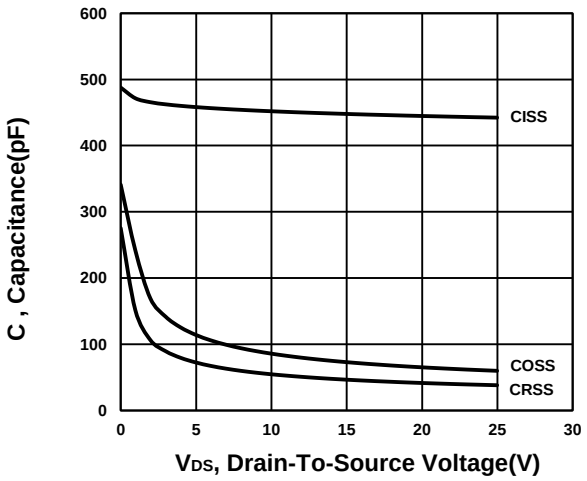
Transfer Characteristics



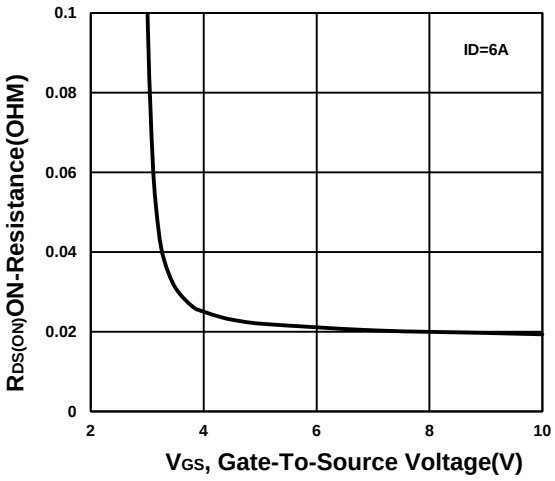
Gate charge Characteristics



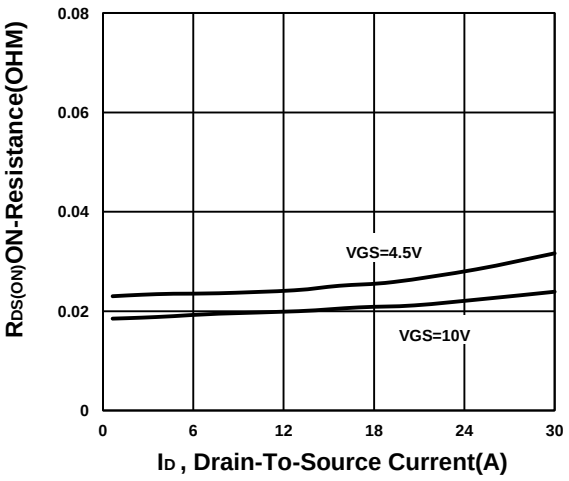
Capacitance Characteristic



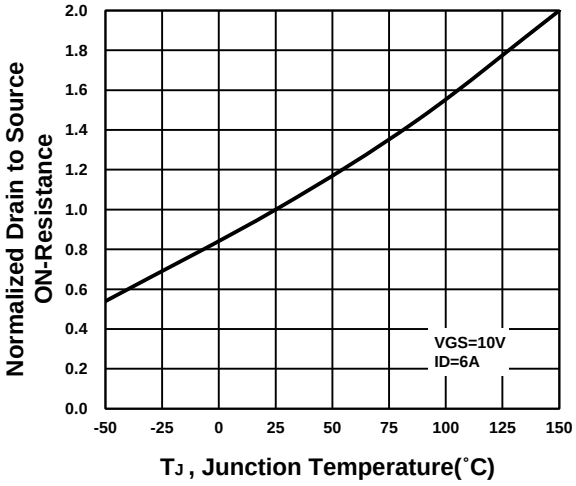
On-Resistance VS Gate-To-Source Voltage



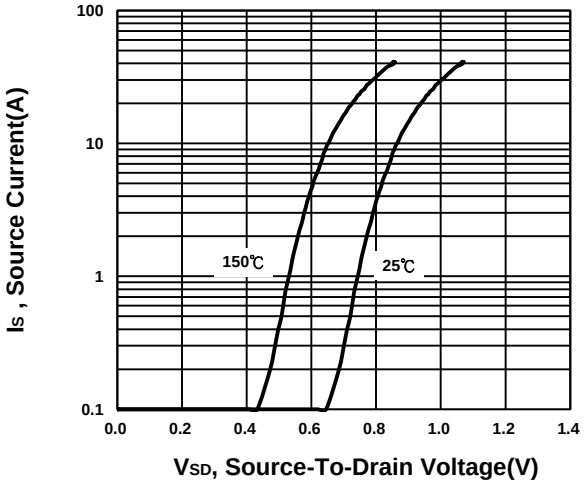
On-Resistance VS Drain Current



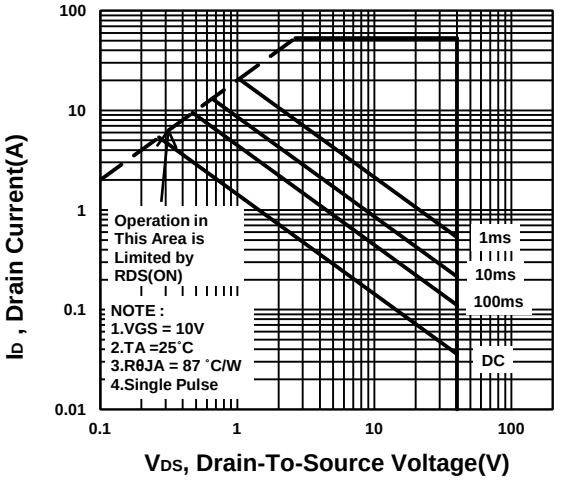
On-Resistance VS Temperature



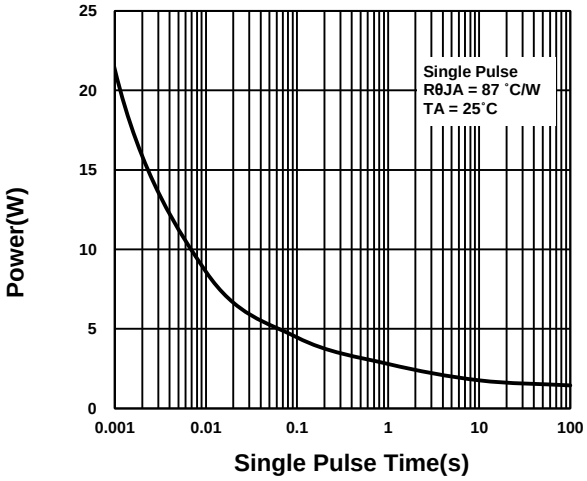
Source-Drain Diode Forward Voltage



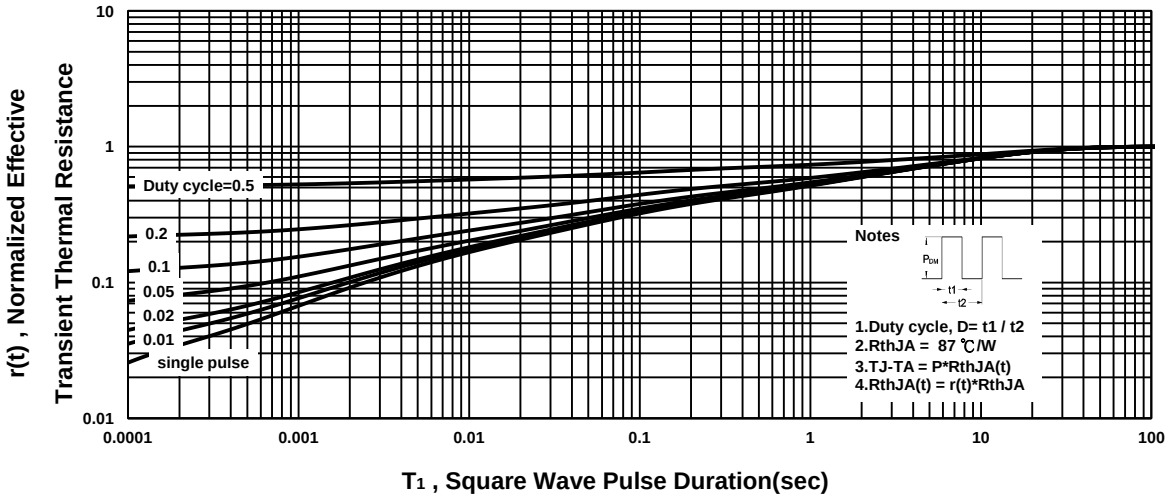
Safe Operating Area



Single Pulse Maximum Power Dissipation

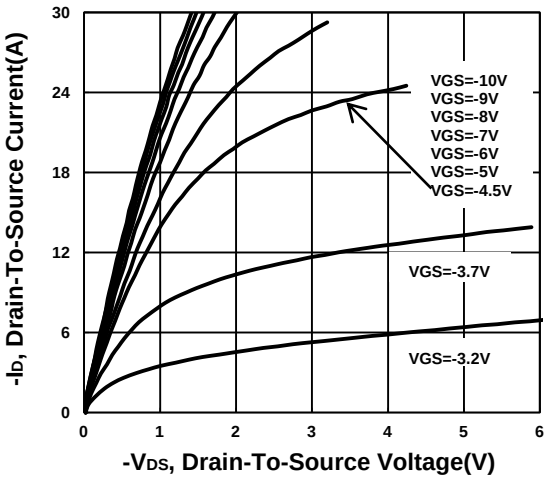


Transient Thermal Response Curve

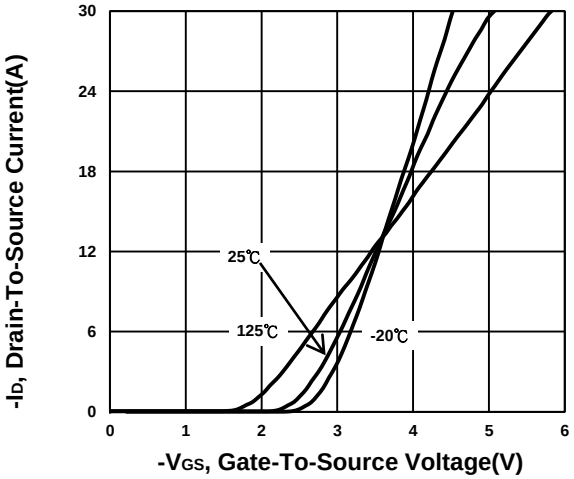


P-CHANNEL

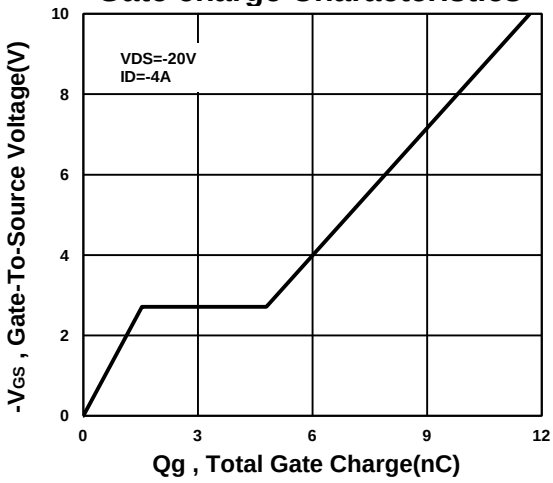
Output Characteristics



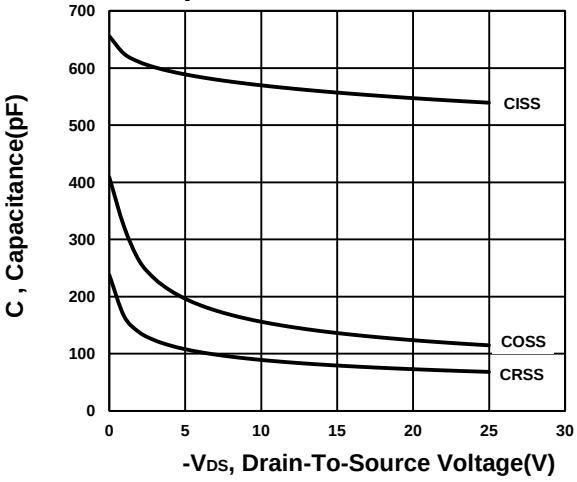
Transfer Characteristics



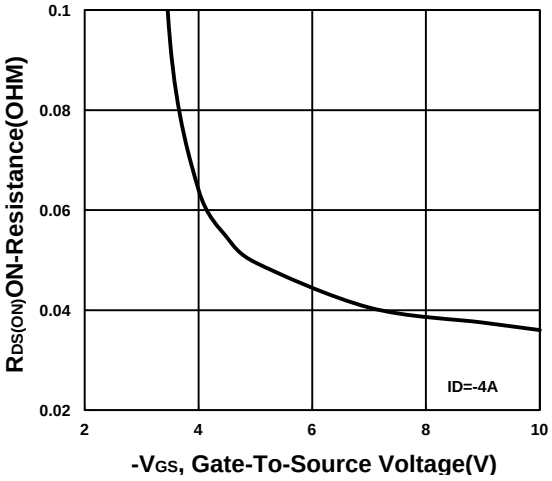
Gate charge Characteristics



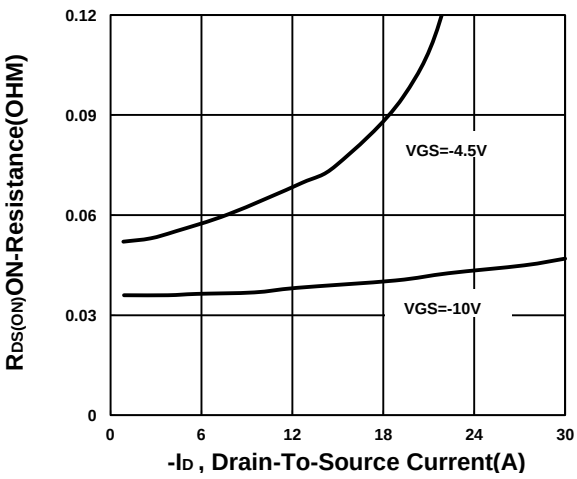
Capacitance Characteristic



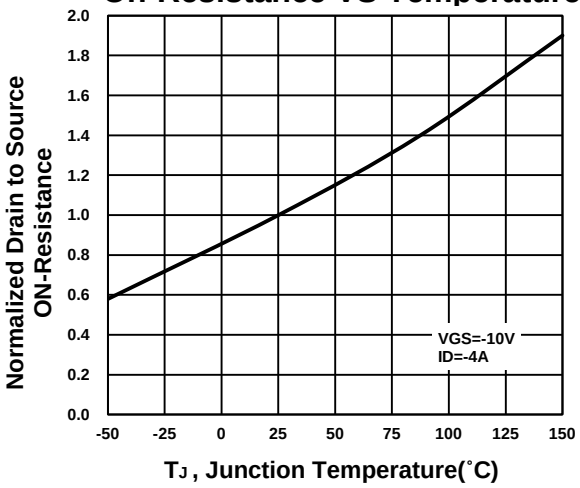
On-Resistance VS Gate-To-Source Voltage



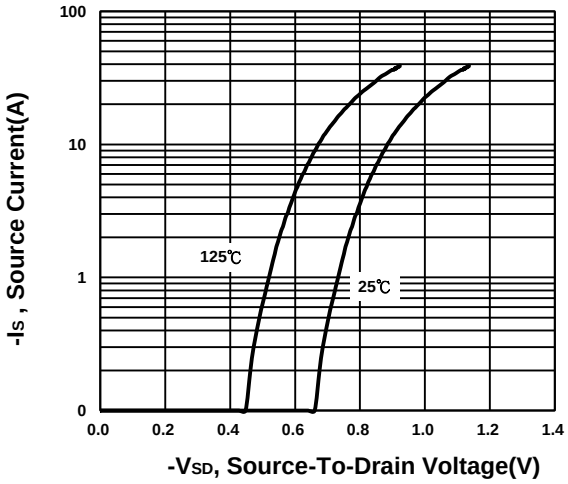
On-Resistance VS Drain Current



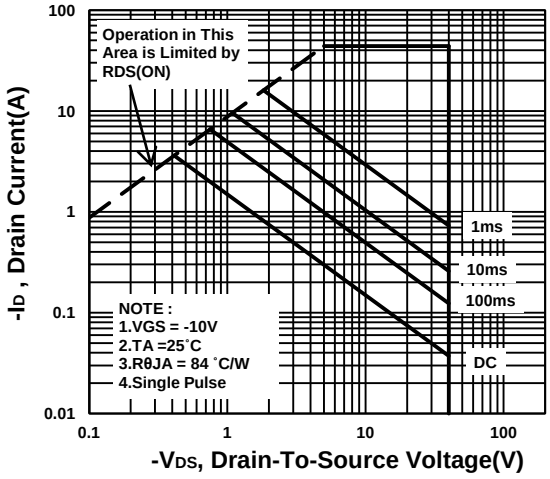
On-Resistance VS Temperature



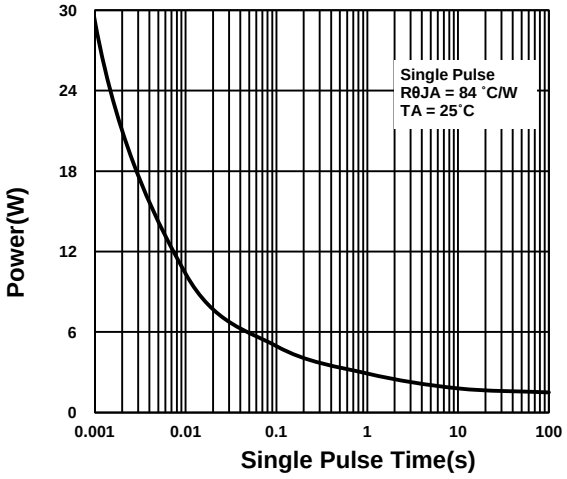
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve