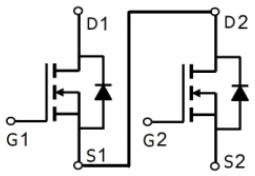
NIKO-SEM

Dual N-Channel Enhancement Mode Field Effect Transistor

PE854DT
PDFN 3x3S
Halogen-Free & Lead-Free

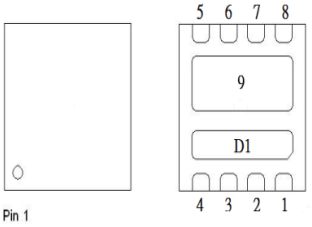
PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
Q2	30V	6.5mΩ	43A
Q1	30V	8mΩ	35A



Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Optimized Gate Charge to Minimize Switching Losses.
- 100% UIS and Rg Tested.



1 : G1
2,3,4 : D1
5,6,7 : S2
8 : G2
9 : S1/D2

Applications

- Protection Circuits Applications.
- Computer for DC to DC Converters Applications.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	Q2	Q1	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	43	35	A
	T_C = 100 °C		27	22	
Pulsed Drain Current[1]		I_{DM}	50	41	
Continuous Drain Current[3]	T_A = 25 °C	I_D	16	13	
	T_A = 70 °C		12	10.5	
Avalanche Current		I_{AS}	25	25	
Avalanche Energy	L = 0.03mH	E_{AS}	9.3	9.3	mJ
Power Dissipation	T_C = 25 °C	P_D	21	17	W
	T_C = 100 °C		8.5	6.9	
Power Dissipation[3]	T_A = 25 °C	P_D	2.8	2.4	W
	T_A = 70 °C		1.8	1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient[2]	t ≦10s	$R_{\theta JA}$	Q2		50	°C / W
			Q1		53	
Junction-to-Ambient[2]	Steady-State	$R_{\theta JA}$	Q2		67	
			Q1		70	
Junction-to-Case		$R_{\theta JC}$	Q2		6.2	
			Q1		6.5	

[1]Pulse width limited by maximum junction temperature $T_{J(MAX)}$=150°C.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
[3]The Power dissipation is based on $R_{\theta JA}$ t ≦10s value.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	Q2	30			V
		V_{GS} = 0V, I_D = 250μA	Q1	30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	Q2	1.3	1.5	2.3	
		V_{DS} = V_{GS}, I_D = 250μA	Q1	1.3	1.5	2.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	Q2			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	Q1			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	Q2			1	μA
		V_{DS} = 30V, V_{GS} = 0V	Q1			1	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 55 °C	Q2			10	
		V_{DS} = 30V, V_{GS} = 0V, T_J = 55 °C	Q1			10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 13A	Q2		7.6	10.5	mΩ
		V_{GS} = 4.5V, I_D = 13A	Q1		8.4	12	
		V_{GS} = 10V, I_D = 13A	Q2		4.9	6.5	
		V_{GS} = 10V, I_D = 13A	Q1		5.6	8	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 13A	Q2		47		S
		V_{DS} = 5V, I_D = 13A	Q1		46		

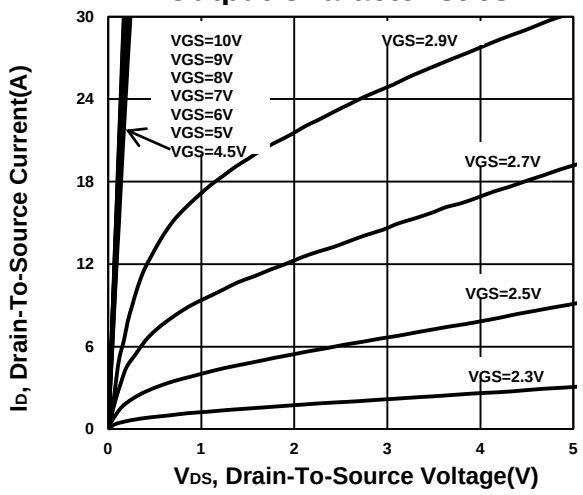
DYNAMIC							
Input Capacitance	C_{iss}	Q2 V_{GS} = 0V, V_{DS} = 15V f = 1MHz Q1 V_{GS} = 0V, V_{DS} = 15V f = 1MHz	Q2		589		pF
			Q1		585		
Output Capacitance	C_{oss}		Q2		324		
			Q1		324		
Reverse Transfer Capacitance	C_{rss}		Q2		36		
			Q1		35		
Gate Resistance	R_g	V_{GS} = 0V, V_{DS} = 0V, f = 1MHz	Q2		2.5		Ω
			Q1		2.5		
Total Gate Charge[2]	Q_g VGS = 10V	Q2 V_{DS} = 15V V_{GS} = 10V, I_D = 13A Q1 V_{DS} = 15V V_{GS} = -10V, I_D = 13A	Q2		10		nC
			Q1		10		
	Q_g VGS = 4.5V		Q2		5.8		
			Q1		5.5		
Gate-Source Charge[2]	Q_{gs}		Q2		1.3		
			Q1		1.5		
Gate-Drain Charge[2]	Q_{gd}		Q2		2.6		
			Q1		2.5		
Turn-On Delay Time[2]	$t_{d(on)}$	Q2 , V_{DS} = 15V $I_D \cong$ 13A V_{GS} = 10V, R_{GEN} =6Ω Q1 , V_{DS} = 15V $I_D \cong$ 13A, V_{GS} = 10V, R_{GEN} =6Ω	Q2		8.9		nS
			Q1		8.4		
Rise Time[2]	t_r		Q2		70		
			Q1		58		
Turn-Off Delay Time[2]	$t_{d(off)}$		Q2		21		
			Q1		19		
Fall Time[2]	t_f		Q2		97		
			Q1		74		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)							
Continuous Current	I_S		Q2			17.5	A
			Q1			14	
Forward Voltage[1]	V_{SD}	I_F = 13A V_{GS} = 0V	Q2			1.2	V
		I_F = 13A, V_{GS} = 0V	Q1			1.2	
Reverse Recovery Time	t_{rr}	Q2 I_F = 13A dI_F/dt = 100A / µS Q1 I_F = 13A, dI_F/dt = 100A / µS	Q2		14		nS
			Q1		14		
Reverse Recovery Charge	Q_{rr}		Q2		4.3		nC
			Q1		4.2		

[1]Pulse test : Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

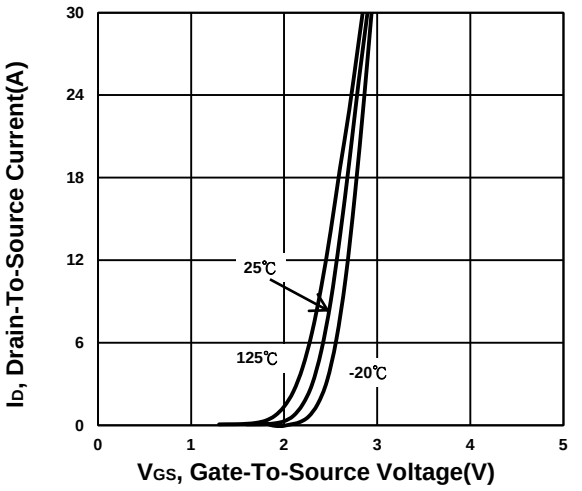
TYPICAL PERFORMANCE CHARACTERISTICS

Q2

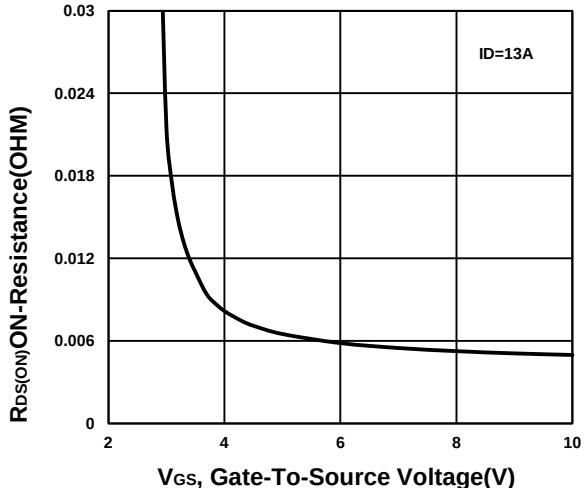
Output Characteristics



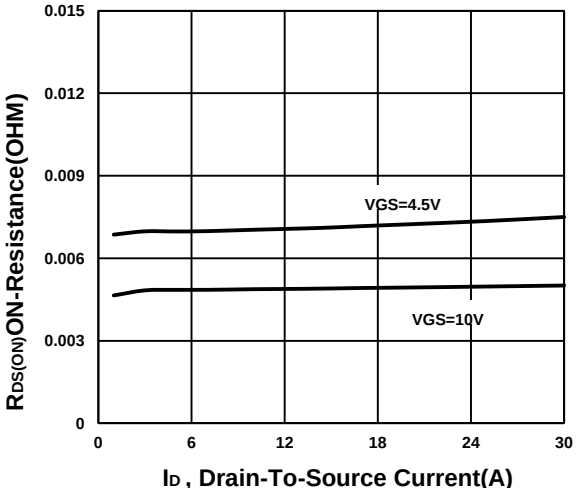
Transfer Characteristics



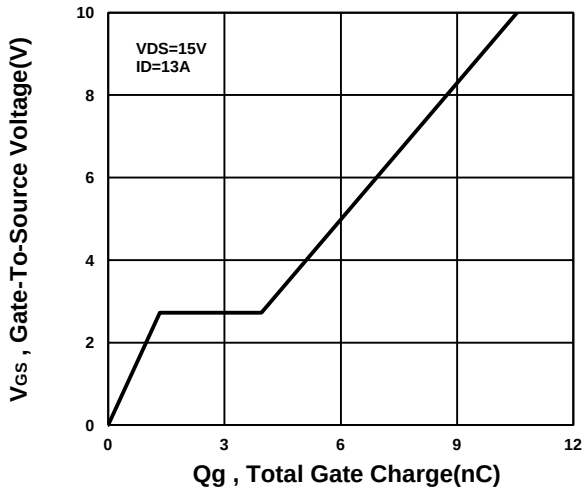
On-Resistance VS Gate-To-Source Voltage



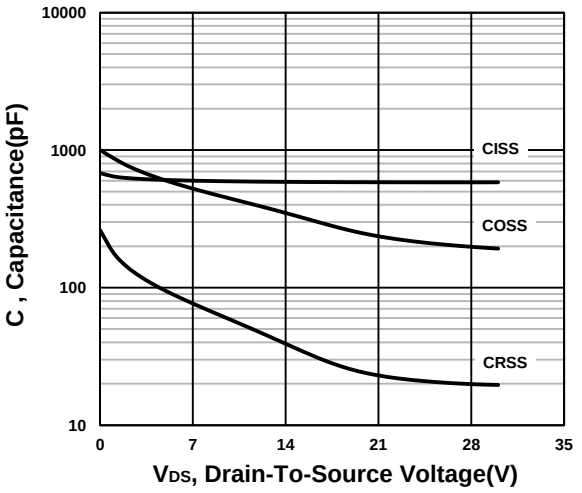
On-Resistance VS Drain Current



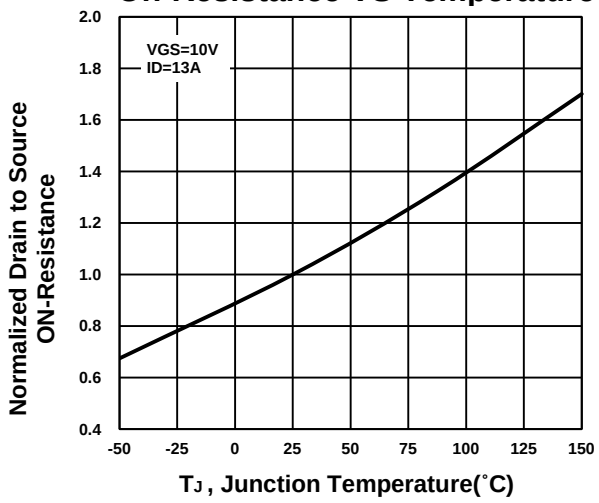
Gate charge Characteristics



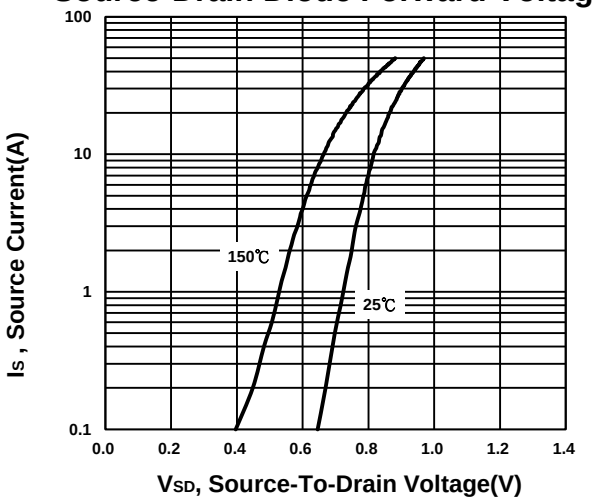
Capacitance Characteristic



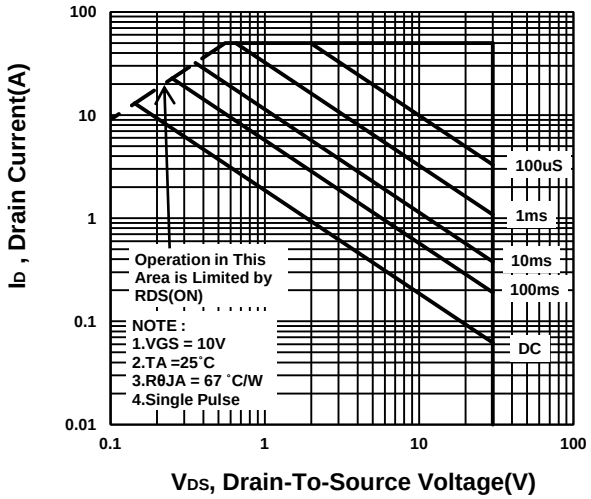
On-Resistance VS Temperature



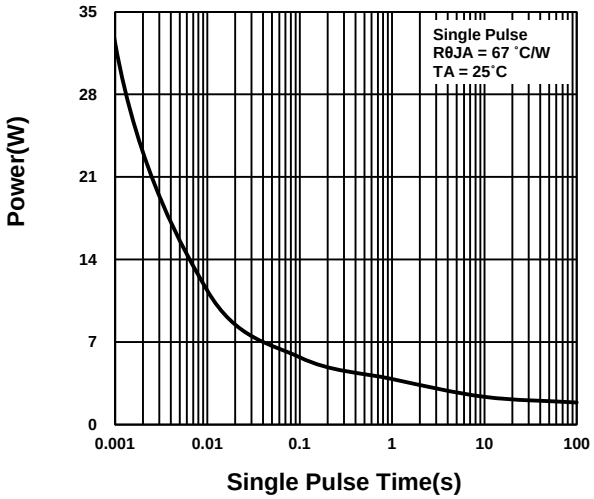
Source-Drain Diode Forward Voltage



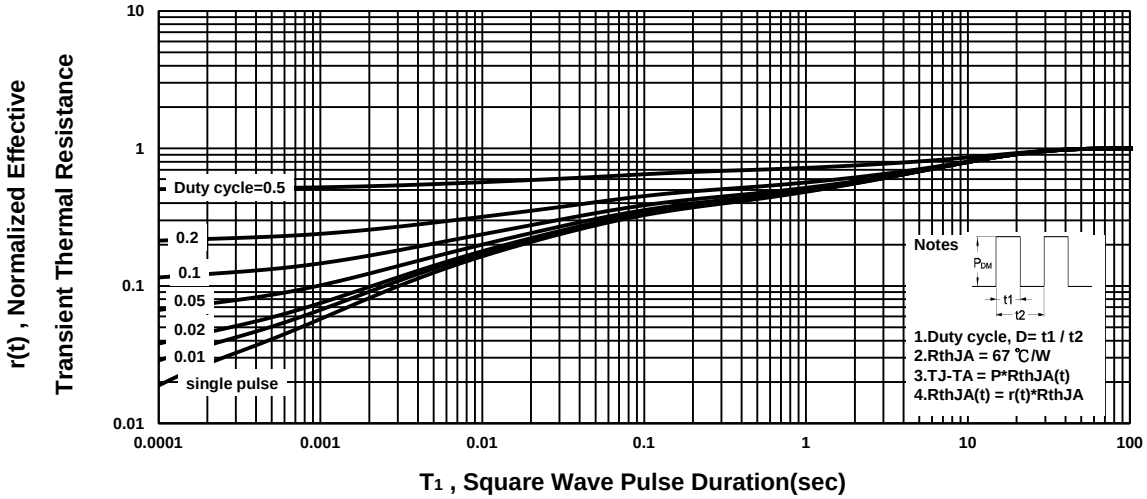
Safe Operating Area



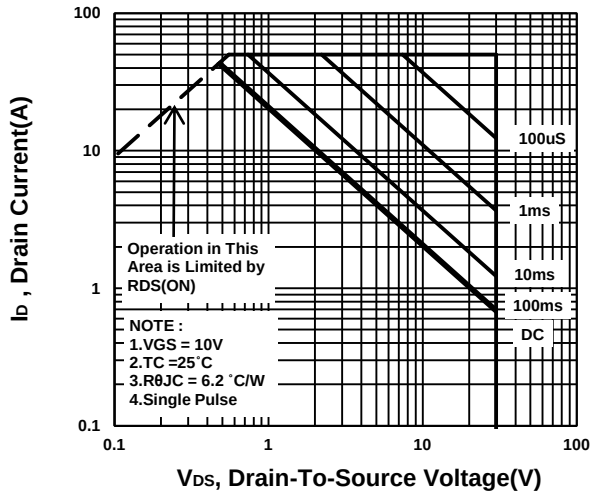
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Safe Operating Area



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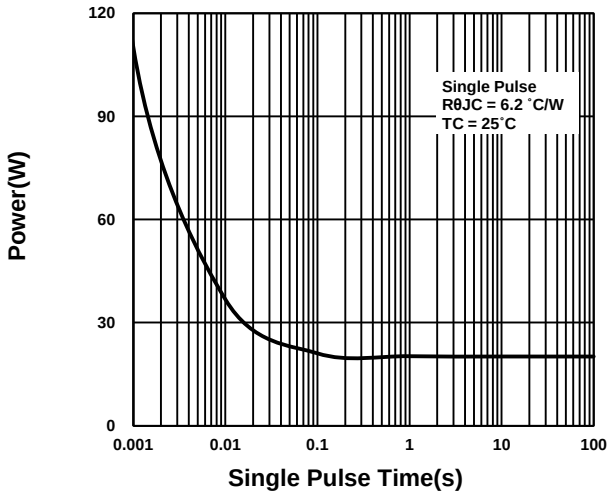
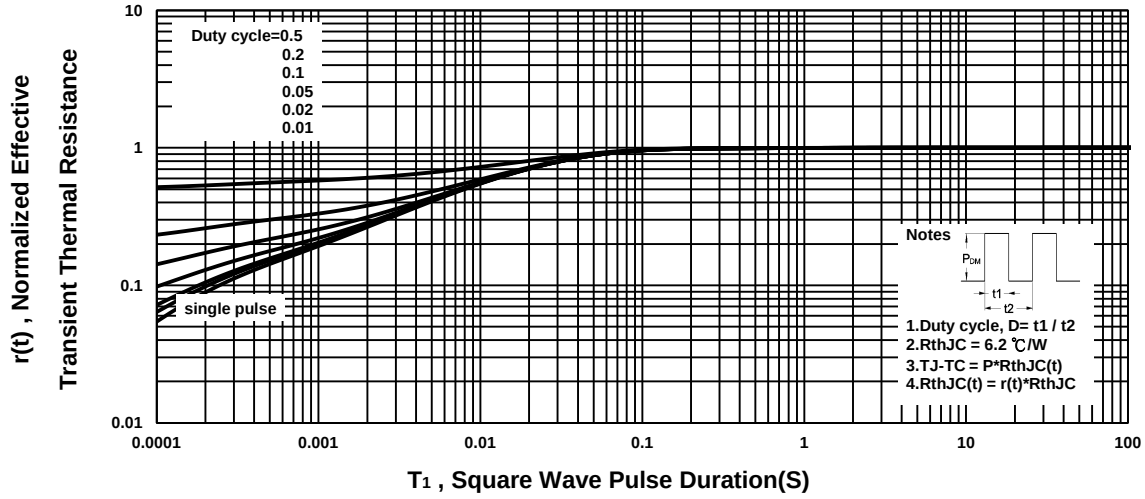
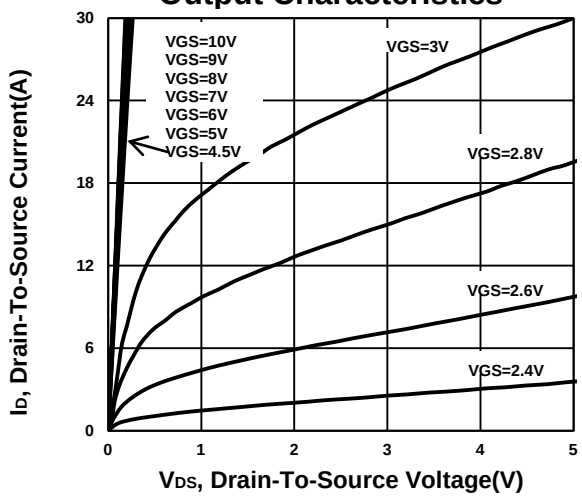


Transient Thermal Response Curve

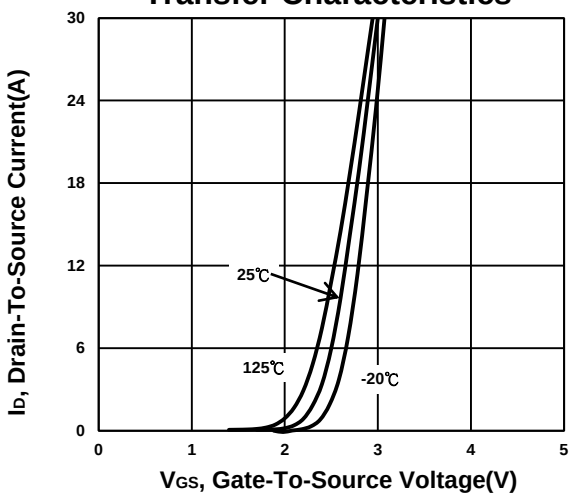


Q1

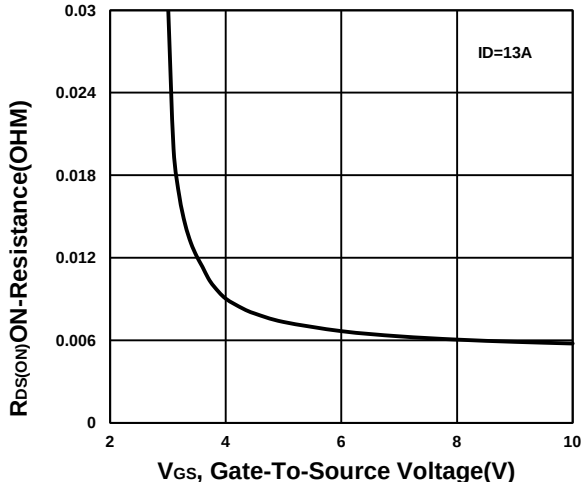
Output Characteristics



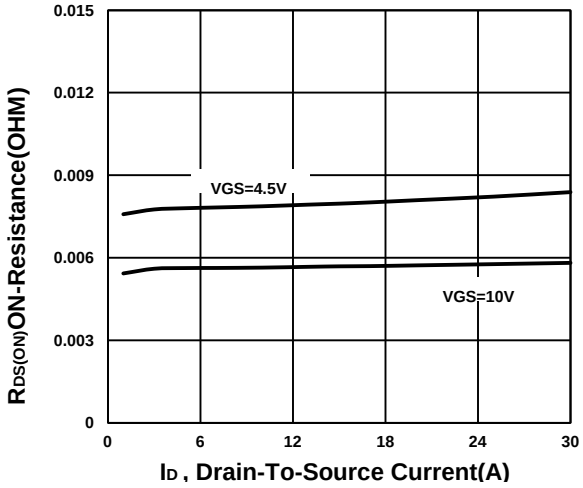
Transfer Characteristics



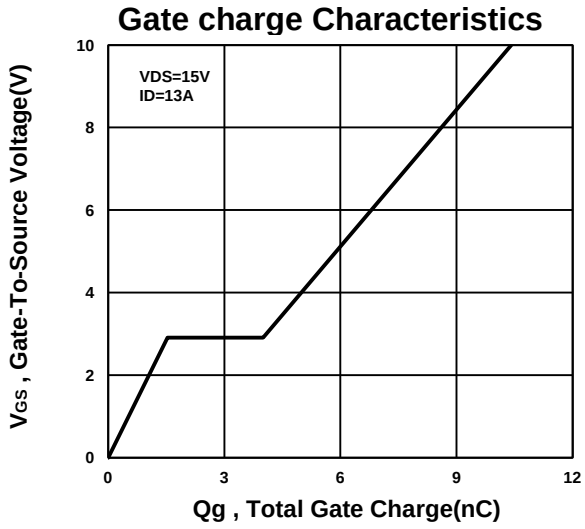
On-Resistance VS Gate-To-Source Voltage



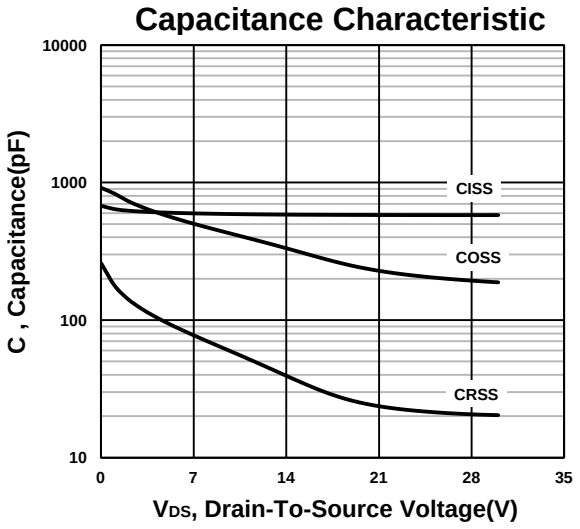
On-Resistance VS Drain Current



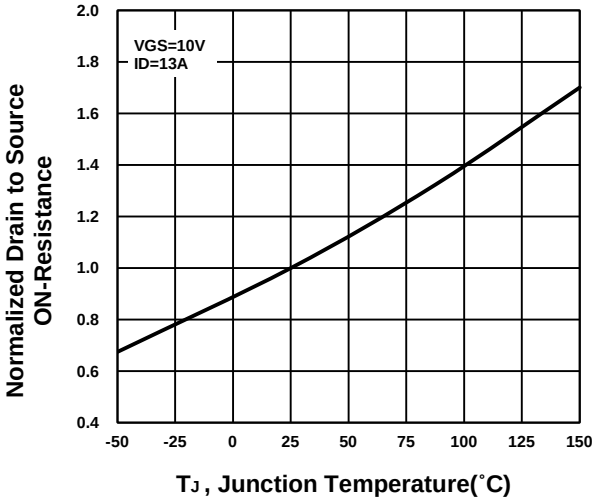
Gate charge Characteristics



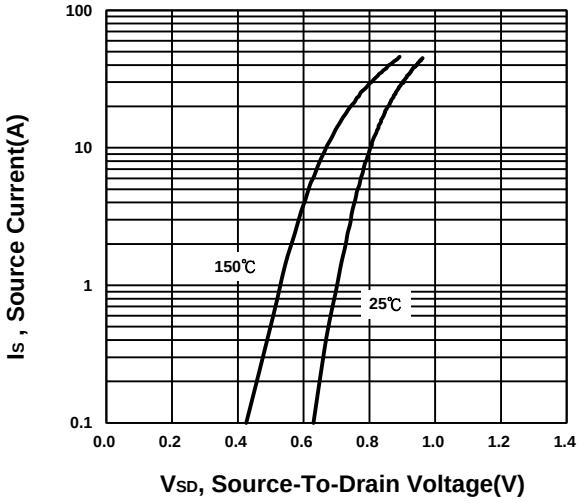
Capacitance Characteristic



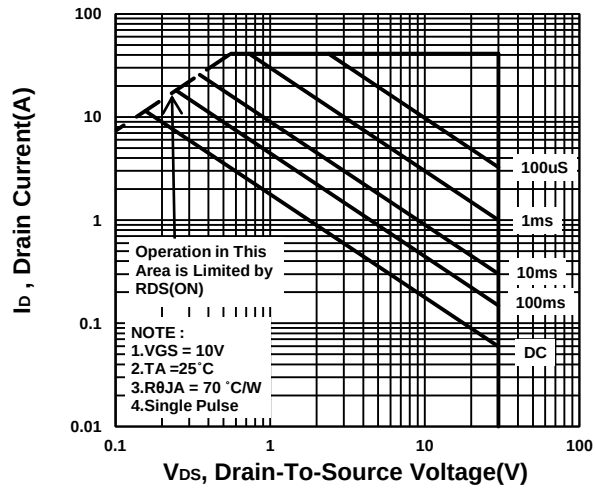
On-Resistance VS Temperature



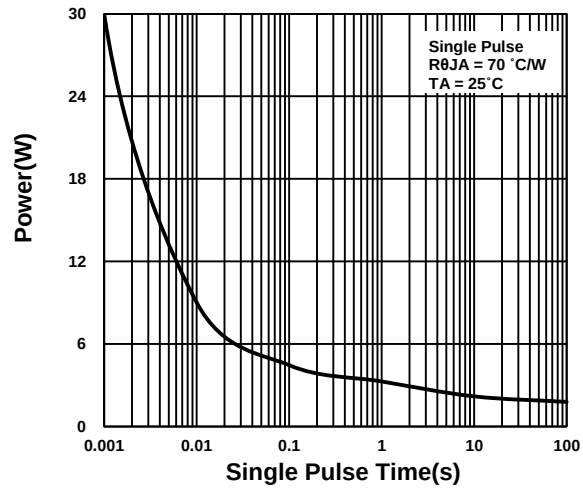
Source-Drain Diode Forward Voltage



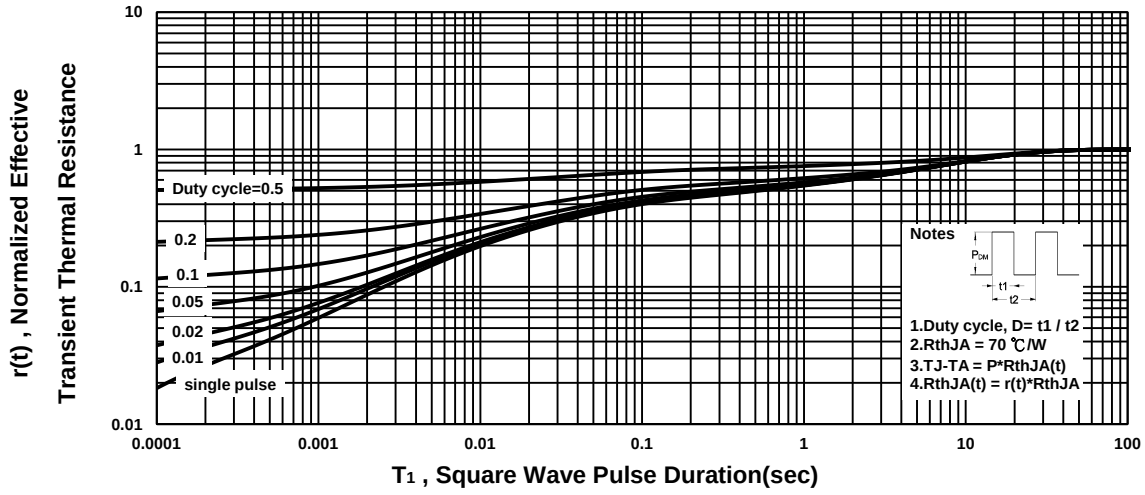
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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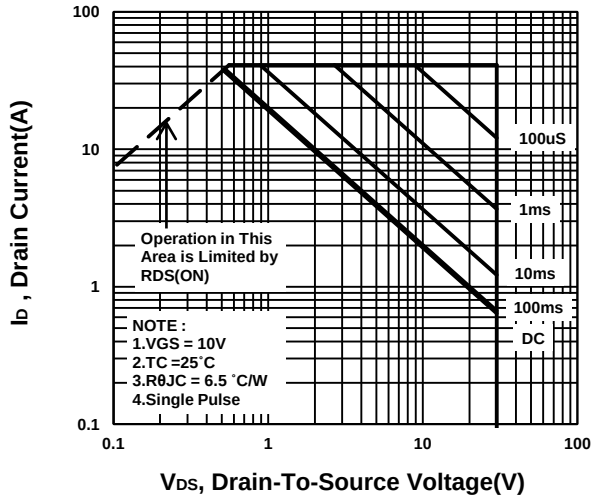

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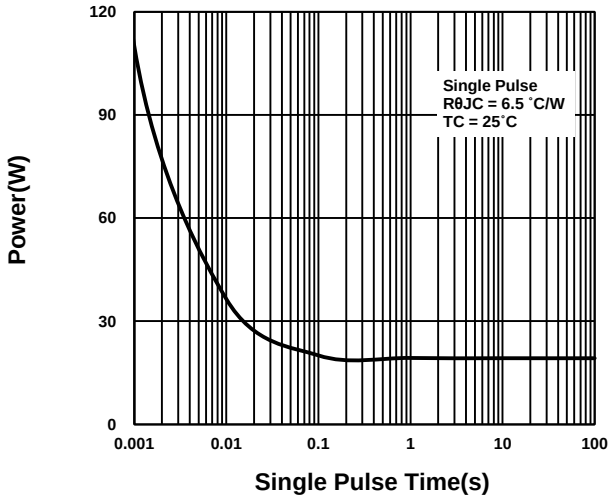

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