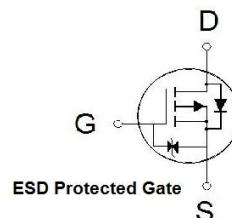


NIKO-SEM**P-Channel Logic Level Enhancement
Mode Field Effect Transistor****PZ5203EMAA**
SOT-23(S)
Halogen-Free & Lead-Free**PRODUCT SUMMARY**

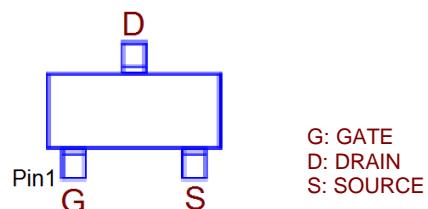
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-30V	60mΩ	-2.8A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- Products Integrated ESD diode with ESD Protected up to 2KV.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.

**ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_A = 25^\circ C$	I_D	-2.8	A
$T_A = 70^\circ C$	I_D	-2.2	
Pulsed Drain Current ¹	I_{DM}	-20	
Power Dissipation $T_A = 25^\circ C$	P_D	0.8	W
$T_A = 70^\circ C$	P_D	0.5	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

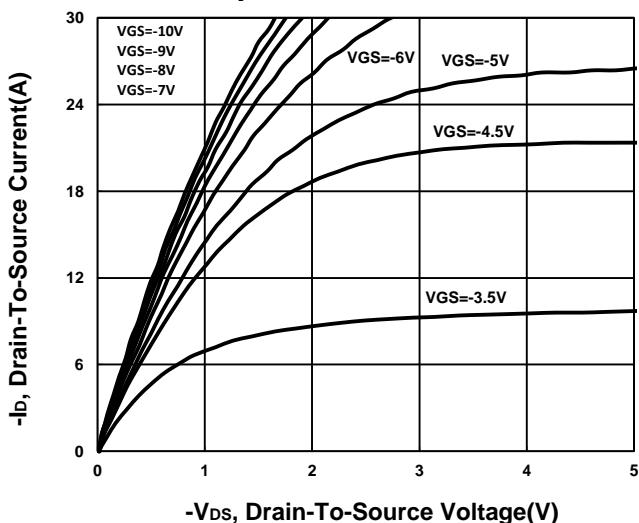
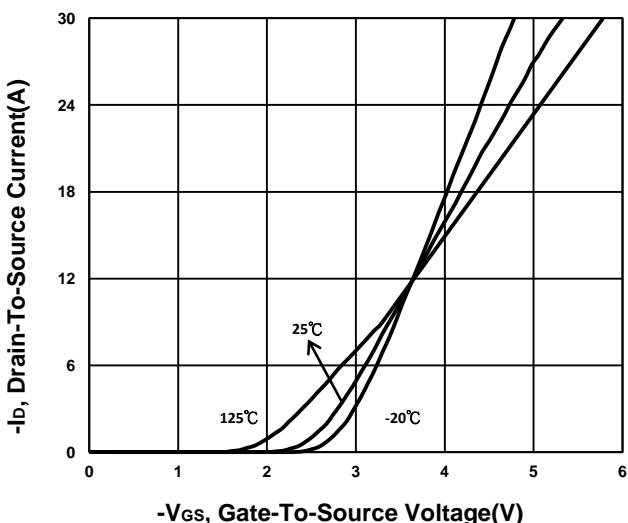
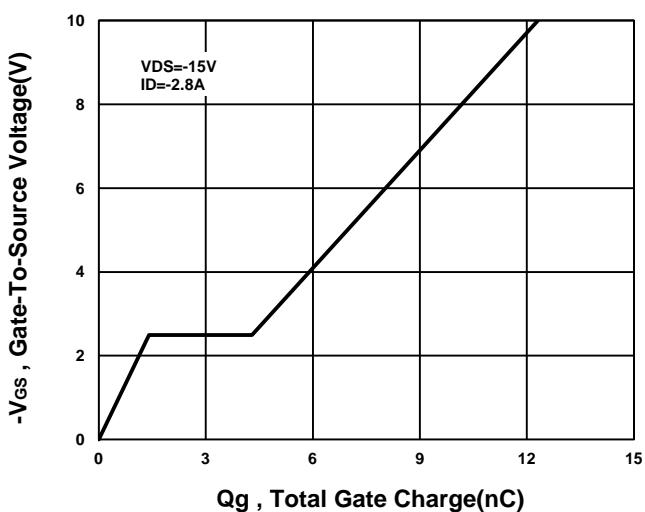
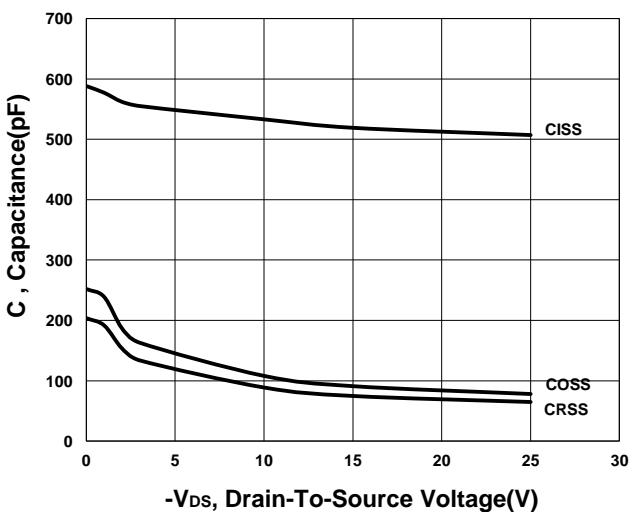
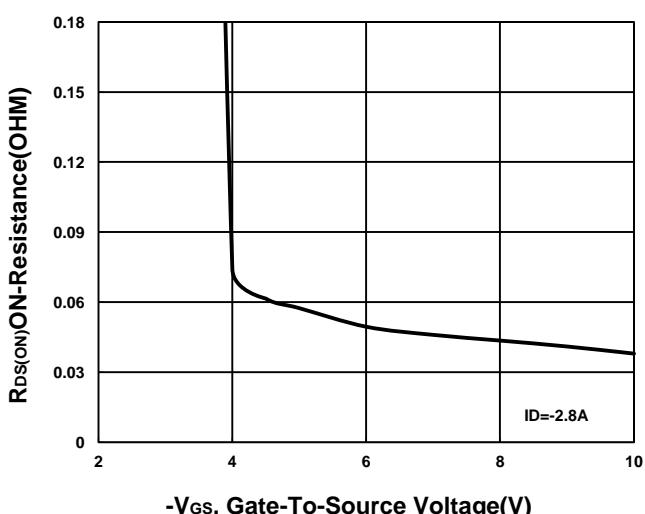
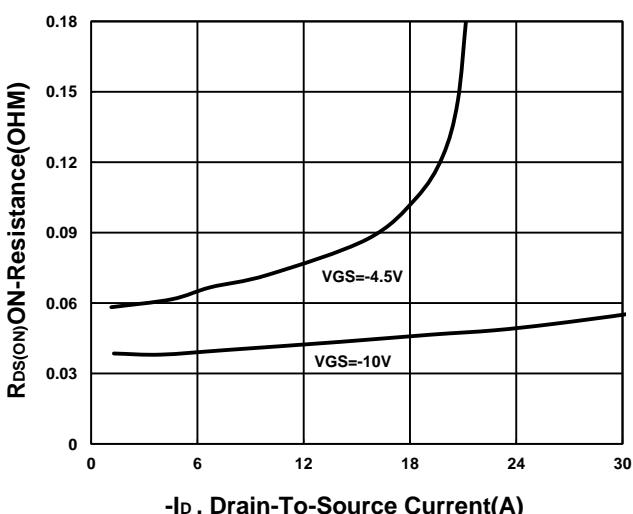
THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		162	°C/W

¹Pulse width limited by maximum junction temperature.²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$. The value in any given application depends on the user's specific board design.

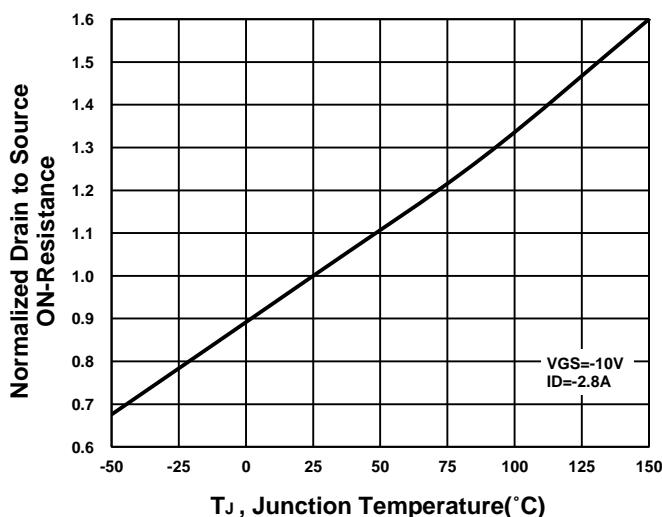
NIKO-SEM**P-Channel Logic Level Enhancement
Mode Field Effect Transistor****PZ5203EMAA**
SOT-23(S)
Halogen-Free & Lead-Free**ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ C$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.3	-1.65	-2.3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 16V$			± 30	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 55^\circ C$			-10	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -2.8A$		70	90	$m\Omega$
		$V_{GS} = -10V, I_D = -2.8A$		52	60	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -2.8A$		9		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		521		pF
Output Capacitance	C_{oss}			92		
Reverse Transfer Capacitance	C_{rss}			76		
Total Gate Charge ²	Q_g	$V_{DS} = -15V, V_{GS} = -10V, I_D = -2.8A$		12.3		nC
Gate-Source Charge ²	Q_{gs}			1.4		
Gate-Drain Charge ²	Q_{gd}			2.9		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = -15V, I_D \approx -2.8A, V_{GS} = -10V, R_{GS} = 6\Omega$		12		nS
Rise Time ²	t_r			21		
Turn-Off Delay Time ²	$t_{d(off)}$			52		
Fall Time ²	t_f			32		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)						
Continuous Current	I_S				-0.7	A
Forward Voltage ¹	V_{SD}	$I_F = -2.8A, V_{GS} = 0V$			-1.1	V
Reverse Recovery Time	t_{rr}	$I_F = -2.8A, dI_F/dt = 100 A/\mu s$		13.5		nS
Reverse Recovery Charge	Q_{rr}			5		uC

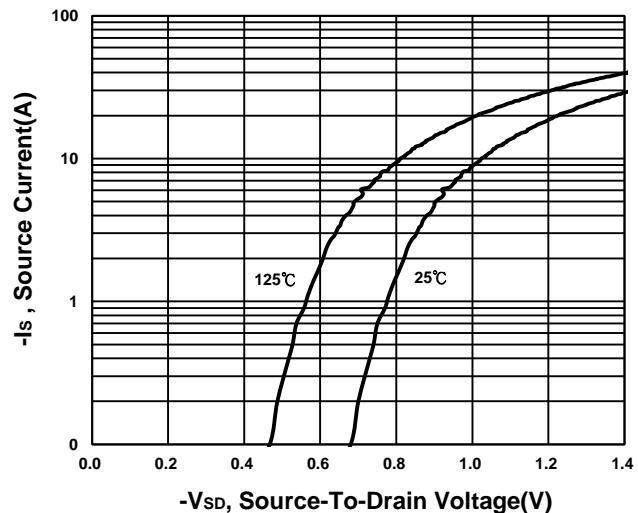
¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

Output Characteristics**Transfer Characteristics****Gate charge Characteristics****Capacitance Characteristic****On-Resistance VS Gate-To-Source****On-Resistance VS Drain Current**

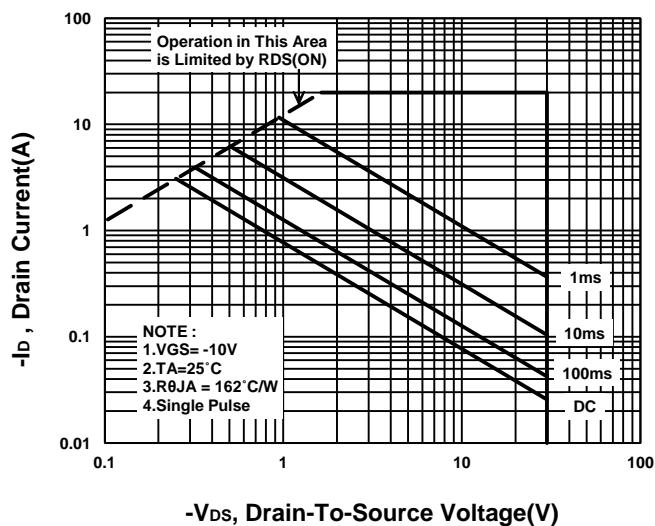
On-Resistance VS Temperature



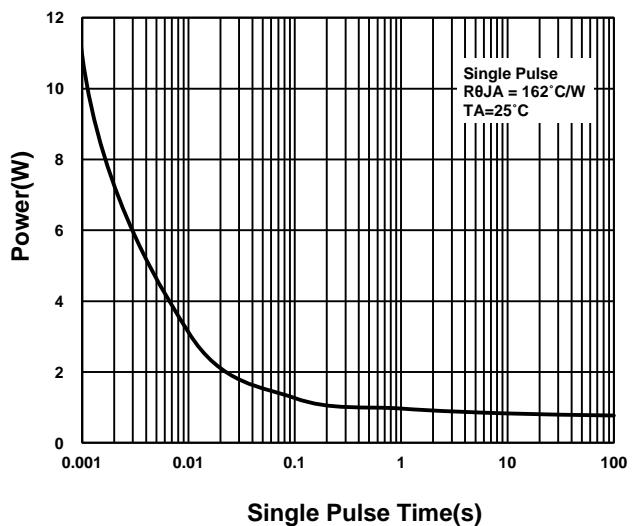
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

