

500mA Low Noise LDO with Soft-Start and Output Discharge Function

Description

The FP6142 is a family of CMOS low dropout (LDO) regulators with a low dropout voltage of 250mV at 500mA designed for noise-sensitive portable device, RF and wireless applications. Quiescent current of FP6142 is as low as 50μA and it works with low-ESR ceramic capacitors, which makes it very suitable for space sensitive handheld applications. The soft-start function will eliminate current surges during start-up and the output discharge function will dissipate the residue output voltage in the capacitor during shut-down.

Other features include current limit, thermal protection, high output accuracy, and low noise output etc..

The FP6142 is available in both SOT-23-5 and SC-70-5 packages.

Features

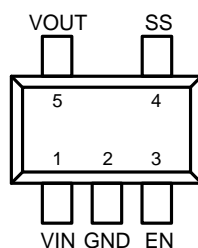
- Ultra-Low Dropout Voltage of 250mV at 500mA
- Wide Operating Voltage Ranges from 2.2V to 5.5V
- Low Quiescent Current at 50μA
- Programmable Soft Start
- 5mA Discharge Current of V_{OUT} when IC Shutdown
- Low Output Noise
- Fast Response in Line/Load Transient
- Current Limit Protection
- Thermal Shutdown Protection
- 1μF Output Capacitor Required for Stability
- RoHS Compliant

Applications

- Digital Still Camera
- CDMA/GSM Cellular-Handset
- Portable Information Appliance
- Laptop, Palmtop and Notebook Computer
- Mini PCI, PCI-Express and PCMCIA Card

Pin Assignments

S5 Package (SOT-23-5)



C5 Package (SC-70-5)

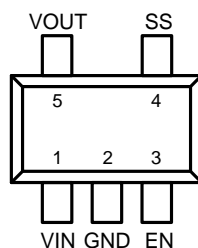
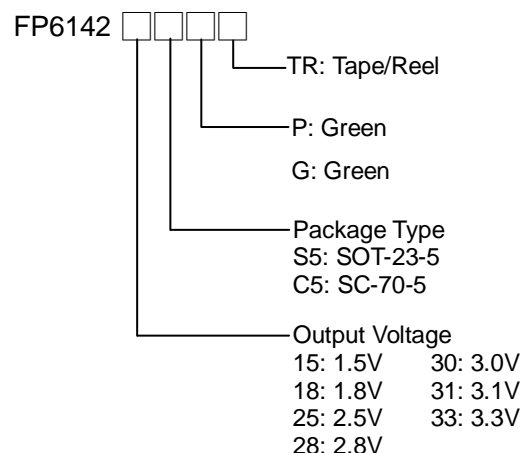


Figure 1. FP6142 Pin Assignments

Ordering Information



Note: Please consult Fitipower sales office or authorized distributors for availability of special output voltages.

SOT-23-5 Marking

Part Number	Product Code	Part Number	Product Code
FP6142-15S5P	Da	FP6142-28S5G	v0=
FP6142-15S5G	Da=	FP6142-30S5P	De
FP6142-18S5P	Db	FP6142-30S5G	De=
FP6142-18S5G	Db=	FP6142-31S5P	Df
FP6142-25S5P	Dd	FP6142-31S5G	Df=
FP6142-25S5G	Dd=	FP6142-33S5P	w0
FP6142-28S5P	v0	FP6142-33S5G	w0=

SC-70-5 Marking

Part Number	Product Code	Part Number	Product Code
FP6142-15C5P	Dm	FP6142-28C5G	x0=
FP6142-15C5G	Dm=	FP6142-30C5P	Ds
FP6142-18C5P	Dn	FP6142-30C5G	Ds=
FP6142-18C5G	Dn=	FP6142-31C5P	Dt
FP6142-25C5P	Dr	FP6142-31C5G	Dt=
FP6142-25C5G	Dr=	FP6142-33C5G	z0=

Typical Application Circuit

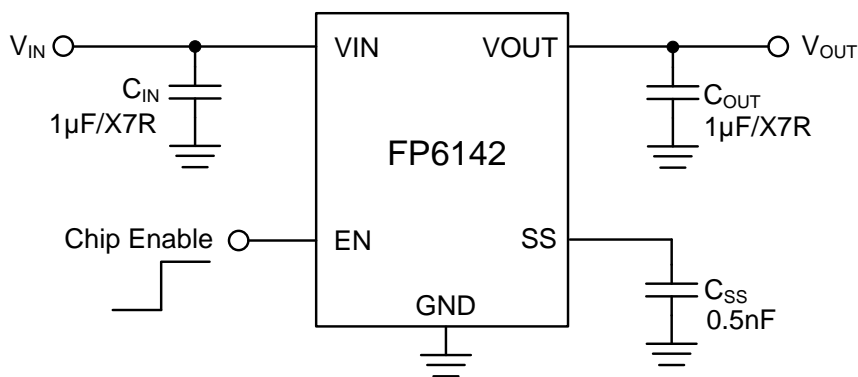


Figure 2. Typical Application Circuit for FP6142

Note 1 : To prevent oscillation, it is recommended to use minimum 1μF X7R or X5R dielectric capacitors if ceramics are used as input/output capacitors.

Functional Pin Description

Pin Name	Pin No.	Pin Function
VIN	1	Supply Voltage.
GND	2	Ground.
EN	3	Chip Enable Control Input. Pull the pin high to enable IC, and pull low or keep it floating to disable the device.
SS	4	Soft Start Pin.
VOUT	5	LDO Output.

Block Diagram

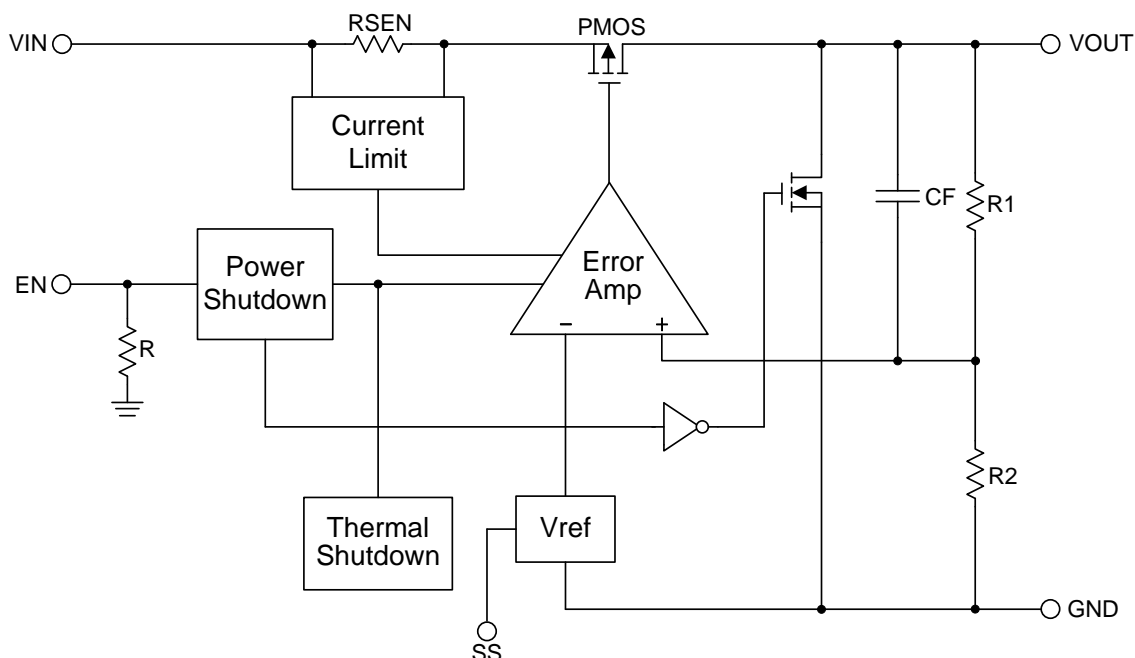


Figure 3. Block Diagram of FP6142

Absolute Maximum Ratings

- V_{IN} , EN, SS to GND ----- +6V
- Power Dissipation @25°C, (P_D)
 - SOT-23-5 ----- +0.4W
 - SC-70-5 ----- +0.3W
- Package Thermal Resistance, (θ_{JA})
 - SOT-23-5 ----- +250°C/W
 - SC-70-5 ----- +333°C/W
- Maximum Junction Temperature ----- +150°C
- Storage Temperature Range (T_{STG}) ----- -65°C to +150°C
- Lead Temperature (Soldering, 10sec) ----- +260°C

Note 2 : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{IN}) ----- +2.2V to +5.5V
- Operating Temperature Range ----- -40°C to +85°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 0.5V$, $V_{EN} = V_{IN}$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Input Voltage Range	V _{IN}			2.2		5.5	V
Output Voltage Accuracy	ΔV _{OUT}	I _L = 10mA		-2		+2	%
Quiescent Current	I _Q	V _{EN} =5V, I _{OUT} =0mA			50	75	μA
Standby Current	I _{STBY}	V _{EN} =0V			0.7	1.5	μA
Current Limit	I _{LIM}	R _{LOAD} =0Ω, 2.7V ≤ V _{IN} ≤ 5.5V		0.5	0.8		A
Dropout Voltage (Note3)	V _{DROP}	I _O =250mA	V _{OUT} =1.5V		360	430	mV
			V _{OUT} =1.8V		280	340	
			V _{OUT} =2.5V		150	180	
			V _{OUT} =3.0V		140	165	
			V _{OUT} =3.3V		120	145	
		I _O =500mA	V _{OUT} =1.5V		700	840	
			V _{OUT} =1.8V		550	660	
			V _{OUT} =2.5V		290	350	
			V _{OUT} =3.0V		270	320	
			V _{OUT} =3.3V		240	290	
Load Regulation (Note4)	ΔV _{LOAD}	1mA< I _{OUT} < 500mA, 2.7V ≤ V _{IN} ≤ 5.5V				1	%
Soft Start Time		C _{SS} =1nF, C _{OUT} =1μF			0.7	1	ms
EN Threshold		Output on		1.5			V
		Output off				0.6	
Enable Pin Current	I _{EN}			0.1	1	5	μA
Output Noise Voltage (Note5)	V _{ON}	C _{OUT} =1μF, I _{OUT} =0mA, C _{SS} =1nF			40		μV _{RMS}
Power Supply Ripple Rejection (Note5)	PSRR	I _{OUT} =10mA, f ≈10kHz			60		dB
Line Regulation	ΔV _{LINE}	V _{IN} = (V _{OUT} + 0.5V) to 5.5V, I _{OUT} = 1mA			0.01	0.2	%/V
Thermal Shutdown Threshold (Note5)	T _{SD}				170		°C
	Δ T _{SD}	Hysteresis			30		

Note 3 : The dropout voltage is defined as $V_{IN}-V_{OUT}$, which is measured when V_{OUT} drops 2% of its normal value with the specified output current.

Note 4 : Load regulation and dropout voltage are measured at a constant junction temperature by using a 40ms low duty cycle current pulse.

Note 5 : Guarantee by design.

Typical Performance Curves

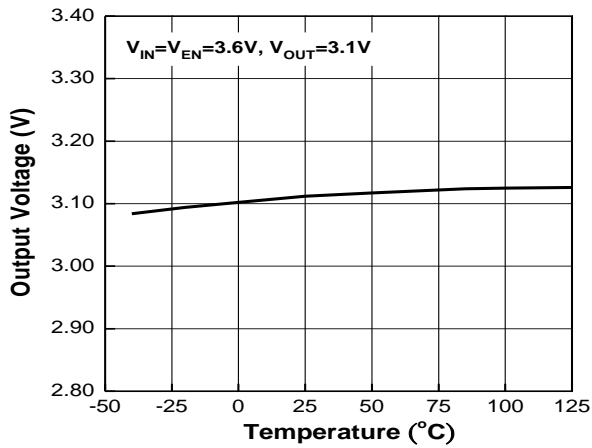


Figure 4. Output Voltage vs. Temperature

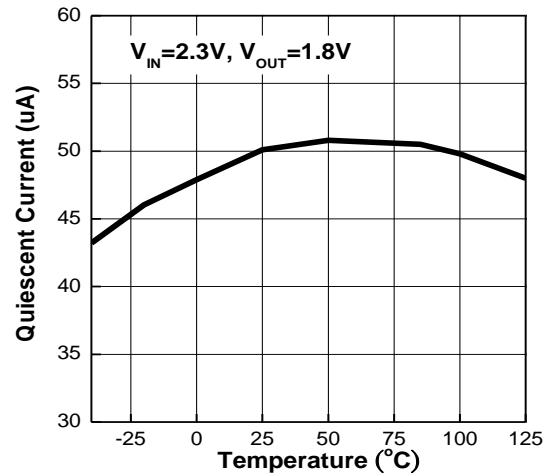


Figure 5. Quiescent Current vs. Temperature

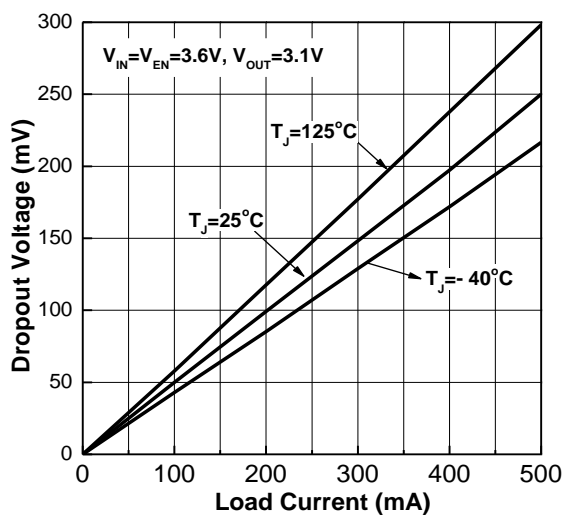


Figure 6. Dropout Voltage vs. Load Current

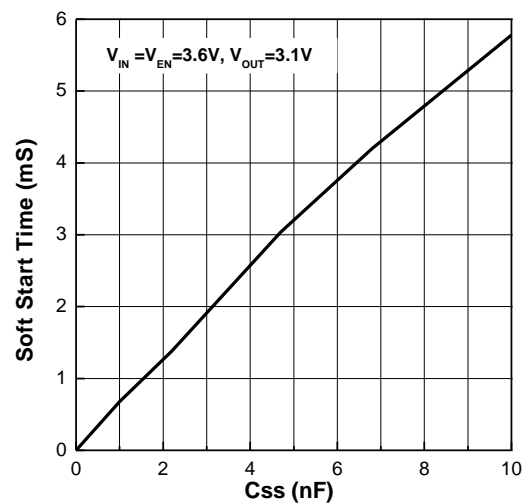


Figure 7. Soft Start Time vs. SS capacitance

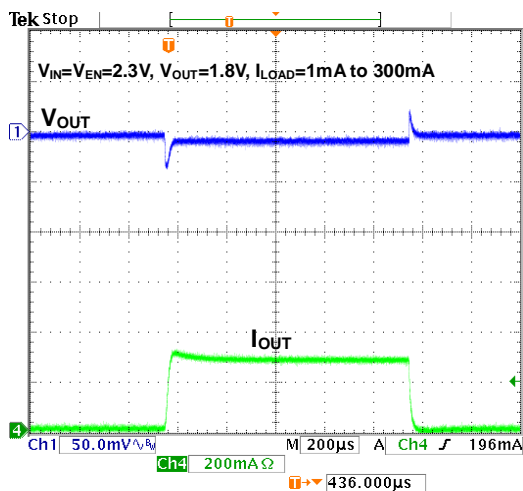


Figure 8. Load Transient Response

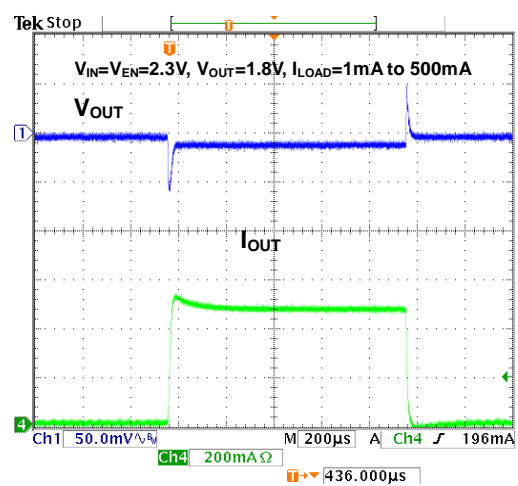


Figure 9. Load Transient Response

Typical Performance Curves (Continued)

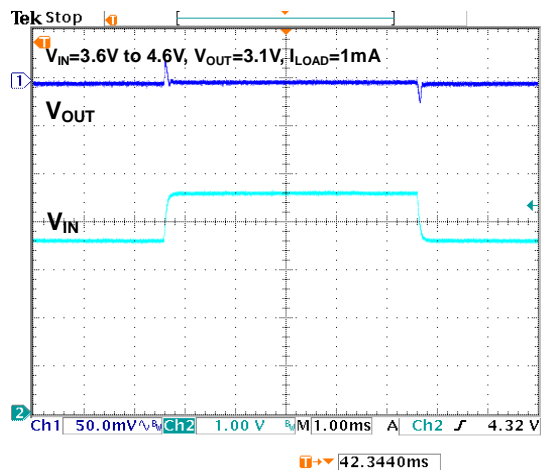


Figure 10. Line Transient Response

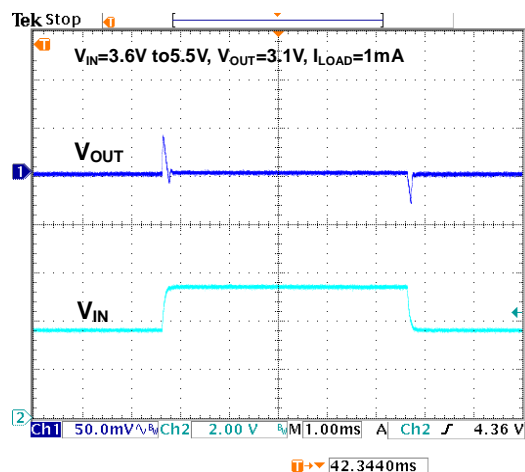


Figure 11. Line Transient Response

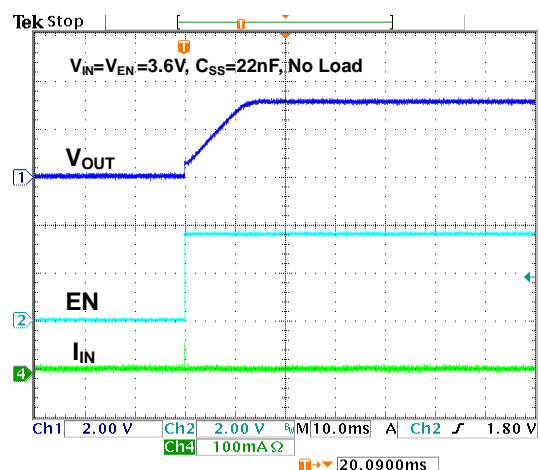


Figure 12. Start-up Response

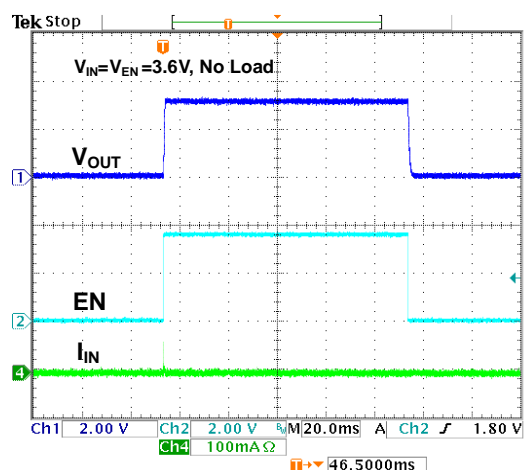


Figure 13. EN Shutdown Response

Applications Information

The FP6142 is a low-noise, low-dropout, low-quiescent current linear regulator designed for space-restricted applications. These devices can supply loads up to 500mA. As shown in the block diagram, the FP6142 consists of a highly accurate band gap core, noise bypass circuit, error amplifier, P-channel pass transistor, soft start, fast discharge and an internal feedback voltage divider. The band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass transistor gate will be pulled low. This allows more current to pass to the output and increases the output voltage. If the feedback voltage is too high, the pass transistor gate will be pulled high, allowing less current to pass to the output. The output voltage is feedback through an internal resistor voltage divider connected to the VOUT pin. Additional blocks include a current limit, over temperature protection and shutdown logic. Besides, current limit and on chip thermal shutdown features provide protection against any combination of over-load or ambient temperature that could cause junction temperature exceeding maximum rating.

Output and Input Capacitor

The FP6142 regulator is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability. Larger value of the output capacitor decreases the peak deviations and improves transition response for larger current changes.

The capacitor types (aluminum, ceramic and tantalum) have different characterizations, such as temperature and voltage coefficients. All ceramic capacitors were manufactured with a variety of dielectrics, each with different behavior across temperature and applications. Common dielectrics used are X5R, X7R and Y5V. It is recommended to use 1.0 μ F to 4.7 μ F X5R or X7R dielectric ceramic capacitors with 10m Ω to 30m Ω ESR range between device outputs to ground for transient stability. The FP6142 is designed to be stable with low ESR ceramic capacitors and higher values of capacitors, and ESR could improve output stability. The ESR of output capacitor is very important because it generates a zero to provide phase lead for loop stability.

There is no requirement for the ESR on the input capacitor, but its voltage and temperature coefficient have to be considered for device application environment.

Current Limit

The FP6142 includes a current limit. It monitors the output current and controls the pass transistor's gate voltage to limit the output current under 800mA (typ). The output can be shorted to ground for an indefinite amount of time without damaging the part.

Quick Discharge

The FP6142 has built-in a quick discharge circuitry to protect system function correct operation. This discharge block discharges output capacitor quickly to avoid low output voltage level to affect system's MCU abnormal work when IC is power off or enable pin pulls down.

Dropout Voltage

The minimum dropout voltage of LDO determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the FP6142 uses a P-channel MOSFET pass transistor, its dropout voltage is a function of drain-to-source on resistance (R_{DS-ON}) multiplied by the load current

Over Temperature Protection

Over temperature protection limits total power dissipation in the FP6142. When the junction temperature exceeds $T_J=+170^{\circ}\text{C}$, the thermal sensor will signal the shutdown logic and turn off the pass transistor. The thermal sensor will turn the pass transistor on again after the IC's junction temperature drops 30°C , resulting in a pulsed output during continuous thermal-overload conditions.

Thermal-Overload protection is design to protect the FP6142 in the event of fault condition. For continual operation, do not exceed the absolute maximum junction temperature rating of $T_J=+150^{\circ}\text{C}$.

Thermal Consideration

The power handling capability of the device will be limited by maximum 125°C operation junction temperature. The power dissipated by the device will be estimated by $P_D = I_{OUT} \times (V_{IN}-V_{OUT})$. The power dissipation should be lower than the maximum power dissipation listed in "Absolute Maximum Ratings" section.

Applications Information (Continued)

Soft Start Capacitor

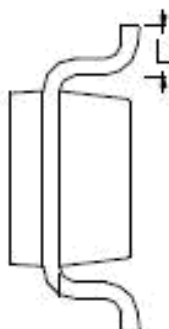
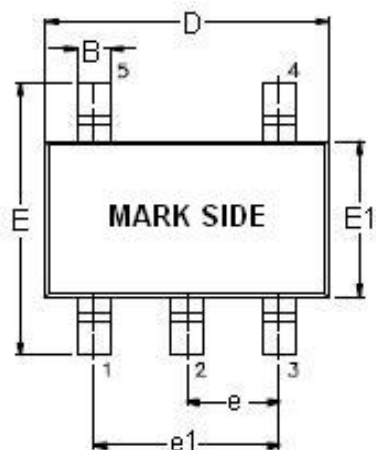
The SS pin connecting a 0.5nF capacitor could suppress inrush current and get a gradual increase of output voltage during power up. As the internal constant current source charges the external soft-start capacitor to compare with feedback voltage to control gate voltage of pass transistor. Therefore, output current increases from zero to the value required for regulation. The maximum load current will be available after the soft-start time is completed.

Active/Shutdown Input Operation

The FP6142 is turned off by pulling the EN pin low and turned on by pulling it high. The enable input is TTL/CMOS compatible threshold for simple logic interfacing. If this feature is not used, the EN pin should be connected to VIN to keep the regulator output operating normally. It will become shutdown with this pin floating because EN pin has built-in a pull down resistor (refer to Block Diagram).

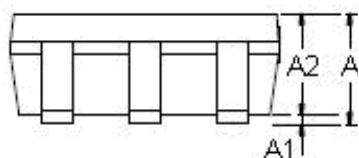
Outline Information

SOT-23-5 Package (Unit: mm)

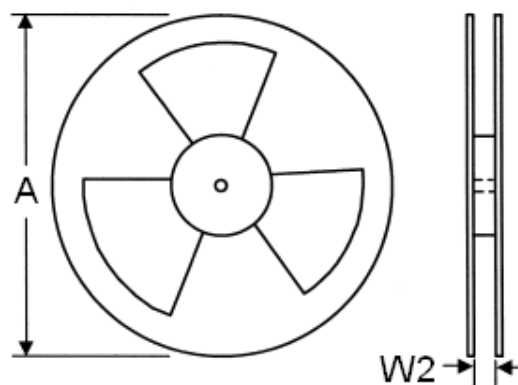
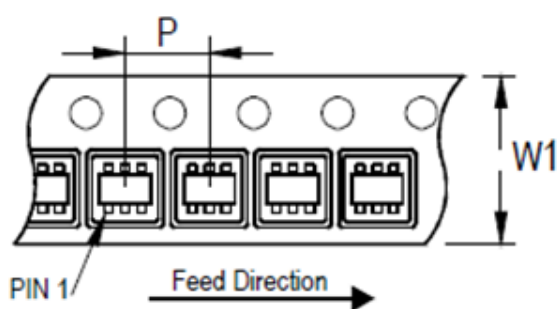


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note : Followed From JEDEC MO-178-C.



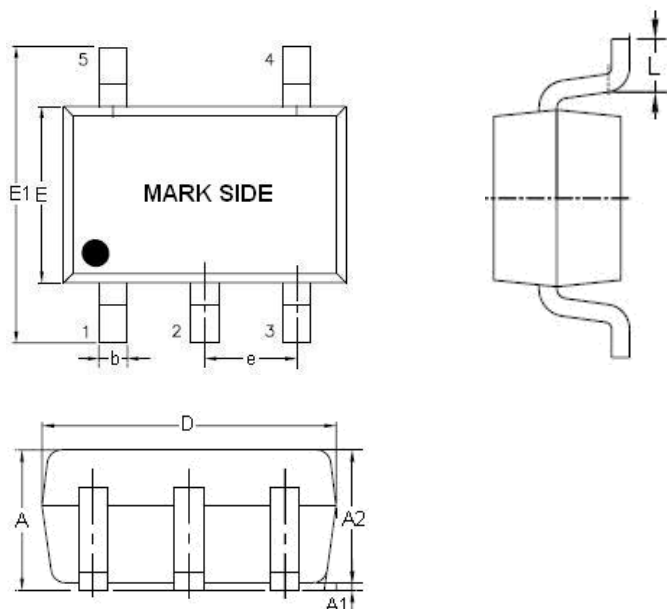
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

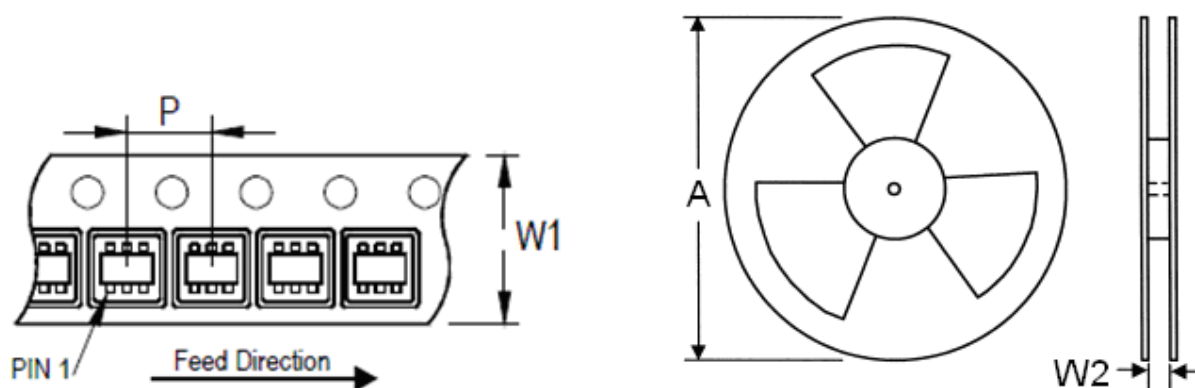
Outline Information (Continued)

SC-70-5 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.15	0.35
D	1.80	2.20
E1	1.80	2.40
E	1.15	1.35
e	0.55	0.75
L	0.26	0.46

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.