Dual High Efficiency 1MHz/1.5MHz 1A Synchronous Step Down Regulator

Description

The FP6382 is a dual channel, high efficiency, high frequency synchronous DC-DC step-down regulator. The 100% duty cycle feature provides low dropout operation, extending battery life in portable systems.

The internal synchronous switch increases efficiency and eliminates the need for external Schottky diode. At shutdown mode, the input supply current is less than 1μA.

The current limit protection and on-chip thermal shutdown features provide protection against any combination of overload or ambient temperature.

Features

- Low $R_{DS(ON)}$ for Internal Switch (Top/Bottom): 200/150mΩ
- 2.5V~5.5V Input Voltage Range
- 1A Output Current
- 1MHz/1.5MHz Switching Frequency Minimizes the External Components
- Internal Soft-Start Limits the Inrush Current
- Internal Compensation Function
- 100% Dropout Operation
- Short Circuit Protection with Auto Recovery
- RoHS Compliant and Halogen Free
- TDFN-12 (3mm×3mm) Package

Applications

- Set Top Box
- LCD TV
- Notebook
- Wireless LAN
- Handheld Instrument
- MP3 Portable Audio Player
- Battery Operated Device

Pin Assignments

WD Package (TDFN-12)(3mmx3mm)

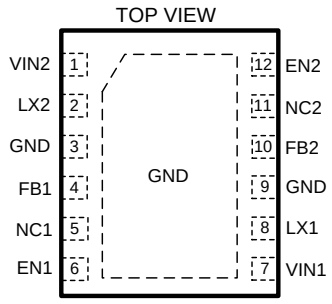
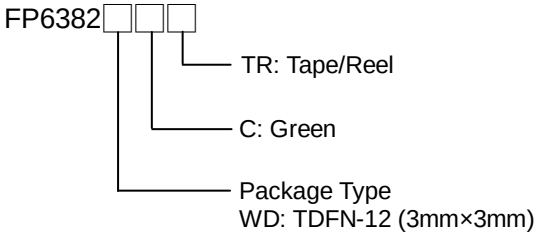


Figure 1. Pin Assignment of FP6382

Ordering Information



Typical Application Circuit

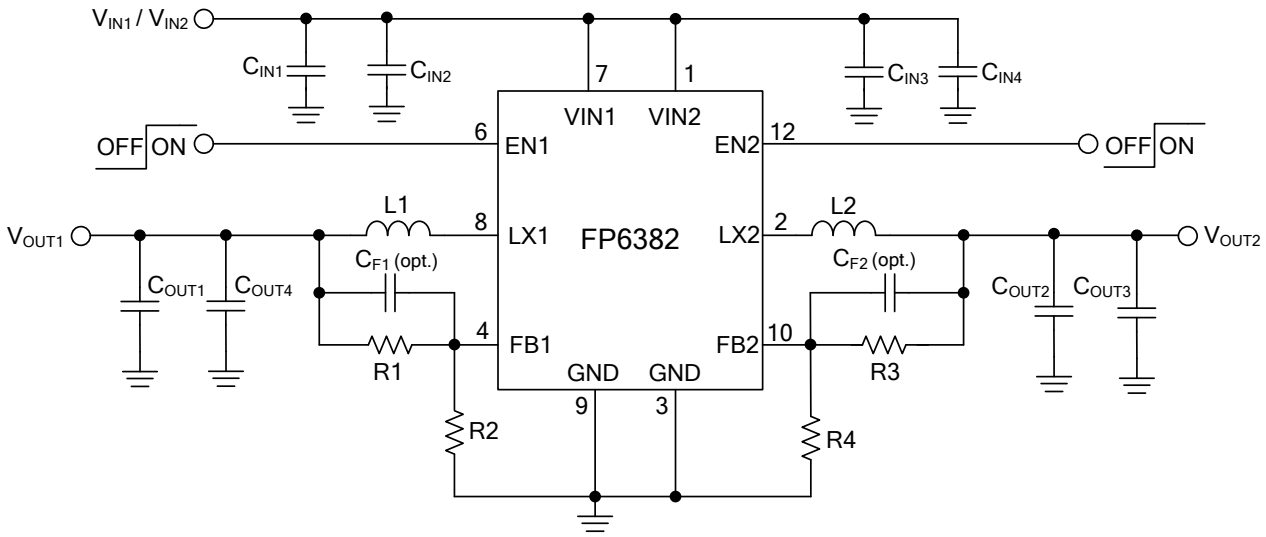


Figure 2. Schematic Diagram

VIN=5V, the recommended BOM list is as below.

V_{OUT}	C_{IN1}, C_{IN3}	C_{IN2}, C_{IN4}	R1, R3	R2, R4	L1, L2	C_{OUT1}, C_{OUT2}	C_{OUT3}, C_{OUT4}
3.3V	4.7μF MLCC	0.1μF	453kΩ	100kΩ	2.2μH	10μF MLCC	0.1μF
2.5V	4.7μF MLCC	0.1μF	316kΩ	100kΩ	2.2μH	10μF MLCC	0.1μF
1.8V	4.7μF MLCC	0.1μF	200kΩ	100kΩ	2.2μH	10μF MLCC	0.1μF
1.5V	4.7μF MLCC	0.1μF	150kΩ	100kΩ	1.8μH	10μF MLCC	0.1μF
1.2V	4.7μF MLCC	0.1μF	100kΩ	100kΩ	1.8μH	10μF MLCC	0.1μF
1.05V	4.7μF MLCC	0.1μF	75kΩ	100kΩ	1.5μH	10μF MLCC	0.1μF

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No.	Pin Function
EN1	6	Enable control. Pull high to turn the IC on, and pull low to turn off the IC. Don't leave this pin floating.
EN2	12	Enable control. Pull high to turn the IC on, and pull low to turn off the IC. Don't leave this pin floating.
GND	3, 9	Ground pin. This pin is connected to the exposed pad with copper.
LX1	8	Power switching output. Connect an external inductor to this switching node.
LX2	2	Power switching output. Connect an external inductor to this switching node.
VIN1	7	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
VIN2	1	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
FB1	4	Feedback input pin. Connect FB1 and VOUT1 with a resistive voltage divider. This IC senses feedback voltage via FB1 and regulates it at 0.6V.
FB2	10	Feedback input pin. Connect FB2 and VOUT2 with a resistive voltage divider. This IC senses feedback voltage via FB2 and regulates it at 0.6V.
NC1	5	No connection.
NC2	11	No connection.

Block Diagram

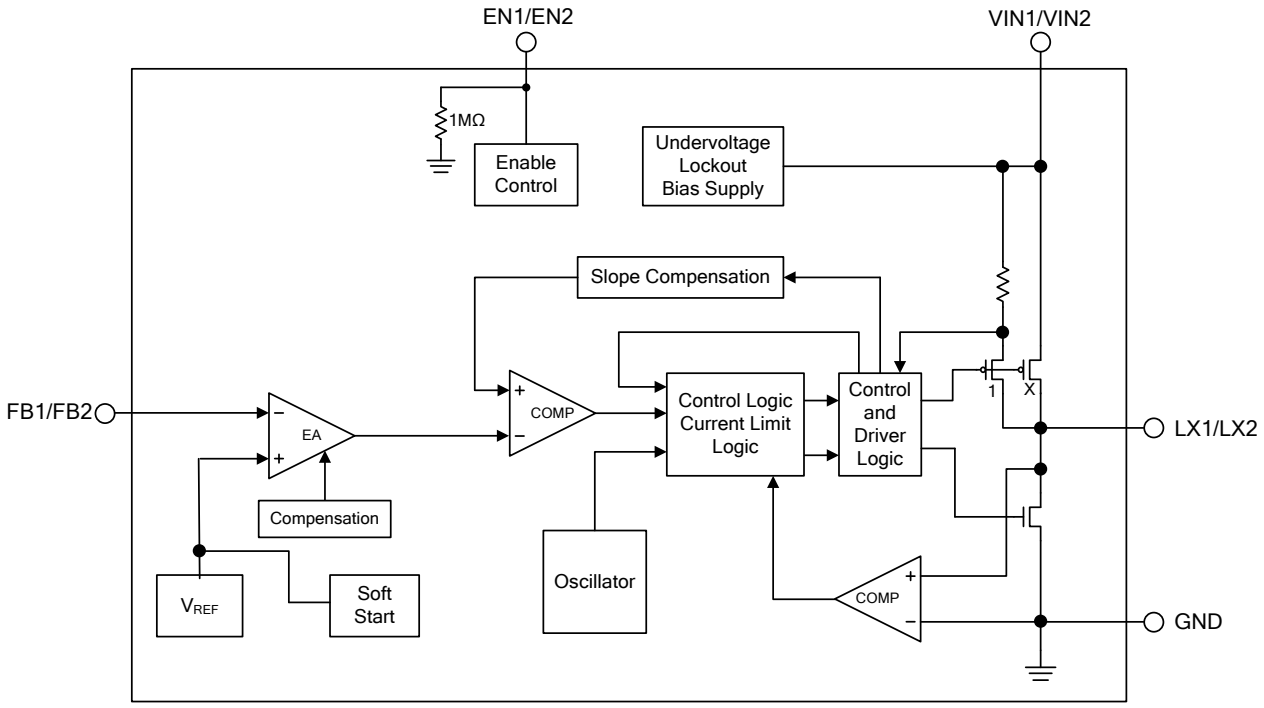


Figure 3. Block Diagram of FP6382

Absolute Maximum Ratings (Note 1)

- VIN to GND ---------- -0.3V to +6.5V
- LX to GND ---------- -0.3V to V_{IN}+0.3V
- EN, FB to GND ---------- -0.3V to V_{IN}
- Package Thermal Resistance, (θ_{JA})

  TDFN-12 (3mm×3mm) ---------- +65°C/W
- Package Thermal Resistance, (θ_{JC})

  TDFN-12 (3mm×3mm) ---------- +29°C/W
- Maximum Junction Temperature (T_J) ---------- +150°C
- Lead Temperature (Soldering, 10 sec.) ---------- +260°C
- Storage Temperature (T_{STG}) ---------- -65°C to +150°C

Note 1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (Note 2)

- Supply Voltage (V_{IN}) ---------- +2.5V to +5.5V
- Operation Temperature Range (T_{OPR}) ---------- -40°C to +85°C

Note 2：The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{IN}=5V, V_{OUT} =2.5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shutdown Current	I_{SHDN}	EN=0V		0.1	1	μA
Quiescent Current	I_q	V_{FB}=0.65V, I_{OUT}=0A		80		μA
Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Leakage Current	I_{FB}	V_{FB}=V_{IN}		0.01	1	μA
P-Channel MOSFET On-Resistance (Note 3)	$R_{DS(ON)}$			200		mΩ
N-Channel MOSFET On-Resistance (Note 3)	$R_{DS(ON)}$			150		mΩ
P-Channel Current Limit (Note 3)	I_{LIM}		1.5			A
EN High-Level Input Voltage	V_{IH}		1.5			V
EN Low-Level Input Voltage	V_{IL}				0.4	V
Under Voltage Lockout Voltage	UVLO			2.4		V
UVLO Hysteresis	V_{HYS}			0.2		V
Oscillation Frequency	F_{OSC}	I_{OUT1}=200mA (LX1)	1.2	1.5	1.8	MHz
		I_{OUT2}=200mA (LX2)	0.8	1	1.2	
Minimum On Time				50		ns
Maximum Duty Cycle			100			%
VOUT Discharge Resistance				100		Ω
Thermal Shutdown Temperature (Note 3)	T_{SD}			150		°C
Internal Soft Start Time	T_{SS}			1		ms

Note 3：Guarantee by design.

Typical Performance Curves

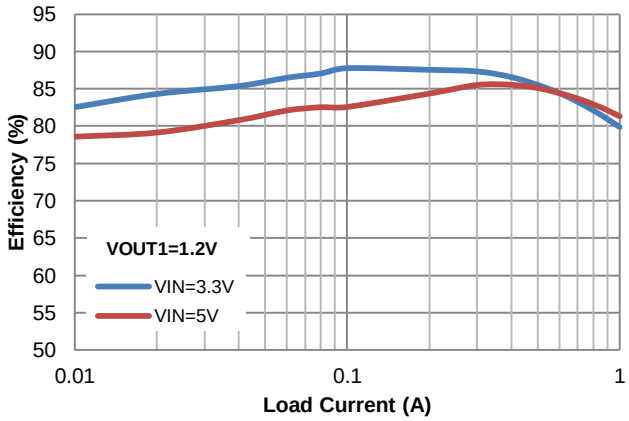


Figure 4. Efficiency vs. Load Current

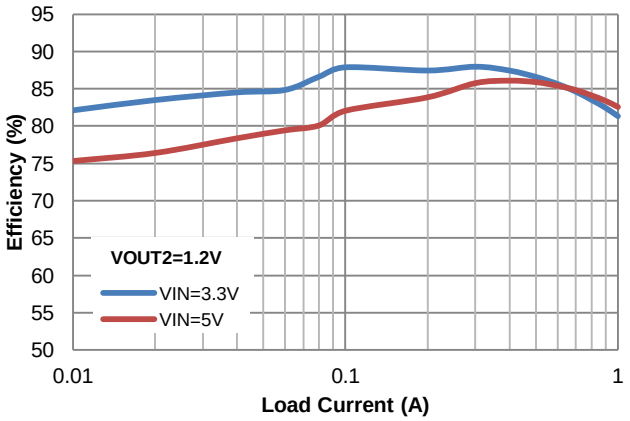


Figure 5. Efficiency vs. Load Current

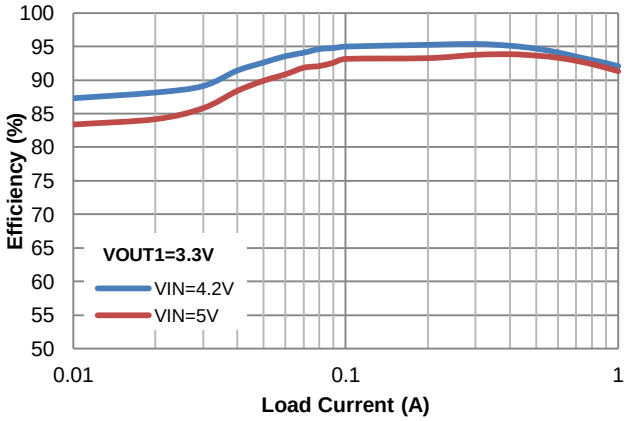


Figure 6. Efficiency vs. Load Current

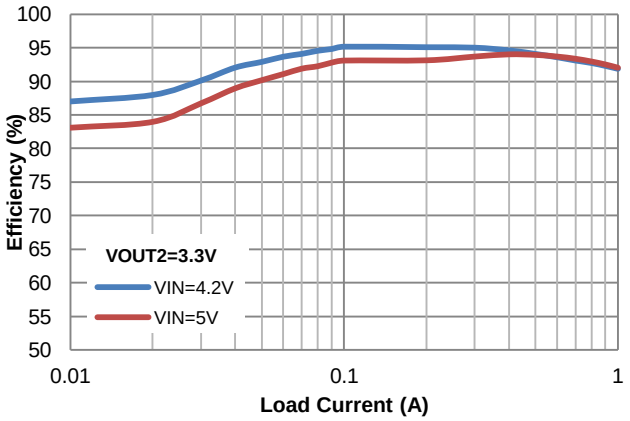


Figure 7. Efficiency vs. Load Current

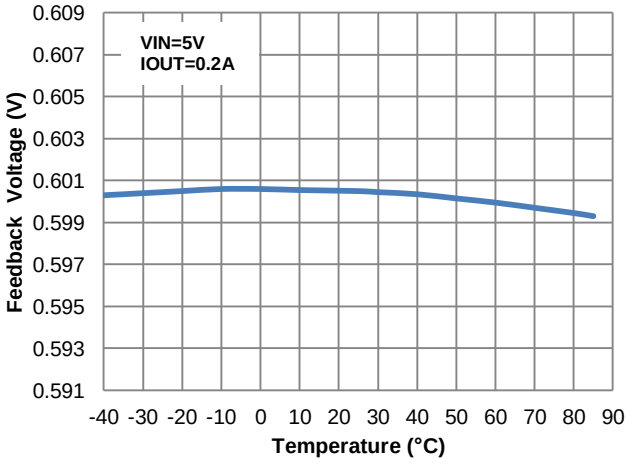


Figure 8. Feedback Voltage vs. Temperature

Typical Performance Curves (Continued)

V_{IN1}, V_{IN2}=5V, V_{OUT1}, V_{OUT2}=1.2V, C_{IN1}, C_{IN2}=4.7μF, C_{OUT1}, C_{OUT2}=10μF, $L_{1,2}$=1.8μH, TA=+25°C, unless otherwise noted.

I_{OUT1}, I_{OUT2}=0A

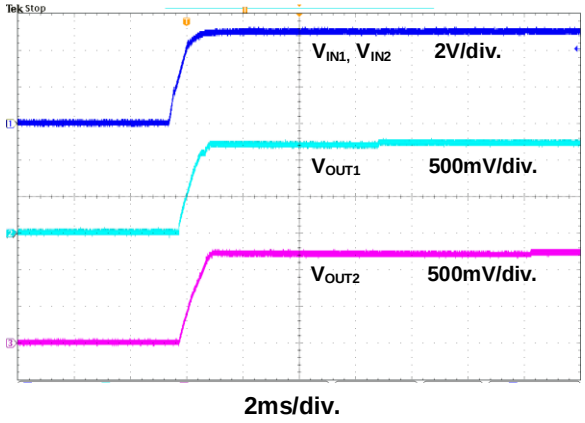


Figure 9. Power On through VIN Waveform

I_{OUT1}, I_{OUT2}=1A

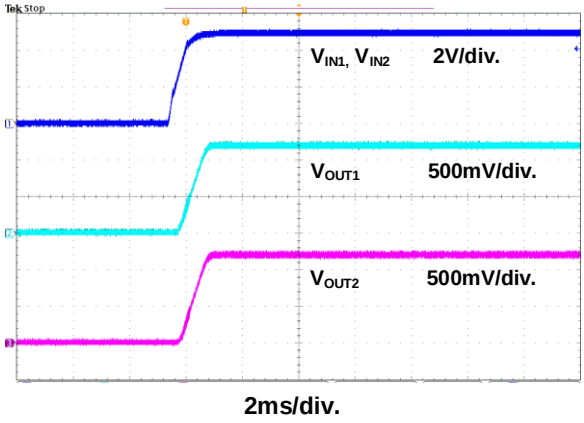


Figure 10. Power On through VIN Waveform

I_{OUT1}, I_{OUT2}=0A

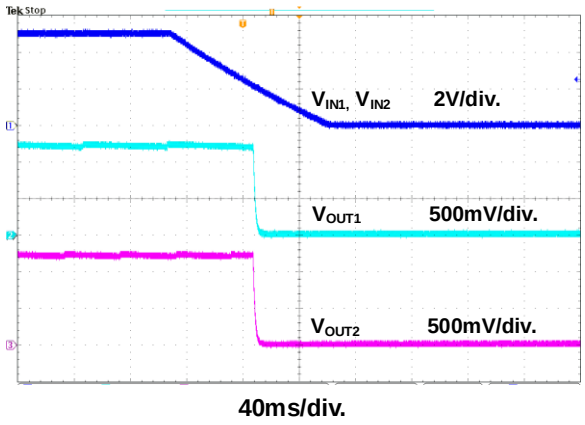


Figure 11. Power Off through VIN Waveform

I_{OUT1}, I_{OUT2}=1A

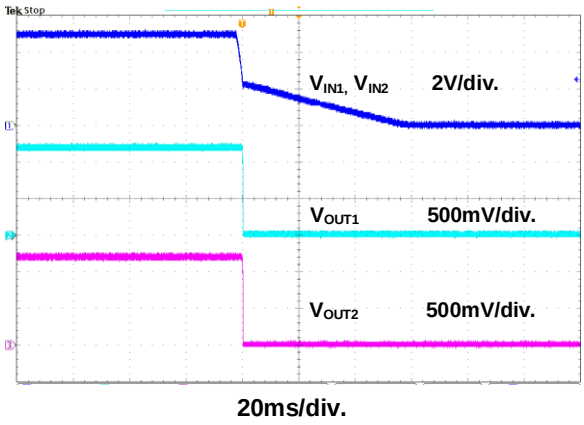


Figure 12. Power Off through VIN Waveform

I_{OUT1}, I_{OUT2}=0A

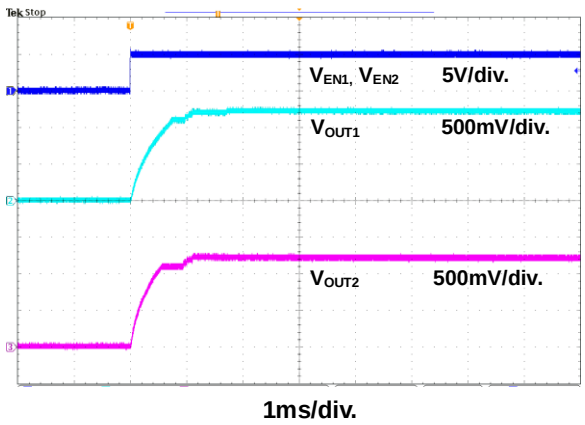


Figure 13. Power On through EN Waveform

I_{OUT1}, I_{OUT2}=1A

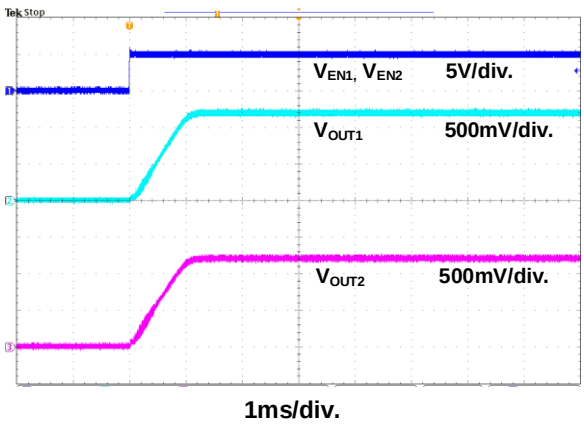


Figure 14. Power On through EN Waveform

Typical Performance Curves (Continued)

V_{IN1}, V_{IN2}=5V, V_{OUT1}, V_{OUT2}=1.2V, C_{IN1}, C_{IN2}=4.7μF, C_{OUT1}, C_{OUT2}=10μF, $L_{1,2}$=1.8μH, TA=+25°C, unless otherwise noted.

I_{OUT1}, I_{OUT2}=0A

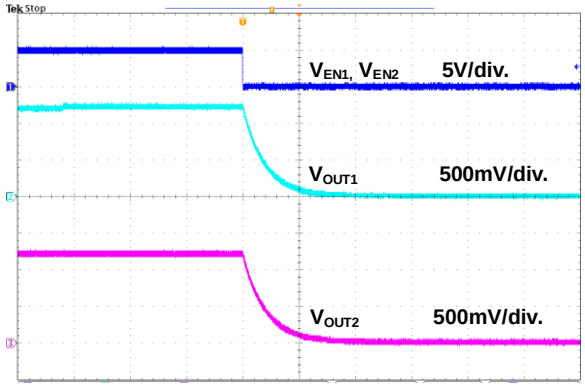


Figure 15. Power Off through EN Waveform

I_{OUT1}, I_{OUT2}=1A

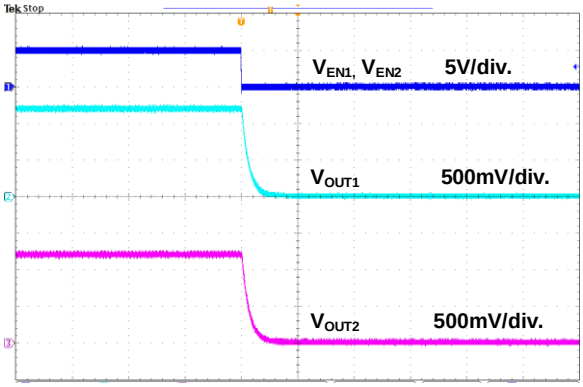


Figure 16. Power Off through EN Waveform

I_{OUT1}=0A

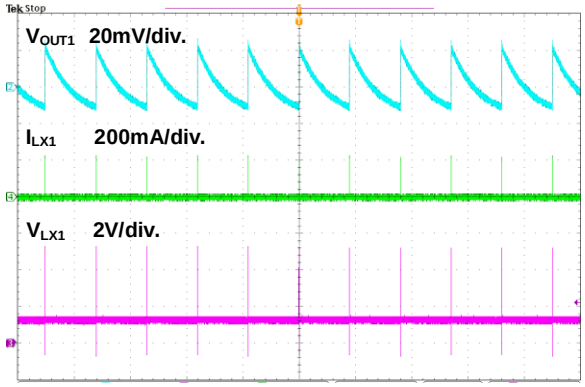


Figure 17. Steady State Waveform

I_{OUT1}=1A

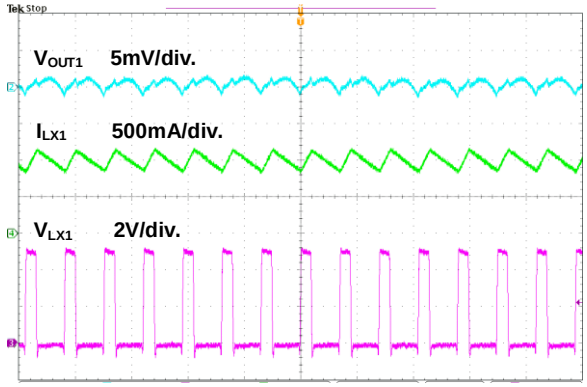


Figure 18. Steady State Waveform

I_{OUT1}=0.1A to 1A

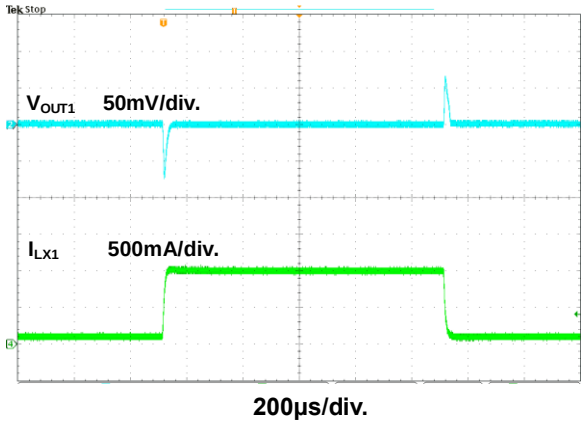


Figure 19. Load Transient Waveform

I_{OUT2}=0.1A to 1A

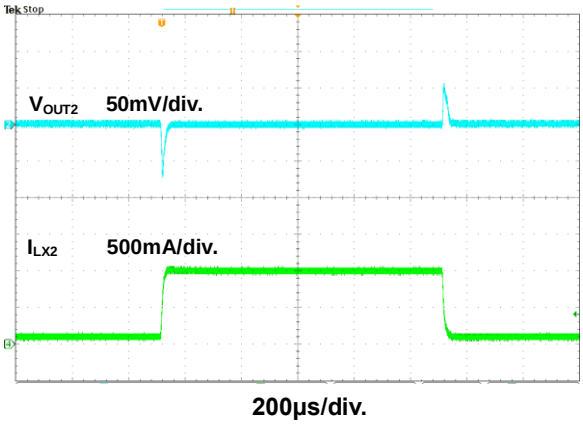


Figure 20. Load Transient Waveform

Function Description

The FP6382 is a dual channel, high efficiency, high frequency synchronous DC-DC step-down regulator. The 100% duty cycle feature provides low dropout operation, extending battery life in portable systems. At light load condition, the FP6382 can operate at PSM mode to support high efficiency and reduce power lose. It has integrated high-side (200mΩ, typ.) and low-side (150mΩ, typ.) power switches, and provides 1A continuous load current. It regulates input voltage from 2.5V to 5.5V, and down to an output voltage as low as 0.6V.

Control Loop

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load, line response, protection of the internal main switch and synchronous rectifier. The FP6382 switches at a constant frequency (1MHz & 1.5MHz) and regulates the output voltage. During each cycle, the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until next cycle starts.

Enable

The FP6382 EN pin provides digital control to turn on/off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator will start the soft start function. If the EN pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect EN to VIN.

Soft Start

The FP6382 employs internal soft start function to reduce input inrush current during start up. The internal soft start time will be 1ms.

Under Voltage Lockout

When the FP6382 is power on, the internal circuits will be held inactive until V_{IN} voltage exceeds the UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the UVLO threshold voltage. The hysteretic of the UVLO comparator is 200mV (typ).

Short Circuit Protection

The FP6382 provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 40% of the regulation level, this will activate the latch protection circuit. Then output will be forced shutdown to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions. Once the short condition is removed, reset EN or VIN to restart IC.

Over Current Protection

The FP6382 over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Over Temperature Protection

The FP6382 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 30°C (typ).

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.6V. Thus the output voltage is:

$$V_{OUT}=0.6V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
3.3V	453kΩ	100kΩ
2.5V	316kΩ	100kΩ
1.8V	200kΩ	100kΩ
1.5V	150kΩ	100kΩ
1.2V	100kΩ	100kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

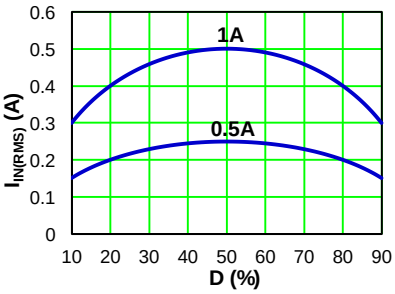
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice.

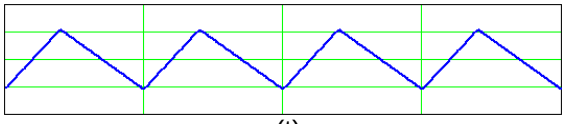
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

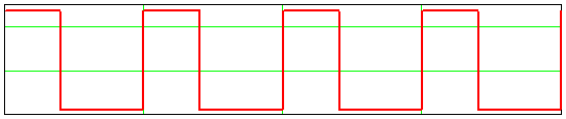
$V_{RIPPLE(ESR)}(t)$



(t)

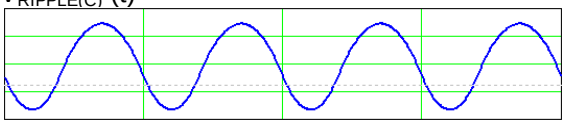
+

$V_{RIPPLE(ESL)}$ (t)



+ (t)

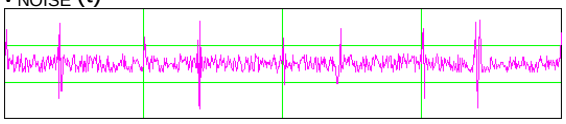
$V_{RIPPLE(C)}$ (t)



(t)

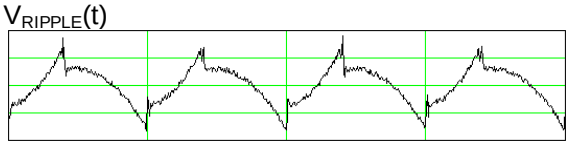
+

V_{NOISE} (t)



=

$V_{RIPPLE}(t)$



(t)

Application Information (Continued)

$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

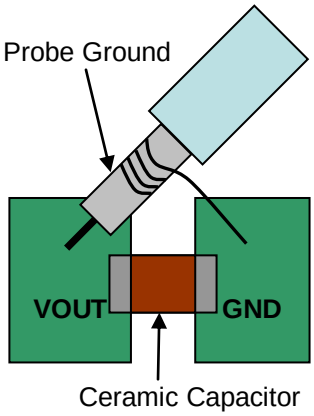
$$V_{RIPPLE(ESL)}=\frac{ESL}{L+ESL}\times V_{IN}$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC^2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



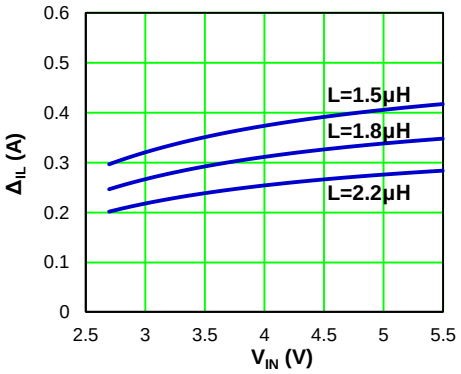
Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphically represent ΔI_L equation.



V_{OUT1}=1.2V, F_{OSC1}=1.5MHz

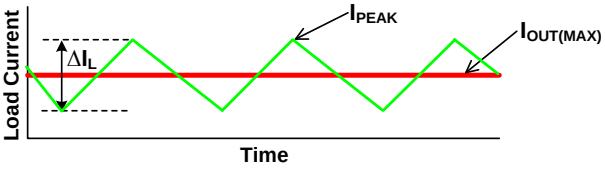
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FP6382 current limit. The peak inductor current is shown as below:

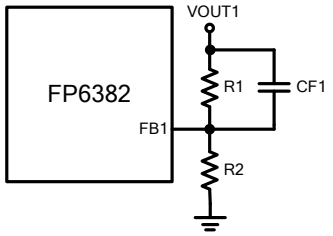
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor CF1 and CF2 in the feedback network is recommended to improve transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor CF1 and CF2 can be calculated with the following equation:

$$CF1=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 330pF.

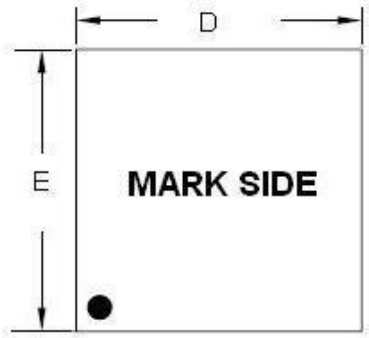
PCB Layout Recommendation

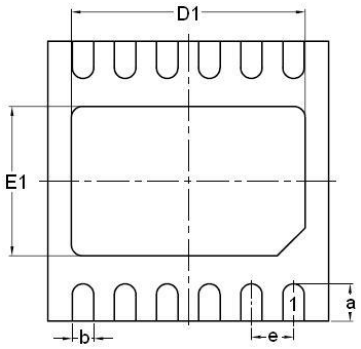
The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. Multi-layer PCB design is recommended.

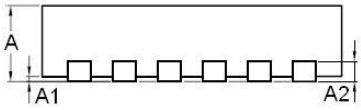
Outline Information

TDFN-12 3mm x 3mm (pitch 0.45mm) Package (Unit: mm)

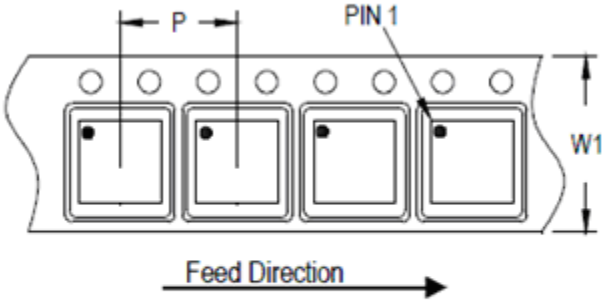


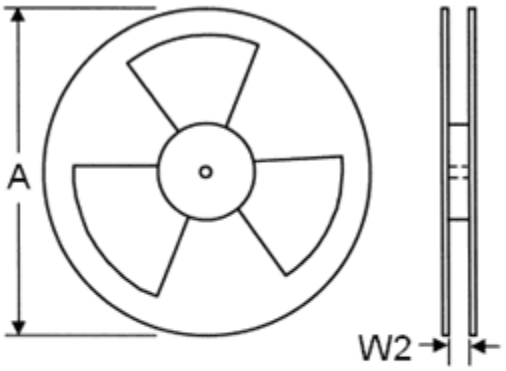


SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	2.90	3.10
E	2.90	3.10
a	0.35	0.48
b	0.18	0.30
e	0.40	0.50
D1	2.30	2.55
E1	1.55	1.80



Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.