PWM Controlled, Step-up DC/DC Converter in Tiny Package

Description

The FP6733 is a high efficiency PWM DC/DC step-up converter with internal compensated current mode controller. The output voltage is set by using two external resistors. The 550kHz switching frequency minimizes the size of external components. Both internal 1A switch and driver for driving external power device (NMOS or NPN) are provided.

The FP6733 starts up below 1V input voltage with 1mA load. Due to built-in automatic PWM/PFM switch-over function, the FP6733 is able to get high efficiency during both light and heavy load. External transistor pin is available to accommodate high output current applications.

The FP6733 is available in SOT-23-6 and TSOT-23-6 packages.

Features

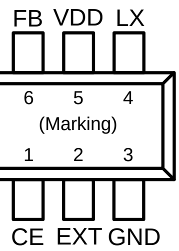
- 0.9V (Typ.) Low Start-up Input Voltage at 1mA Load
- High Switching Frequency at 550kHz
- Provide Flexibility for Using Internal and External Power Switches
- Automatic PFM Mode at Light Load
- Low Ripple and High Efficiency
- Excellent Line/Load Regulation
- Chip Enable Control Function
- Current Limit Protection
- Thermal Overload Protection
- Space Saving Packages: SOT-23-6 and TSOT-23-6

Applications

- PDA
- MP3
- DSC
- RF Tag
- Wireless Equipment
- Portable Equipment

Pin Assignments

S6 Package (SOT-23-6)



S9 Package (TSOT-23-6)

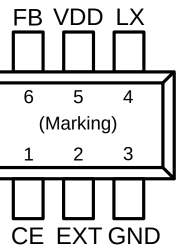
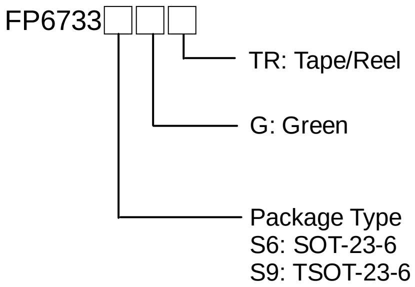


Figure1. Pin Assignment of FP6733

Ordering Information



SOT-23-6 Marking

Part Number	Product Code
FP6733S6G	AA=

TSOT-23-6 Marking

Part Number	Product Code
FP6733S9G	aa=

Typical Application Circuit

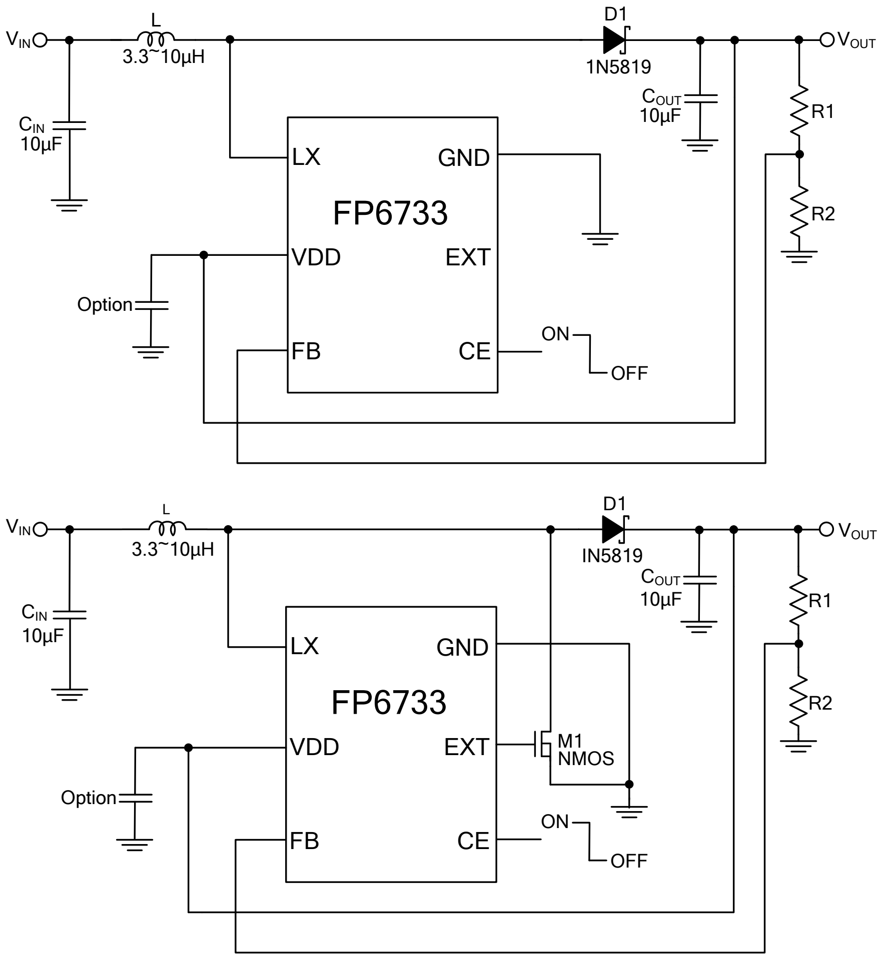


Figure 2. Typical Application Circuit of FP6733

Functional Pin Description

Pin Name	Pin Function
CE	IC chip enable.
EXT	External switch transistor driver output.
GND	Ground.
LX	Internal switch MOS output.
VDD	IC internal power supply.
FB	Feedback input pin. Internal reference voltage for error amplifier is 1.25V.

Block Diagram

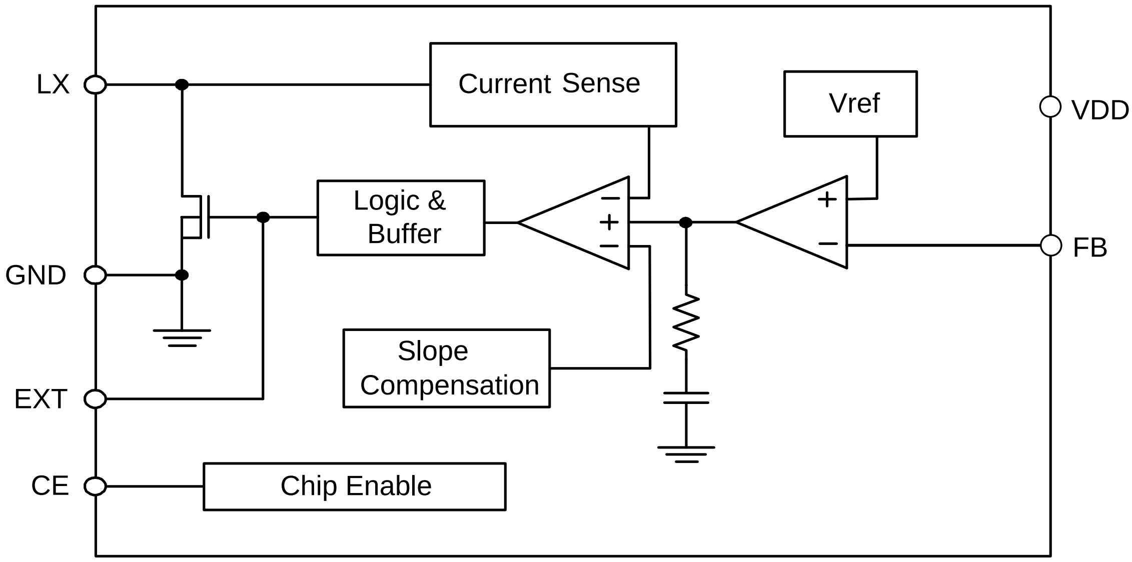


Figure 3. Block Diagram of FP6733

Absolute Maximum Ratings

- LX to GND -- +6V
- All Other Pins to GND --- +6V
- Maximum Junction Temperature -- +150°C
- Power Dissipation @T_A=25°C, SOT-23-6, TSOT-23-6 (P_D) -- +0.40W
- Package Thermal Resistance, SOT-23-6, TSOT-23-6 (θ_{JA}) -- +250°C/W
- Storage Temperature Range (T_{STG}) -- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) (T_{LEAD}) -- +260°C

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Operating Voltage (V_{DD}) --- +2.9V to +5.5V
- Operating Temperature Range (T_{OPR}) --- -40°C to +85°C

Electrical Characteristics

(T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operation Voltage	V_{DD}	Normal Operation	2.9		5.5	V
Start-Up Voltage	V_{START}	V_{IN} : 0→1V, I_{OUT}=1mA		0.9	1.05	V
No-Load Input Current	I_{NO_LOAD}	V_{IN}=1.5V, V_{OUT}=3.3V		75		μA
Continuous Switching Current	I_{SWITCH}	V_{DD}=3.3V, V_{FB}=0V	0.2	0.3	0.4	mA
No Switch Current	I_Q	V_{IN}=6V		17	25	μA
Shutdown Current	I_{SD}	VDD=4.5V, CE pin=0V		0.1	1.0	μA
Feedback Reference Voltage	V_{FB}	Close loop, V_{DD}=3.3V	1.225	1.25	1.275	V
EXT ON Resistance to V_{DD}		V_{DD}=3.3V		5	8.5	Ω
EXT ON Resistance to GND		V_{DD}=3.3V		5	8.5	Ω
LX ON Resistance (Note 2)	R_{DS-ON}	V_{DD}=3.3V		0.3		Ω
Max. Duty Ratio	DUTY	V_{DD}=3.3V	85	95		%
Oscillator Frequency	f_{OSC}	V_{DD}=3.3V	450	550	650	kHz
LX Leakage Current	I_{LXL}	V_{LX}=6V		0.1	1.0	μA
Line Regulation	ΔV_{LINE}	V_{IN}=1.5 ~2.5V, I_L=50mA		3	10	mV/V
Load Regulation	ΔV_{LOAD}	V_{IN}=2.5V, I_L=1~100mA		0.15	0.3	mV/mA
Switch Current Limit (Note 2)	I_{LIMIT}	V_{DD}=3.3V	0.75	1		A
CE "High" Voltage	V_{CEH}	V_{DD}=3.3V, switch ON	1.2			V
CE "Low" Voltage	V_{CEL}	V_{DD}=3.3V, switch OFF			0.4	V
CE "High" Current	I_{CEH}	V_{DD} =3.3V, V_{CE}=V_{DD}			0.1	μA
CE "Low" Current	I_{CEL}	V_{DD} =3.3V, V_{CE}=0V			-0.1	μA
Efficiency (Note 2)	η			85		%
Thermal Shutdown Threshold (Note 2)	T_{SD}			145		ºC
	ΔT_{SD}	Hysteresis		30		ºC

Note 2：Guarantee by design.

Typical Performance Curves

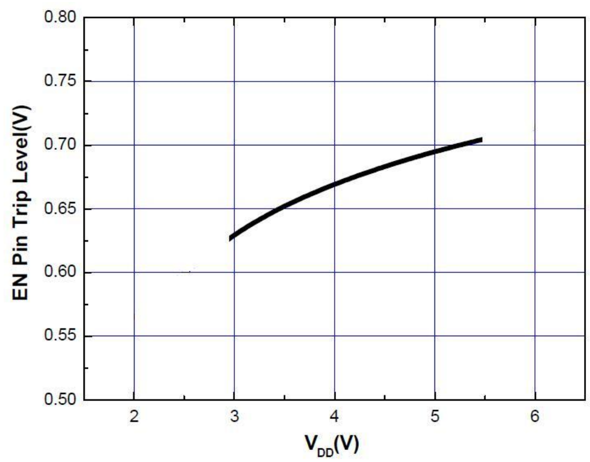


Figure 4. Operation Voltage vs. En Pin Trip Level

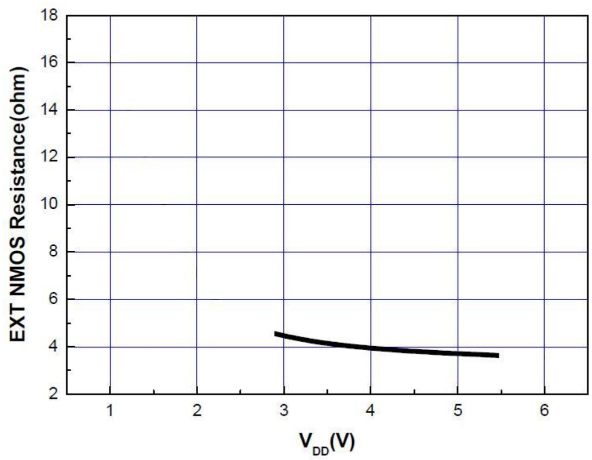


Figure 5. Operation Voltage vs. EXT NMOS Resistance

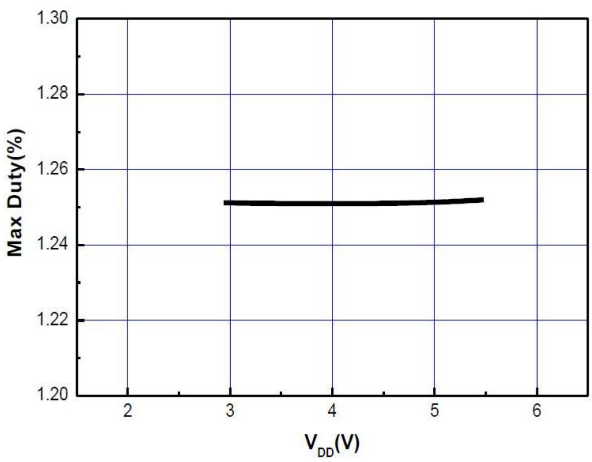


Figure 6. Operation Voltage vs. Max Duty

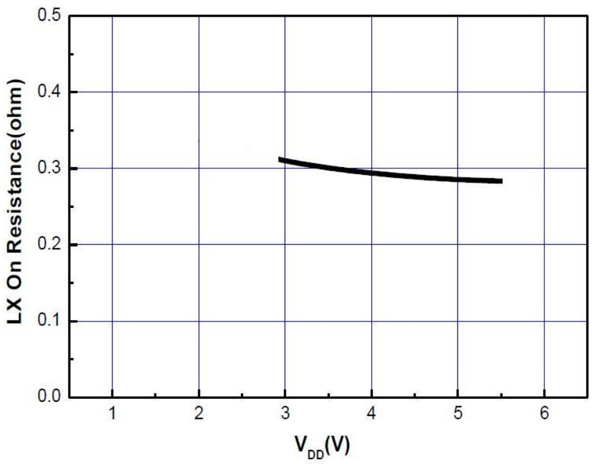


Figure 7. Operation Voltage vs. LX On Resistance

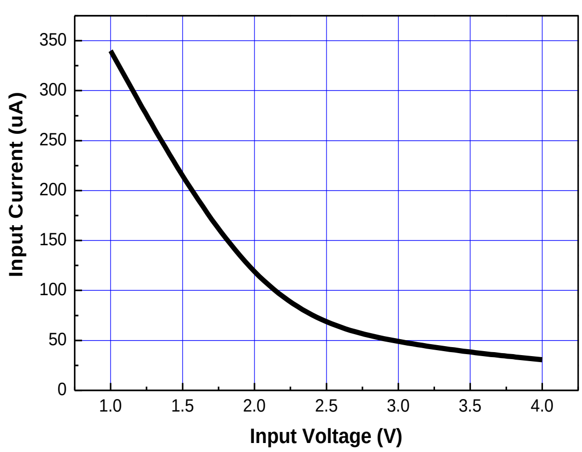


Figure 8. Input Voltage vs. Input Current

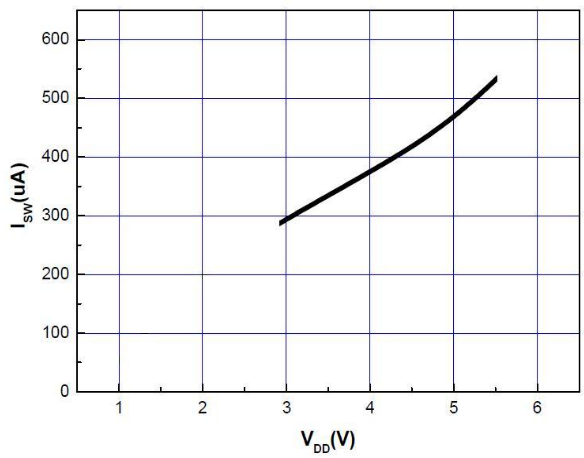


Figure 9. Operation Voltage vs. Switch Current

Typical Performance Curves (Continued)

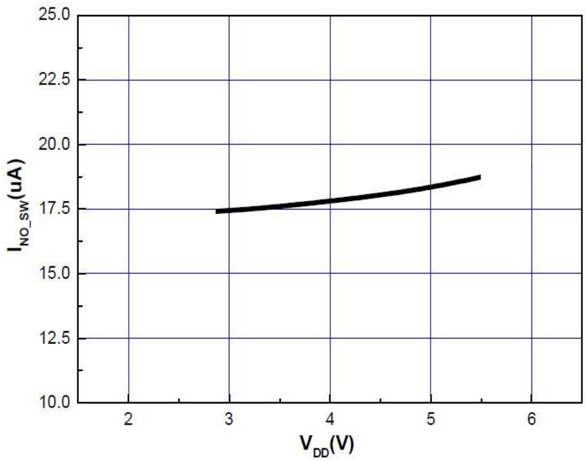


Figure 10. Operation Voltage vs. Quiescent Current

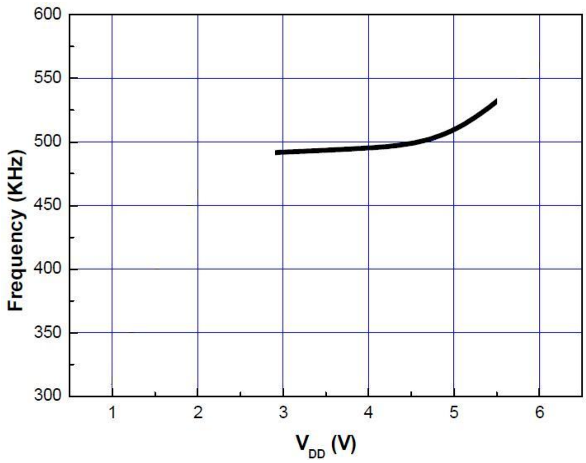


Figure 11. Operation Voltage vs. Frequency (analog control)

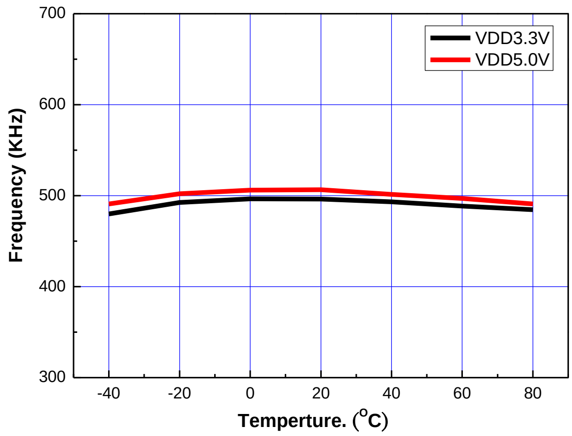


Figure 12. Temperature vs. Frequency

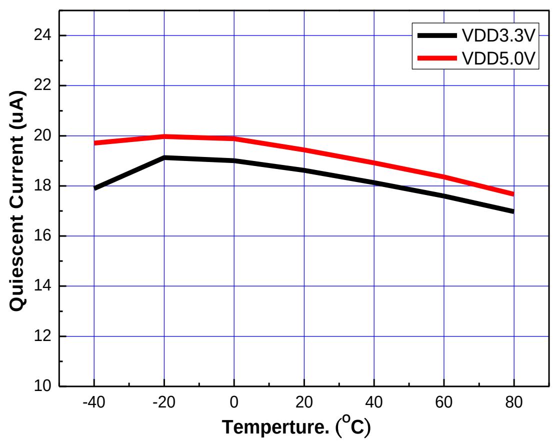


Figure 13. Temperature vs. Quiescent Current
Vin=5V, 3LEDs, ILED=100mA, Cout=1μF

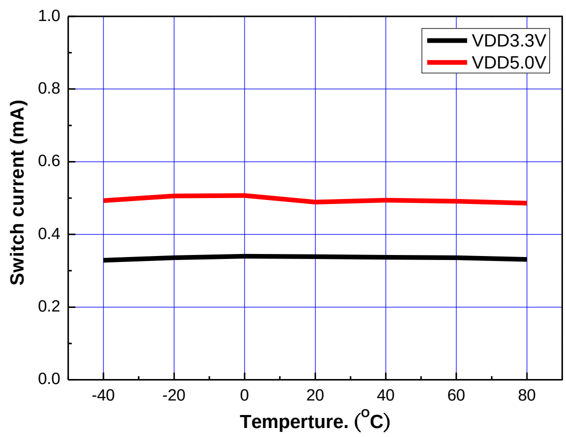


Figure 14. Temperature vs. Switch current
3.3Vi to 3LEDs (PWM control)

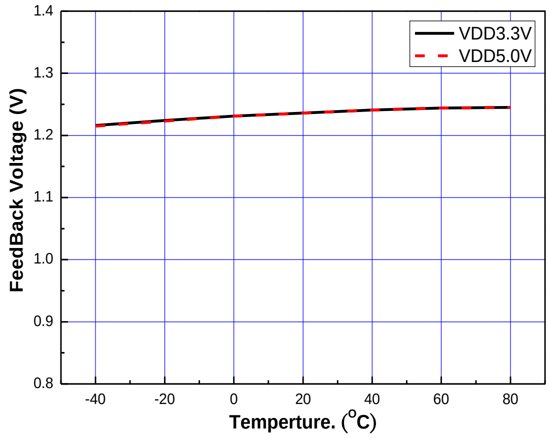


Figure 15. Temperature vs. Feedback Voltage
3.3Vi to 4LEDs (PWM control)

Typical Performance Curves (Continued)

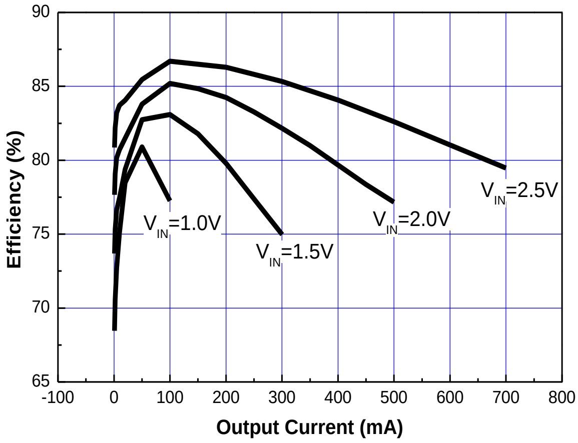


Figure 16. Efficiency (V_{OUT}=3.3V)

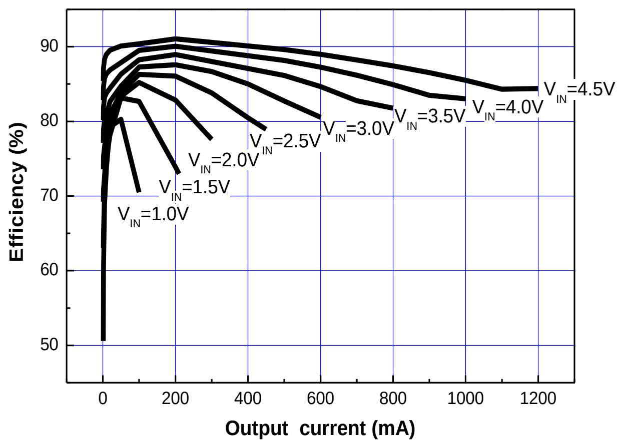


Figure 17. Efficiency (V_{OUT}=5.0V)
(analog control)

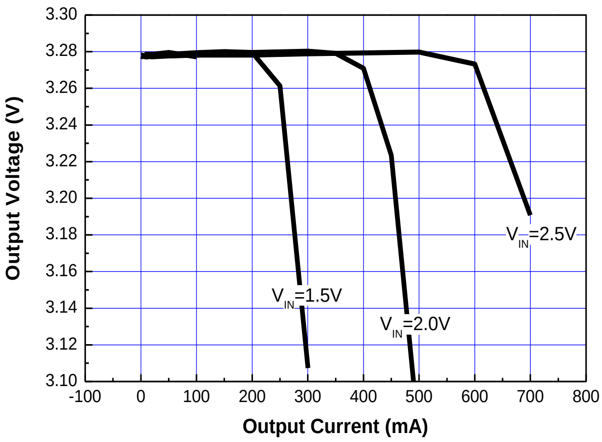


Figure 18. Load Regulation (V_{OUT}=3.3V)

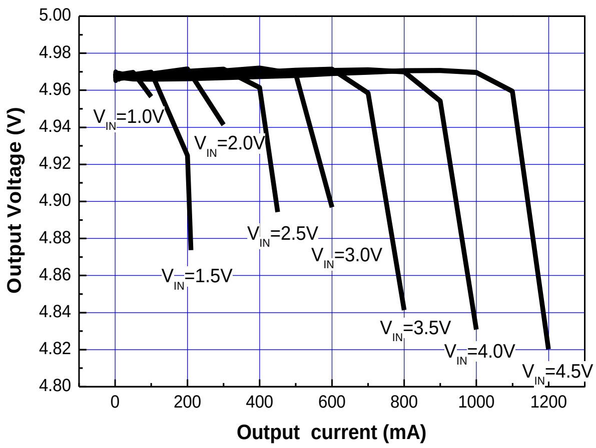


Figure 19. Load Regulation (V_{OUT}=5.0V)
VIN=5V, 3LEDs, ILED=100mA, COUT=1μF

Application Information

Operation

The FP6733 is designed in a current mode PFM/PWM scheme which features an automatic switch PFM/PWM mode to maintain the highest efficiency and extend battery life. The quiescent current is less than 25μA at no switching status.

The control loop is internally compensated reducing the amount of external components.

Chip Enable

The FP6733 features a chip enable input pin that allows on/off control of the regulator. When CE=Low, shutdown of the chip occurs and at that time almost no quiescent current (<1μA) flows. The chip enable input is TTL/CMOS compatible. Connect CE to battery for normal operation.

Current Limit Protection

The FP6733 provides cycle-by-cycle over-current protection. Current limit is accomplished by sensing voltage drop across the drain to source of power switch. If the current sense amplifier output voltage is larger than current-limited threshold level (Typ. 1.0A), it will immediately turn off power MOS.

Thermal Protection

Thermal protection limits total power dissipation in the FP6733. When the junction temperature exceeds Tj=145°C, the thermal sensor signals the shutdown logic and turns off most of the internal circuitry. The thermal sensor will turn internal circuitry on again after the IC's junction temperature drops 30°C.

Adjustable Output Voltage

The output voltage of FP6733 ranges from 1.25V to 5.0V which is set by the external feedback resistor. It can be calculated as:

$$V_{OUT}=1.25\times\left(1+\frac{R1}{R2}\right)$$

Inductor Selection

A 3.3μH to 10μH inductor is recommended for general use. The value of inductor depends on the operating frequency. Higher frequency allows smaller inductor and capacitor but increasing internal switching loss. Two inductor parameters should be considered, current rating and DCR. The DCR of inductor affects the efficiency of the converter. The inductor with lowest DCR is chosen for highest efficiency.

The inductor value can be calculated as:

$$L=\frac{V_{IN}(V_{OUT}-V_{IN})}{f\times\Delta I_L\times V_{OUT}}$$

ΔI_L: inductor ripple current, usually set 20% x I_L, which defined as:

$$\Delta I_L=\frac{(V_{OUT}-V_{IN})}{L\times f}\left(\frac{V_{IN}}{V_{OUT}}\right)$$

The inductor should be rated for the maximum output current ($I_{O(MAX)}$) plus the inductor ripple current (ΔI_L) to avoid saturation. The maximum inductor current ($I_{L(MAX)}$) is given by:

$$I_{L(MAX)}=I_{O(max)}+\frac{\Delta I_L}{2}$$

Capacitor Selection

The FP6733 is permissible to use ceramic capacitor for hand held instrument applications. The value of capacitor depends on acceptable voltage ripple.

The input capacitor can reduce peak current and noise at power source. It should be 10μF at least and be increased for better input voltage filtering. Select the input capacitor to meet the input ripple current and voltage rating.

When selecting an output capacitor, consider the output ripple voltage and the ripple current. The ESR of capacitor is a major factor to the output ripple. For best performance, a low ESR output capacitor is required. The ripple voltage is given by:

$$\Delta V_O=\Delta I_L\left(ESR+\frac{1}{8\times f\times C_O}\right)$$

The common aluminum-electrolytic capacitors have high ESR and should be avoided. Ceramic capacitors have the lowest ESR in general. It's recommended to use 10μF ceramic output capacitors for the FP6733.

Diode Selection

For diode selection, both forward voltage and diode capacitance need to be considered. The output diode should be rated to the output voltage and peak switch current. Schottky diodes, with low forward voltage drop and fast reverse recovery, are the ideal choices for FP6733 applications. Make sure the diode's peak current rating is at least IPK and its breakdown voltage exceeds V_{OUT}.

Application Information (Continued)

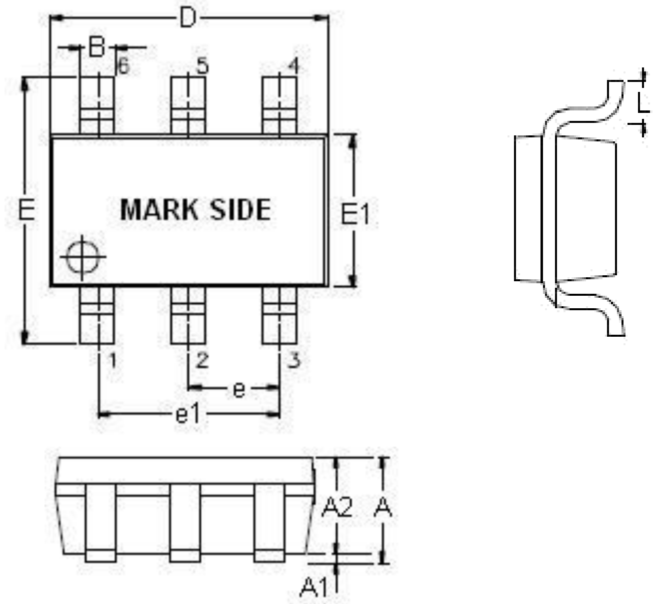
Layout Consideration

Careful PCB layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

- Place the Boost converter diode and inductor close to the LX pin and no via.
- Place the ceramic bypass capacitors near the V_{DD} and GND pin.
- Place C_{OUT} next to Schottky diode as possible.
- Use as wide and short traces as possible to the LX node.
- Keep the noise-sensitive feedback away from the switching node.

Outline Information

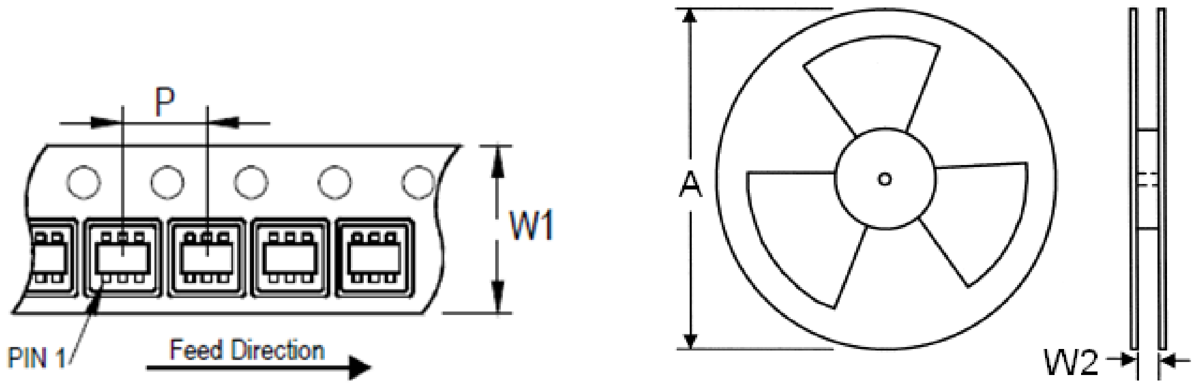
SOT-23-6 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note：Followed From JEDEC MO-178-C.

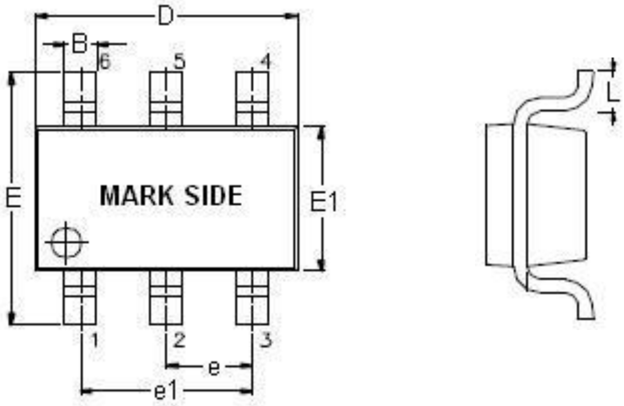
Carrier Dimensions

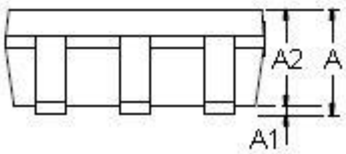


Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Outline Information (Continued)

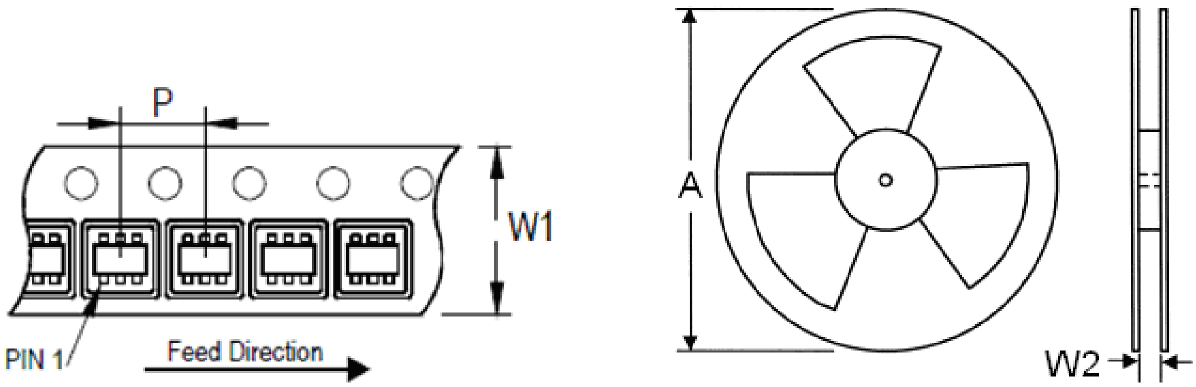
TSOT-23-6 Package (Unit: mm)





SYMBOLS UNIT	DIMENSION IN MILLIMETER MIN	MAX
A	0.70	0.90
A1	0.00	0.10
A2	0.70	1.00
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A) in	Reel Size (A) mm	Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
8	4	7	180	8.4	300~1000	3,000

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.