

Integrated Multi-Channel DC-DC Converter for TFT LCD Panel

Description

The FP6787/A offers a compact power supply solution to provide all voltages required by thin-film transistor (TFT) LCD panel. The FP6787/A includes a high performance boost regulator, a low dropout linear regulator (LDO), a voltage detector, a VCOM buffer (unity-gain OPA), a positive charge pump and a negative charge pump to provide adjustable regulated output voltages.

The boost converter provides the regulated supply voltage for the panel source driver ICs. The converter is a 640kHz current-mode regulator with an integrated 16V N-Channel 0.2Ω MOSFET. It provides fast transient response to pulsed loading while achieving efficiency over 85%. The device can produce output voltage as high as 14V from an input as low as 2.7V. FP6787/A includes internal 8ms soft start.

The low dropout (LDO) linear regulator can supply up to 600mA current while input voltage is 5V. It uses an internal PMOS as the pass device. It is suitable for the supply voltage of the timing controller.

The voltage detector monitors the supply voltage to issue a reset signal while the detected voltage is too low. The detecting level is decided by an external resistor divider and the delay time is programmable by an external capacitor.

The VCOM buffer can drive the LCD VCOM voltage that features high short-circuit current (250mA), fast slew rate (12V/μs), wide bandwidth (12MHz) and rail-to-rail inputs and outputs.

The positive charge pump controller provides regulated TFT gate-on voltage. The negative charge pump controller provides regulated TFT gate-off voltage. The regulation of the positive and negative charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal voltage reference.

Features

- High Efficiency
- Low Power Consumption
- 2.7V to 5.5V Input Supply Voltage

640kHz Current-Mode Boost Regulator

- Fast Transient Response to Pulsed Load
- Adjustable Output Voltage with ±1% Accuracy
- Built-In 16V, 3A, 0.2Ω N-Channel MOSFET
- High Efficiency up to 85%
- Built-in 8ms Soft-Start
- Over-Current Protection
- Over-Voltage Protection

Low Dropout Linear Regulator

- 600mA Maximum Output Current
- Fixed Output Voltage : 3.3V (FP6787) and 2.5V (FP6787A)
- ±2% Output Voltage Accuracy

Low Voltage Detector

- Programmable Detection Voltage
- ±2% Detection Voltage Accuracy
- Programmable Reset Delay Time
- Push-Pull Output

Unity-Gain Operation Amplifier for VCOM Buffer

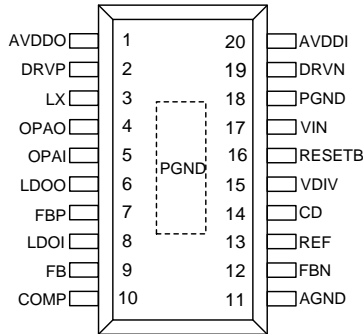
- Rail-to-Rail Input and Output
- 12V/μs Slew Rate and 12MHz Bandwidth
- 250mA Short-Circuit Current
- Charge Pump for VGH Regulation
- Charge Pump for VGL Regulation
- Over-Temperature Protection
- TSSOP-20 And TQFN-20 Exposed Pad Packages
- RoHS Compliant

Applications

- Notebook Computers Displays
- LCD Monitor Panels

Pin Assignments

TP Package (TSSOP-20 Exposed Pad)



WQ Package (TQFN-20, 4mm x 4mm)

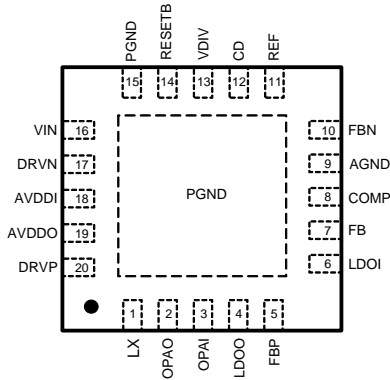
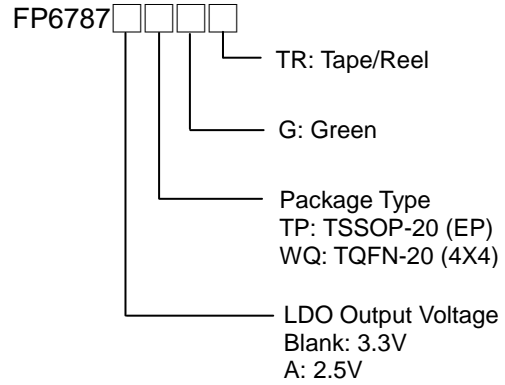


Figure1. Pin Assignment of FP6787/A

Ordering Information



Typical Application Circuit

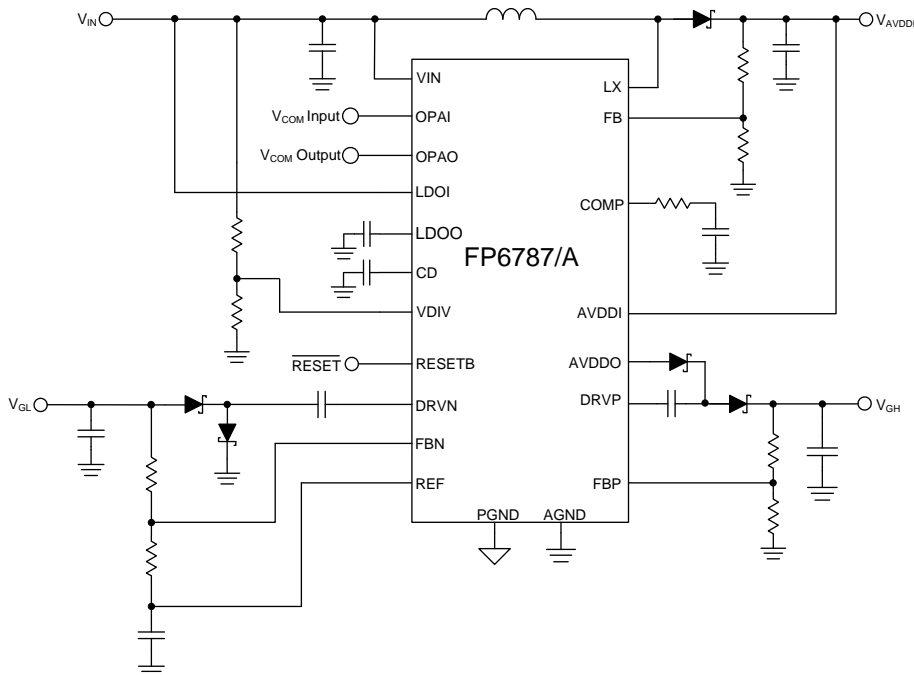


Figure2. Typical Application Circuit of FP6787/A

Functional Pin Description

Pin Name	Pin Function
LX	Switching Pin. Drain of the internal power NMOS for the main step-up regulator.
DRVP	Voltage Driver Output of Positive Charge Pump.
AVDDI	VDD for Source Driver Power. This also supplies the OPA block.
OPAO	Unity-Gain Operational Amplifier Output Pin.
OPAI	Unity-Gain Operational Amplifier Input Pin.
LDOO	Voltage Output of LDO.
LDOI	Voltage Input of LDO.
FBP	Voltage Feedback to Determine Positive Charge Pump Output Voltage. FBP regulates to 1.233V.
AGND	Analog Ground
FB	Main Boost Regulator Feedback Input. FB regulates to 1.233V.
COMP	Compensation Pin for Error Amplifier.
FBN	Negative Charge-Pump Regulator Feedback Input. FBN regulates to 0.25V.
REF	Internal Reference Bypass Terminal.
VDIV	Voltage Detector Divider Input.
RESETB	Voltage Detector Output for Reset. This is push-pull output. The output is pulled low if input voltage falls below detection threshold.
CD	Delay Time Setting Pin. Connect an external capacitor to set the delay time for voltage detector reset delay.
VIN	Power Supply Input. The supply voltage powers all the control circuits.
AVDDO	Connect AVDD Output for Positive Charge Pump Power Sequence Control
DRVN	Voltage Driver Output of Negative Charge Pump
PGND	Power Ground. PGND is the source of boost converter power NMOS.

Absolute Maximum Ratings

- LX, AVDDI, AVDDO, OPAI, OPAO, DRVP, DRVN ----- -0.3V to 18V
- CD, RESETB, VDIV, COMP, FB, FBP, FBN, REF ----- -0.3V to 6V
- VIN, LDOI, LDOO ----- -0.3V to 6V
- PGND, AGND ----- -0.3V to 0.3V
- Power Dissipation @ $T_A=25^{\circ}\text{C}$:
 - TSSOP-20(Exposed Pad) ----- 1.38W
 - TQFN-20 (4mmx4mm) ----- 1.1W
- Package Thermal Resistance (θ_{JA}):
 - TSSOP-20 (Exposed Pad) ----- 40°C/W
 - TQFN-20 (4mmx4mm) ----- 50°C/W
- Lead Temperature (Soldering, 10sec.) ----- 260°C
- Maximum Junction Temperature (T_J) ----- 150°C
- Storage Temperature (T_{STG}) ----- -65°C to 150°C
- ESD Susceptibility
 - HBM(Human Body Mode) ----- 1.5KV
 - MM(Machine Mode) ----- 100V

Note 1 : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{IN}) ----- 2.7V to 5.5V
- Output Voltage of Main Boost Converter (V_{AVDDI}) ----- V_{IN} to 14V
- Operating Temperature Range ----- -40°C to 85°C

Block Diagram

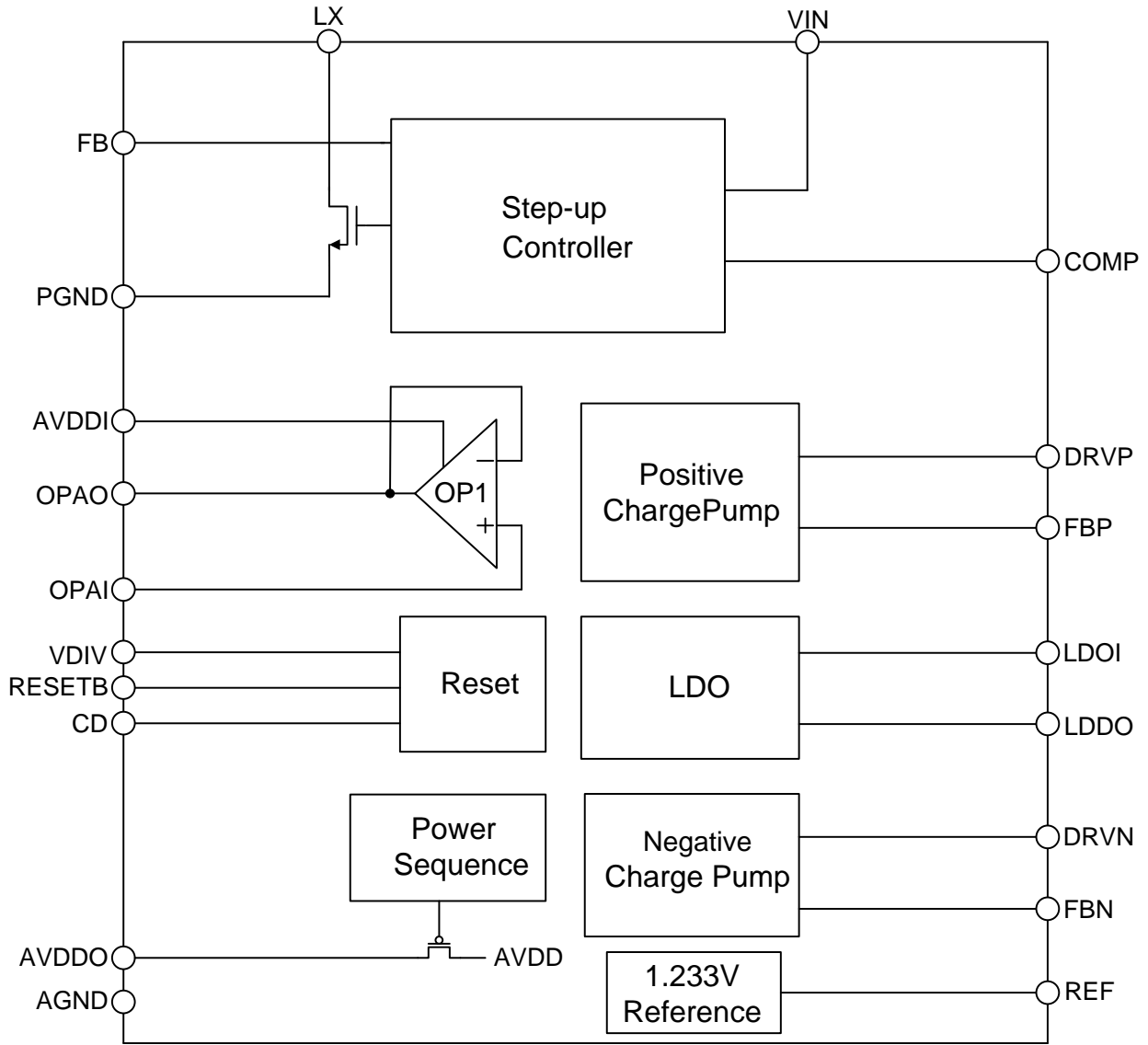


Figure3. Block Diagram of FP6787/A

Electrical Characteristics

($V_{IN}=5V$, $V_{AVDDI}=10V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System Supply						
Input Voltage Range	V_{IN}		2.7		5.5	V
V_{IN} UVLO Threshold	V_{UVLO}	V_{IN} Rising	2.3	2.5	2.7	V
		Hysteresis		0.2		
V_{IN} Supply Current	I_{IN}	$V_{FB}=V_{FBP}=1.4V$ $V_{FBN}=0$	0.5	1	1.5	mA
REF Output Voltage	V_{REF}		1.215	1.233	1.25	V
Thermal Shutdown Threshold (Note2)	T_{SD}			160		$^{\circ}C$
		Hysteresis		20		
Boost Regulator						
Output Voltage Range	V_{AVDDI}		V_{IN}		V_{OVP}	V
Over-Voltage Protection	V_{OVP}		14	15	16	V
Operation Frequency	F_{OSC}		540	640	740	kHz
Maximum Duty Cycle				85		%
Feedback regulation Voltage	V_{FB}	No Load, $T_A=25^{\circ}C$	1.221	1.233	1.245	V
Feedback Input Bias Current	I_{FB}	$V_{FB}=1.5V$		10		nA
Transconductance of Error Amplifier	G_m	$I_{COMP}=5\mu A$		170		$\mu A/V$
Voltage Gain of Error Amplifier	A_v			700		V/V
Switch ON-Resistance	R_{ON}			0.2		Ω
Switch Current Limit (Note2)	I_{LIM}	$V_{FB}=1V$ Duty Cycle=65%		3		A
Switch Leakage Current (Note2)	I_{LX}	$V_{LX}=10V$		0.1		μA
Current Sense Transconductance				3.8		S
Soft-Start Time (Note2)	T_{SS}			8		ms
Low Dropout Linear Regulator (LDO)						
Input Voltage	V_{LDOI}		2.8		5.5	V
LDO Output Voltage	V_{LDO}	FP6787	3.234	3.3	3.366	V
		FP6787A	2.45	2.5	2.55	V
Dropout Voltage	V_{DROP}	FP6787, $I_{OUT}=600mA$			600	mV
		FP6787A, $I_{OUT}=600mA$			800	mV
Current Limit	I_{LIM}		600			mA
Quiescent Current	I_{LDO}		10	30	50	μA
Voltage Detector						
Minimum Operating Voltage			1.6			V
Detecting Voltage Adjustment	V_{DIV}		1.078	1.1	1.122	V
Hysteresis				5		%
CD Pin Charge Current	I_{CD}		4.5	5.5	6.5	μA

Electrical Characteristics (Continued)

($V_{IN}=5V$, $V_{AVDDI}=10V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCOM Buffer						
Supply Voltage Range			4.5		16	V
Supply Current	I_{OP}			1.2		mA
Input Offset Voltage	V_{OS}	$V_{COM}=V_{AVDDI}/2$, $T_A=25^{\circ}C$	-30		30	mV
Input Bias Current	I_{BIAS}		-50	0	50	nA
Output Voltage Swing High	V_{OH}	$I_{OUT}=100\mu A$		AVDDI-5	AVDDI-15	mV
		$I_{OUT}=5mA$		AVDDI-80	AVDDI-150	mV
Output Voltage Swing Low	V_{OL}	$I_{OUT}=-100\mu A$		5	15	mV
		$I_{OUT}=5mA$		80	150	mV
Short-Circuit Current		To $V_{AVDDI}/2$, Source & Sink	150	250		mA
Output Source & Sink Current		To $V_{AVDDI}/2$, Source & Sink	40			mA
-3dB Bandwidth	F_{3DB}			12		MHz
Gain Bandwidth Product	GBW			8		MHz
Slew Rate	SR			12		V/ μs
Positive Charge Pump						
FBP Reference Voltage	V_{FBP}	$I_{DRVP}=100\mu A$	1.202	1.233	1.264	V
FBP Input Bias Current	I_{FBP}	$V_{FBP}=1.4V$	-50	0	50	nA
DRVP PCH On-Resistance		$I_{OUT}=20mA$		8		Ω
DRVP NCH On-Resistance		$I_{OUT}=20mA$		1.1		Ω
Switching Frequency			540	640	740	kHz
Soft-Start Time	T_{SSP}			8		ms
Negative Charge Pump						
FBN Reference Voltage	V_{FBN}	$I_{DRVN}=100\mu A$	235	250	265	mV
FBN Input Bias Current	I_{FBN}	$V_{FBN}=0V$	-50	0	50	nA
DRVN PCH On-Resistance		$I_{OUT}=20mA$		4.4		Ω
DRVN NCH On-Resistance		$I_{OUT}=20mA$		2.6		Ω
Switching Frequency			540	640	740	kHz
Soft-Start Time (Note2)	T_{SSN}			5		ms

Note 2 : Guaranteed by design.

Typical Performance Curves

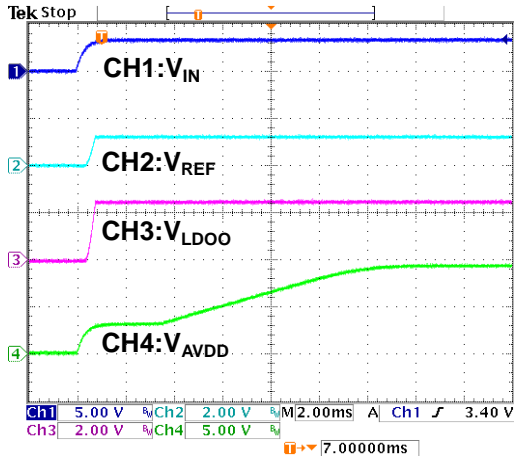


Figure4. Power-up Sequence

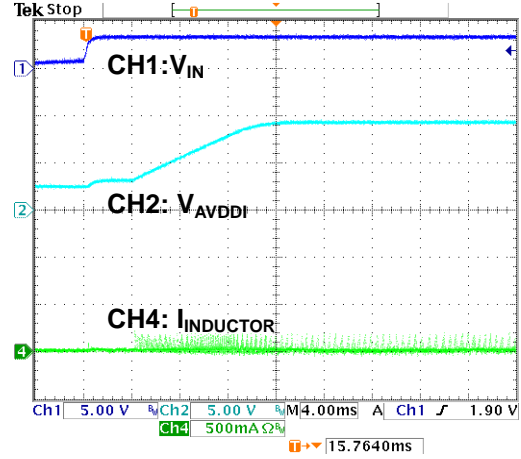


Figure5. Boost Converter Power-up waveform

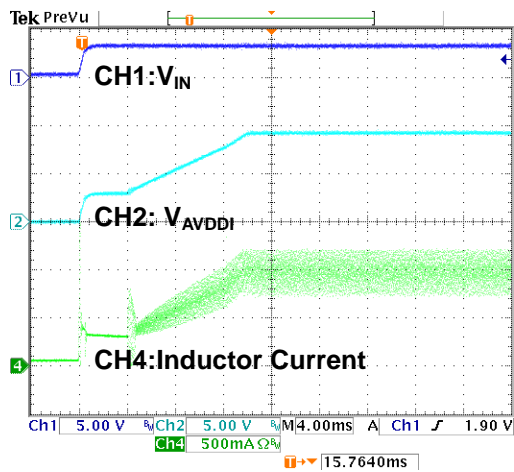


Figure6. Boost Converter Power-up waveform

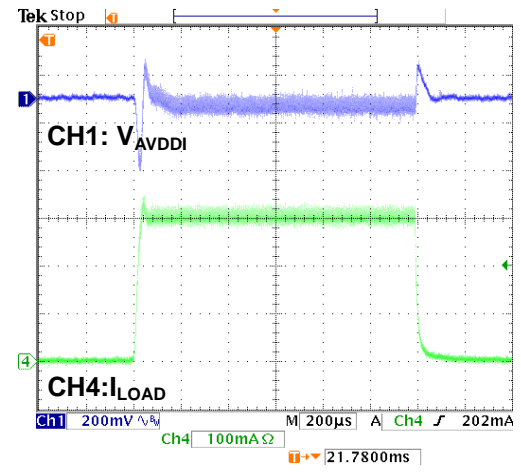


Figure7. Boost Converter Load Transient Response (0→300mA)

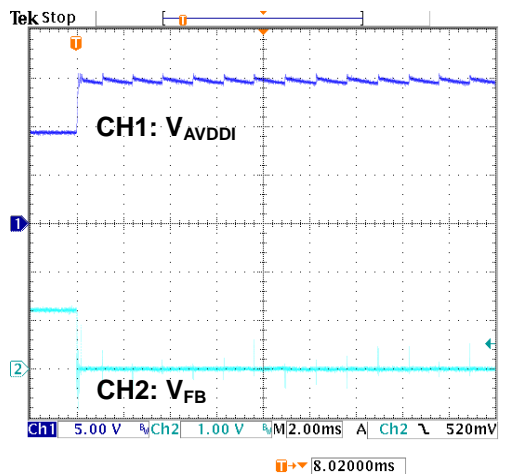


Figure8. Boost converter Over-Voltage Protection Waveform.

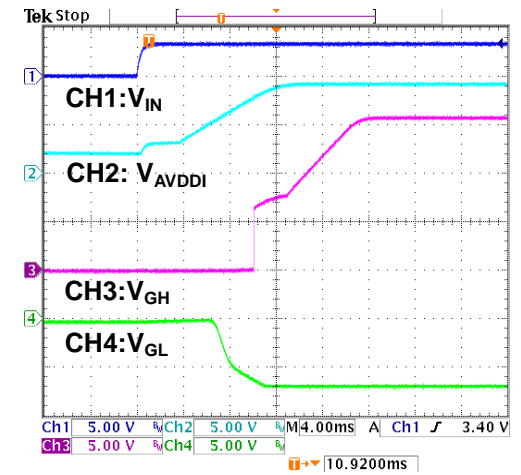


Figure9. Charge Pumps Power-up Sequence

Typical Performance Curves (Continued)

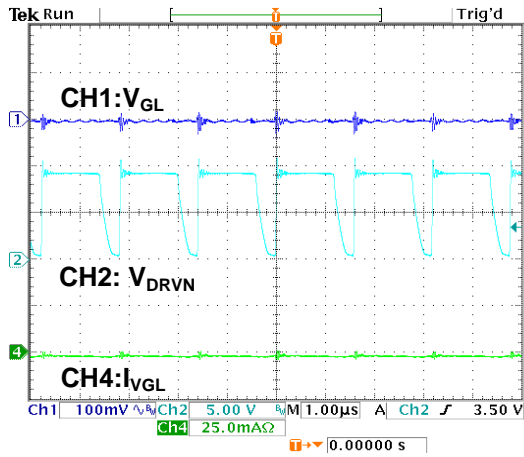


Figure10. VGL operation waveform (Output Current =0mA)

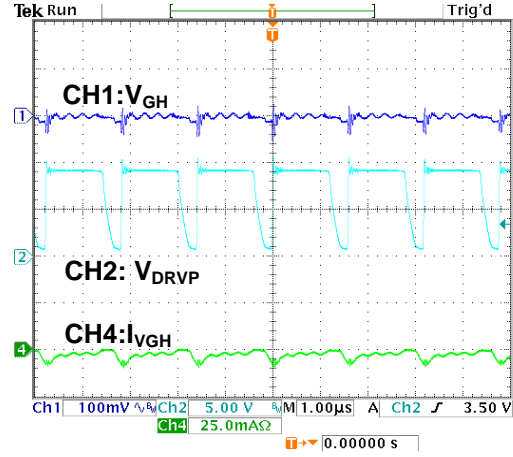


Figure11. VGH operation waveform (Output Current =0mA)

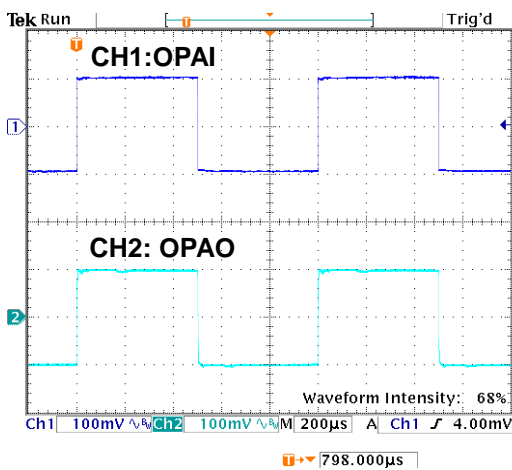


Figure12. Unit-Gain Small-Signal Step Response

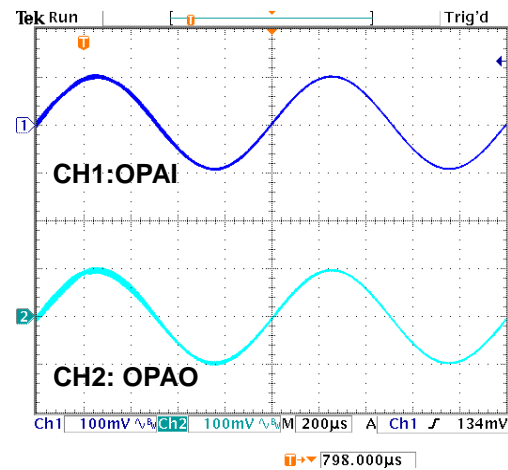


Figure13. Unit-Gain Small-Signal Sine wave Response

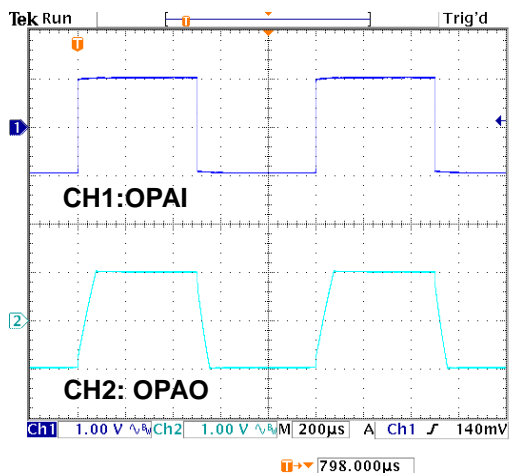


Figure14. Unit-Gain Large-Signal Step Response

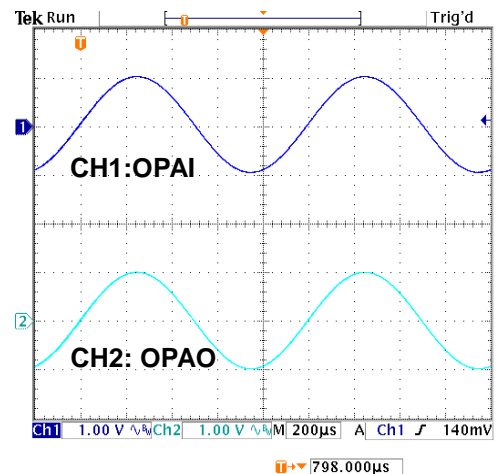


Figure15. Unit-Gain Large-Signal Sine wave Response

Typical Performance Curves (Continued)

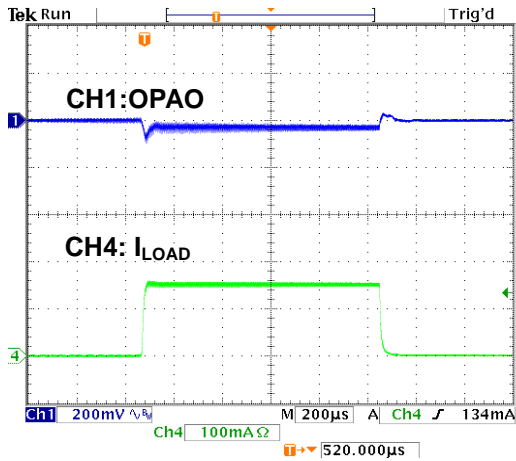


Figure16. Unit-Gain Sink 150mA dynamic load transient

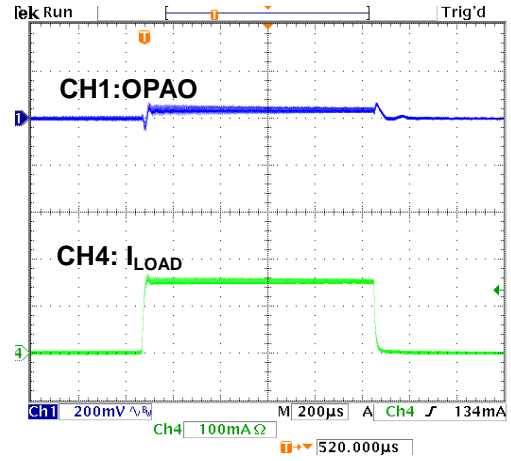


Figure17. Unit-Gain Source 150mA dynamic load transient

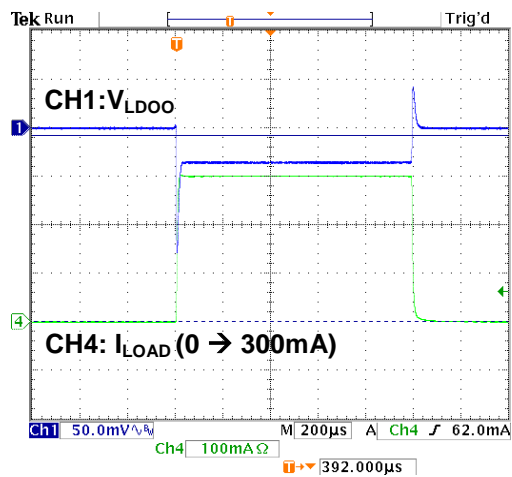


Figure18. LDO Load Transient Response

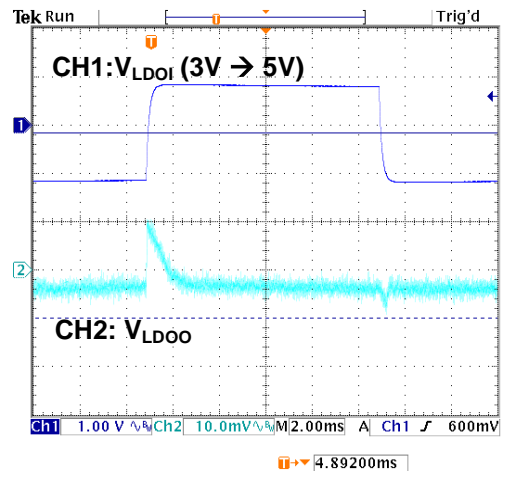


Figure19. LDO Line Transient Response

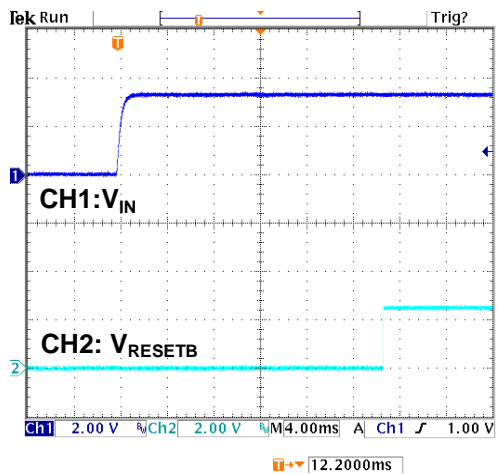


Figure20. Reset Power on

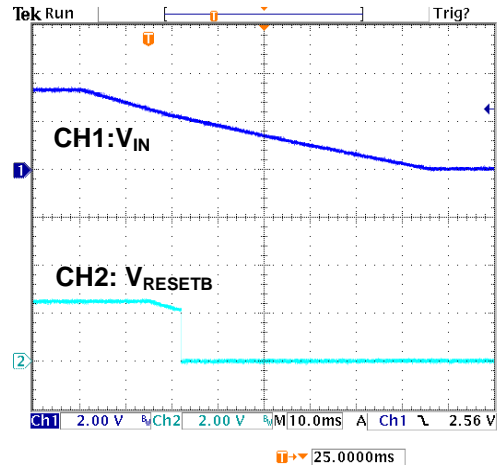


Figure21. Reset Power off

Typical Performance Curves (Continued)

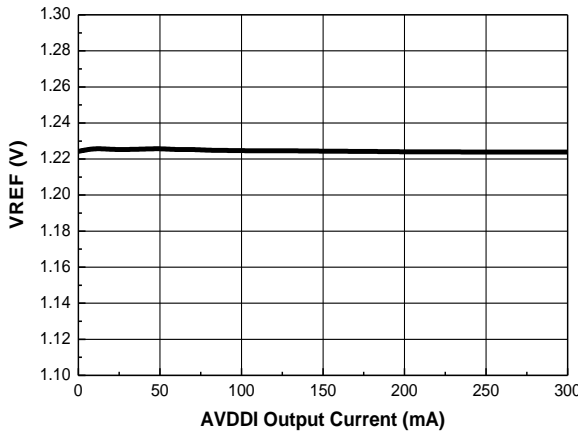


Figure22. VREF vs. Boost Converter Output Current

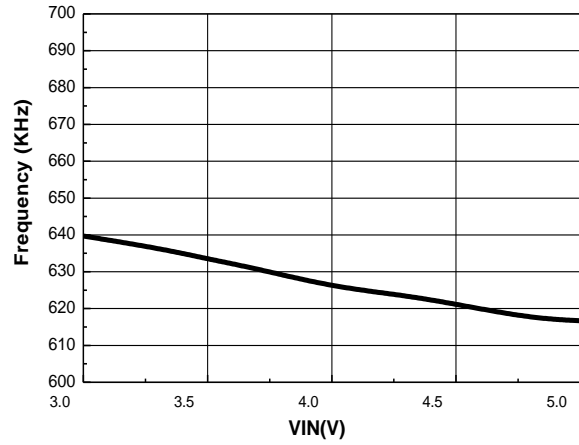


Figure23. Switching Frequency vs. Vin

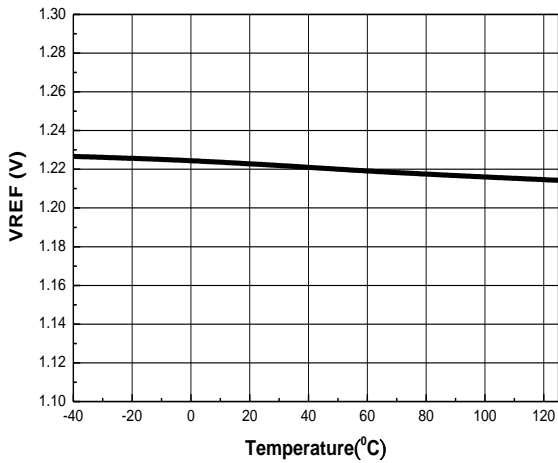


Figure24. VREF vs. Temperature

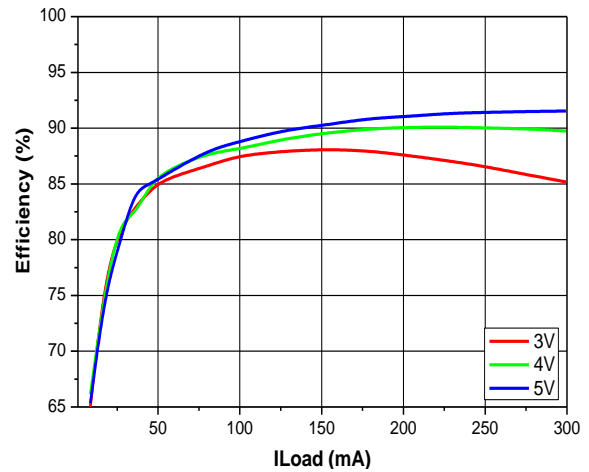


Figure25. Boost Converter Efficiency

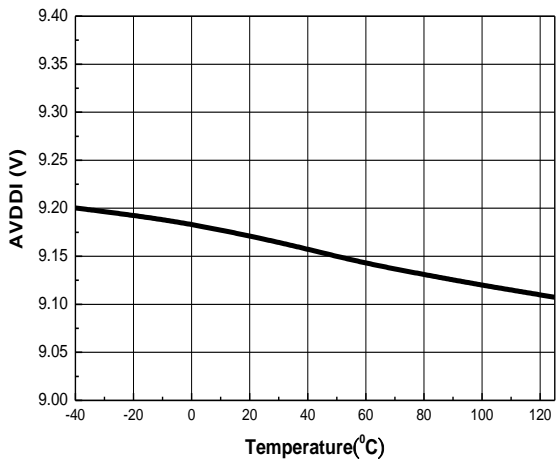


Figure26. Boost Converter Output Voltage vs. Temperature

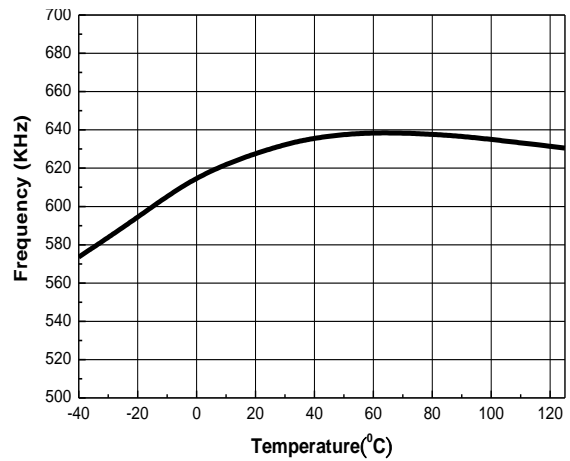


Figure27. Switching Frequency vs. Temperature

Typical Performance Curves (Continued)

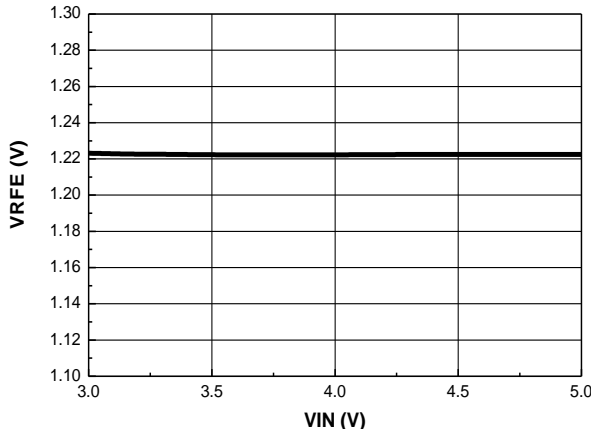


Figure28. VREF vs. VIN

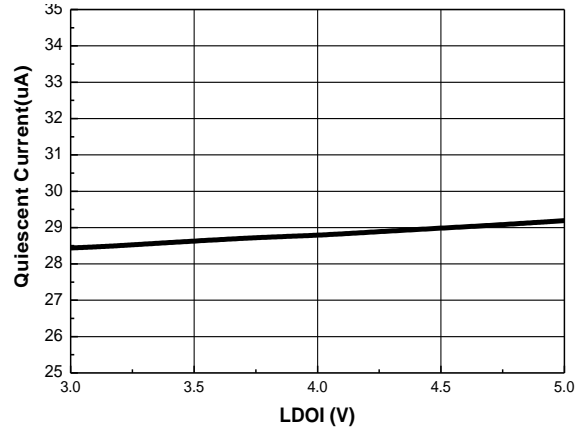


Figure29. LDO Quiescent Current vs. LDO Input Voltage

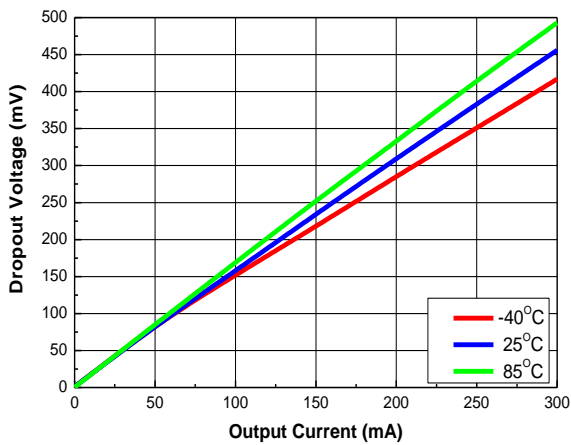


Figure30. LDO Dropout Voltage vs. Output current

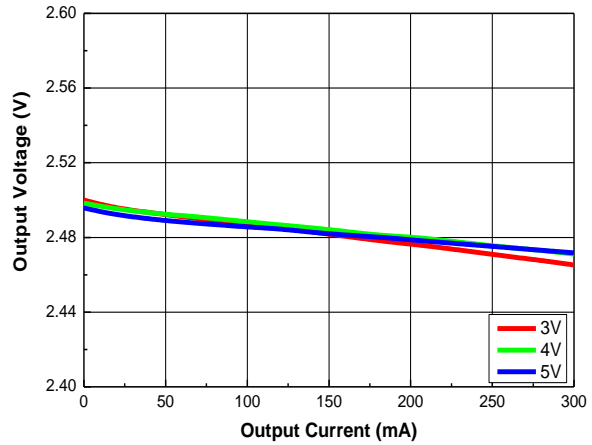


Figure31. LDO Output Voltage vs. Output Current

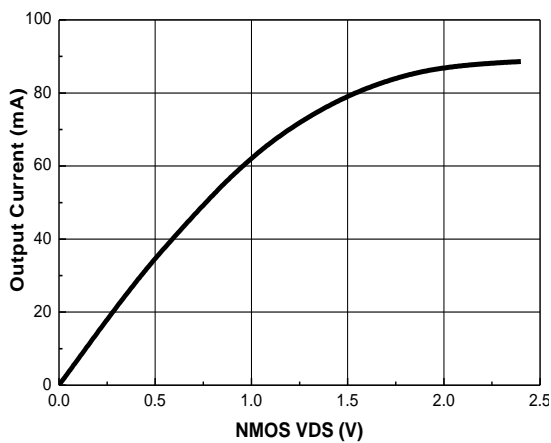


Figure32. Reset Output NMOS Driving Ability

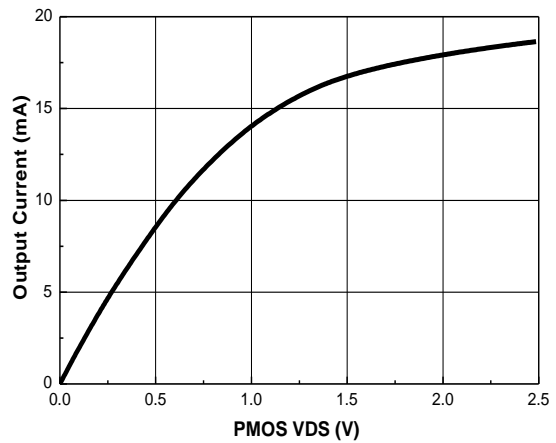


Figure33. Reset Output PMOS Driving Ability

Typical Performance Curves (Continued)

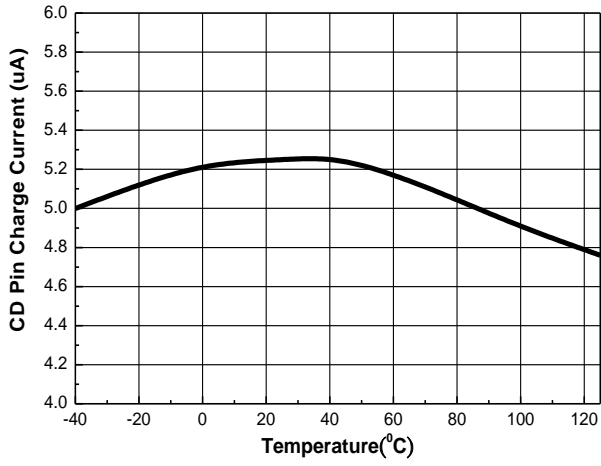


Figure 34. CD Pin Charge Current V.S. Temperature

Functional Description

Introduction

The FP6787/A represents DC/DC regulator to provide a complete power solution for active matrix thin-film transistor liquid crystal display (TFT-LCD) applications. It contains a high performance boost regulator to generate voltage for the panel source driver ICs, a low dropout (LDO) linear regulator is suitable for supply voltage of the timing controller, a positive charge pump and negative charge pump provide regulated TFT gate-on and gate-off voltage, a unity-gain OPA can drive the VCOM (LCD backplane), and a voltage detector monitors the supply voltage. The FP6787/A also consists of a precision 1.233V reference, current-limited, soft-start, power-up sequencing and thermal shutdown. The following content includes detailed description and information of the component selection in the general application circuit as shown in Figure 36.

Boost Regulator

The boost regulator can operate in both discontinuous conduction mode (DCM) at light load and continuous conduction mode (CCM). In continuous current mode, current flows continuously in the inductor during entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by :

$$\frac{V_{AVDDI}}{V_{IN}} = \frac{1}{1-D}$$

Where D is the duty cycle of the switching MOSFET. The boost regulator uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback and slop compensation. A comparator monitors the peak inductor current cycle by cycle and terminates the PWM cycle if it reaches the current limit. To add higher flexibility to the selection of external component values, the device uses external loop compensation.

Soft Start

The FP6787/A provides internal 8ms soft-start function to minimize the inrush current. When power is on, a constant current will charge the internal capacitor. The inductor peak current will be limited during the charging period. In the meanwhile, the frequency increases slowly at the beginning. When power is off, the internal capacitor will be discharged for next soft-start time.

Compensation

The boost converter of FP6787/A can be compensated by a RC network connected from COMP pin to ground. The external compensation network consists of R8, C9, and C10 as shown in figure 36. The larger value resistor and lower value capacitor can reduce the transient overshoot. R8 is used to set the high-frequency integrator gain for fast transient response. While R8 is decided, C10 is chosen to set the integrator zero to maintain the loop stability. C9 is used to cancel the zero caused by the output capacitor and its ESR.

For each components of external compensation network, the above equations provide the approximate calculations. In order to obtain better transient performance, it is necessary to adjust the component values of external compensation network.

Over Current Protection

The FP6787/A boost converter has over current protection to limit peak inductor current. It prevents inrush current damaging the external component (inductor, diode, capacitor etc.) and IC. When peak inductor current reaches current limit during the ON-time, the over current protection function will work. The action of protection function will terminate the internal LX switch and shorten the duty cycle. When the over current protection is relieved, the chip will operate well again. Therefore, the output voltage will drop if the over current condition occurs. Actual current limit is always larger than the nominal value because of the internal circuit delay. Current limit is also affected by the input voltage, duty cycle and inductor value. The switch current is monitored to limit the value not to exceed 3A typically. When the switch current reaches 3A, the NMOS will be turned-off so that the output voltage will be pulled down to limit the total output power to protect the power switch and external components.

Over Voltage Protection

The over-voltage protection is detected by detecting circuit. Connect the AVDDI pin to output terminal to monitor boost output voltage. Once V_{AVDDI} goes over the detecting voltage, LX pin will stop switching. When the over-voltage protection is released, the chip will operate well again.

Functional Description (Continued)

Over Temperature Protection

Over temperature protection function is integrated in the chip. The thermal protection function prevents the excessive power dissipation from overheating. When the chip temperature is higher than 160°C, the controller will be shutdown. 20°C is the hysteresis range of temperature to product time gap for IC cooling down. When the thermal protection is released, the chip will operate well again.

Under Voltage Lockout Protection

When power is on, the chip will keep in shutdown mode till the input voltage V_{IN} reaches 2.3V. 200mV is the hysteresis range of voltage to prevent unstable operation when the under voltage lock-out protection happens. The under voltage lock-out circuit is adopted as a voltage detector and always monitors the supply voltage (V_{IN}).

Reset Control

The RESETB pin is a push-pull output. The RESETB output voltage follows the voltage of LDOO pin. The output pulls low when the voltage of VDIV falls below detection threshold. The VDIV pin is a voltage sense terminal. An external resistor divider connects with VDIV pin. This resistor divider is required to divide the input voltage down to the nominal threshold voltage. The values of resistor are determined by the following formula:

$$\frac{R_{12}}{R_{11}+R_{12}} \times V_{IN(MIN)} = 1.1V$$

Where detecting voltage = 1.1V (Typical)

5% is the hysteresis range of voltage to prevent unstable operation. Connect an external capacitor to CD pin to set the delay time for voltage detector reset delay. The reset delay time can be calculated by:

$$T_D = C_8 \times \frac{1.1V}{5.5\mu A}$$

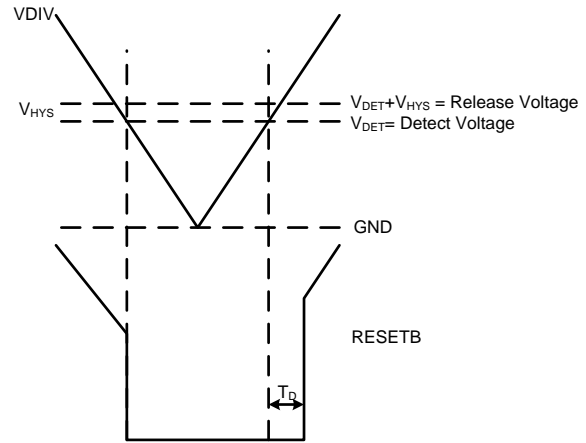


Figure.35

Linear regulator

The low dropout (LDO) linear regulator can supply up to 600mA output current with 800mV dropout voltage. It uses an internal PMOS as the pass device.

Output Voltage of Boost Converter

External resistor dividers are required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. The boost converter output voltage is determined by the following equation:

$$V_{ADD} = \frac{R_5 + R_6}{R_6} \times V_{FB} = \left(1 + \frac{R_5}{R_6}\right) \times 1.233$$

Where V_{FB} is the feedback voltage, 1.233V typical.

Output Voltage of Positive Charge Pump

Output voltage of positive charge pump is determined by connecting an external resistor divider. The external resistor divider connects with FBP pin. The output voltage of positive charge pump is determined by the following equation:

$$V_{POS} = \frac{R_1 + R_2}{R_2} \times V_{FBP} = \left(1 + \frac{R_1}{R_2}\right) \times 1.233$$

Functional Description (Continued)

Where V_{POS} is the output voltage of positive charge pump. V_{FBP} is the feedback voltage of positive charge pump, 1.233V typical.

Output Voltage of Negative Charge Pump

Since comparator input of negative charge pump, FBN pin, is referenced to 0.25V, a positive reference voltage, which can be obtained by adding a bypass capacitor between VREF pin and ground. The output voltage of negative charge pump is determined by the following equation:

$$V_{NEG} = V_{FBN} \times \left(1 + \frac{R_{13}}{R_{14}}\right) - V_{REF} \times \frac{R_{13}}{R_{14}} = 0.25 \times \left(1 + \frac{R_{13}}{R_{14}}\right) - 1.233 \times \frac{R_{13}}{R_{14}}$$

Where V_{NEG} is the represent output voltage of negative charge pump. V_{REF} is the reference voltage, 1.233V typical. V_{FBN} is the feedback voltage of negative charge pump, 0.25V typical.

The VCOM amplifier is designed to control the voltage on the back plate of TFT-LCD display. This plate is capacitive coupled to the pixel drive voltage which alternately cycles positive and negative at the line rate for the display. Thus the amplifier must be capable of sourcing and sinking capacitive pulses of current, which can occasionally be quite large.

The FP6787/A VCOM amplifier's output current is limited to 250mA in typically. This limit level, which roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen on the μs time scale in practical systems, the VCOM voltage will have settled again before the next line is processed.

Power-Up Sequencing

The FP6787/A goes through start-up power sequence after power-up. First V_{in} reaches UVLO threshold, then reference voltage start-up. Next, LDO regulator start-up, then boost converter and negative charge pump start-up. The boost's voltage achieves the setting value after approximate 8ms. Next, the positive charge pump start-up to reach the target level. (Reference Figure.9)

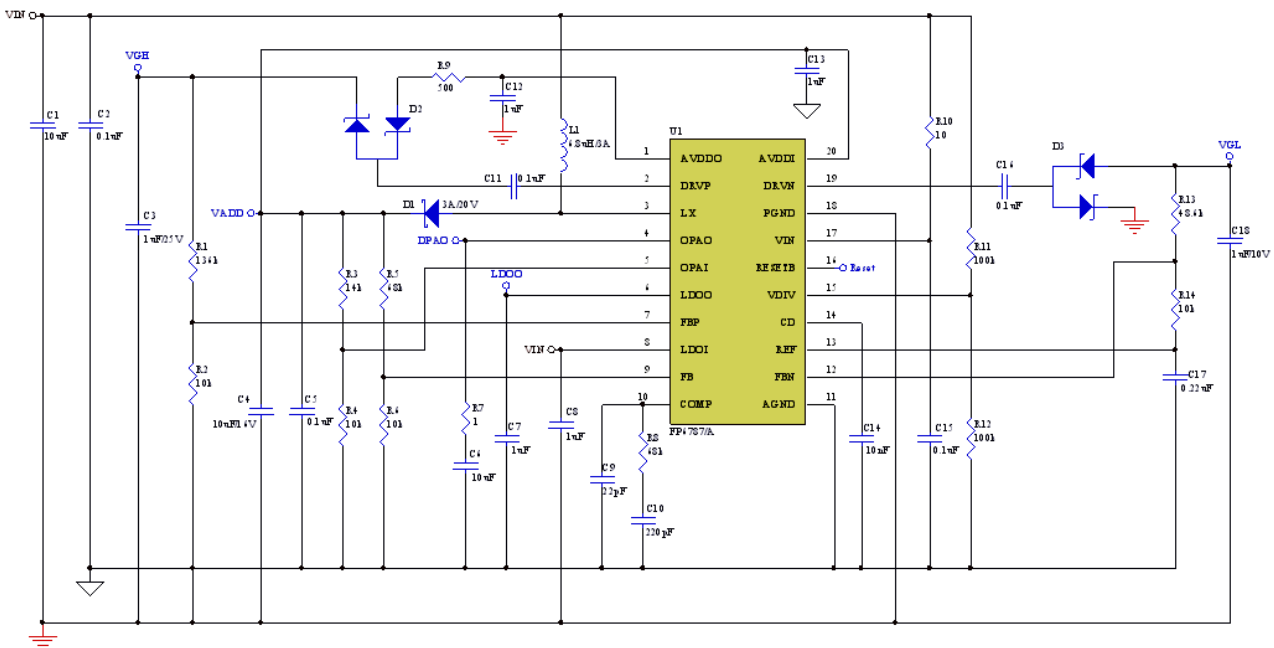


Figure.36

Application Information

Inductor Selection

Although small physical size and high efficiency are major concerns, the inductor should have low core losses at 640 kHz and series resistance (DCR, copper wire resistance). The minimum inductor value, peak current rating and series resistance will affect the converter efficiency, maximum output load capability, transient response time and output voltage ripple. The inductor selection depends on input voltage, output voltage and maximum output current, Very high inductor value minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and conduct losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire. The size of inductor will become bigger and increase conduct losses. Low inductor values decrease the size but increase the current ripple and the peak current. Choosing the inductor values is based on the application.

The inductor selection depends on the switching frequency and current ripple by the following formula:

$$L \geq \frac{V_{IN}}{f_{OSC} \times \Delta I_L} \left(1 - \frac{V_{IN}}{V_{OUT}} \right)$$

where f_{OSC} is the 640kHz switching frequency of the FP6787/A. ΔI_L is the inductor ripple current.

In addition, it is important to ensure the inductor saturation current exceeds the peak value of inductor current in application to prevent core saturation. Calculate the ripple current at the operating point and the peak current required for the inductor:

$$\Delta I_L = V_O \left[\left(1 - \frac{V_O}{V_I} \right) / (L \times f_{OSC}) \right]$$

$$I_{L(MAX)} = I_{O(max)} + \frac{\Delta I_L}{2}$$

Rectifier Diode Selection

A high-speed diode is necessary due to the high switching frequency. The Schottky diode is recommended because of their fast recovery time and low forward drop voltage for better efficiency. The forward drop voltage of Schottky diode will result in the conduction losses in the diode, and the diode capacitance (C_T or C_D) will cause the switching losses. Therefore, it is necessary to consider both forward voltage drop and diode capacitance for diode selection. In addition, the reverse voltage rating of this diode should 1.3 times of the maximum output voltage. The rectifier diode must meet the peak inductor current requirement.

Flying Capacitor Selection

Increase of flying capacitor value results in a rise of output capability with smaller ripple voltage, therefore flying capacitor is an important component in charge pump system. The voltage rating for flying capacitor value is given by:

$$V_{CFLY} > 1.5 \times (V_{IN} \times N)$$

Where V_{CFLY} is the voltage rating of charge pump flying capacitor, N is number of charge pump stages.

Output Capacitor Selection

The FP6787/A is permissible in using ceramic capacitor for TFT LCD panel application. The value of capacitor depends on acceptable voltage ripple. Selecting an output capacitor must consider the output ripple voltage and the ripple current. The ESR of capacitor is a major factor to the output ripple. For lower output voltage ripple, the low ESR ceramic capacitor is recommended. The ripple voltage is given by:

$$\Delta V_O = \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_O} \right)$$

The common aluminum-electrolytic capacitors have high ESR and should be avoided. Ceramic capacitors have the lowest ESR in general.

Input Capacitor Selection

The input capacitor can reduced peak current and noise at power source. It should have 10 μ F at least and can be increased for better input voltage filtering. For better input bypassing, low ESR ceramic capacitor is recommended for better performance.

Output Capacitor of Charge Pump Selection

The capacitor which tenfold flying capacitor is suitable for the output capacitor of charge pump.

Application Information (Continued)

Layout Recommendation

For high frequency switching power supplies, the device's performance including efficiency, output noise, transient response and control loop stability are dramatically affected by the PCB layout. There are some general guidelines for layout:

1. The PGND and AGND pin must connect to the exposed pad directly to avoid voltage difference between PGND and AGND.
2. Place the external power components (input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. The traces, which connect to these components, should be as short and wide as possible to minimize parasitic inductance and resistance.
3. Place V_{IN} bypass capacitor close to the pin.
4. Place LDO's input and output capacitor close to the IC.
5. The feedback network should sense the output voltage directly from the point of load, and be as far away from noisy loop as possible.
6. The compensation circuit should be away from the power loops and should be shielded with a ground trace to prevent noise coupling.
7. The exposed pad, on the underneath of the package, should be soldered to an equivalent area of metal PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers to maximize thermal dissipation away from IC.
8. The power ground (PGND) consists of input and output capacitor grounds. The PGND should be wide and short enough to connect to a ground plane. The analog ground (AGND) consists of the ground of compensation, delay capacitor, FB divider and OPA divider.

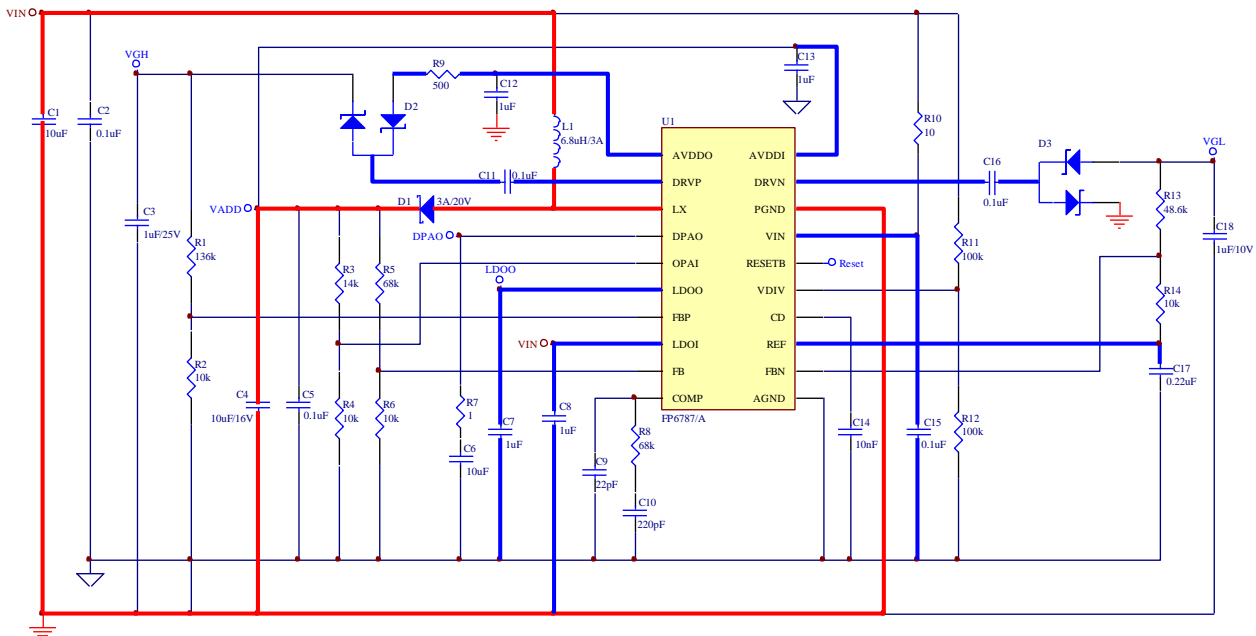
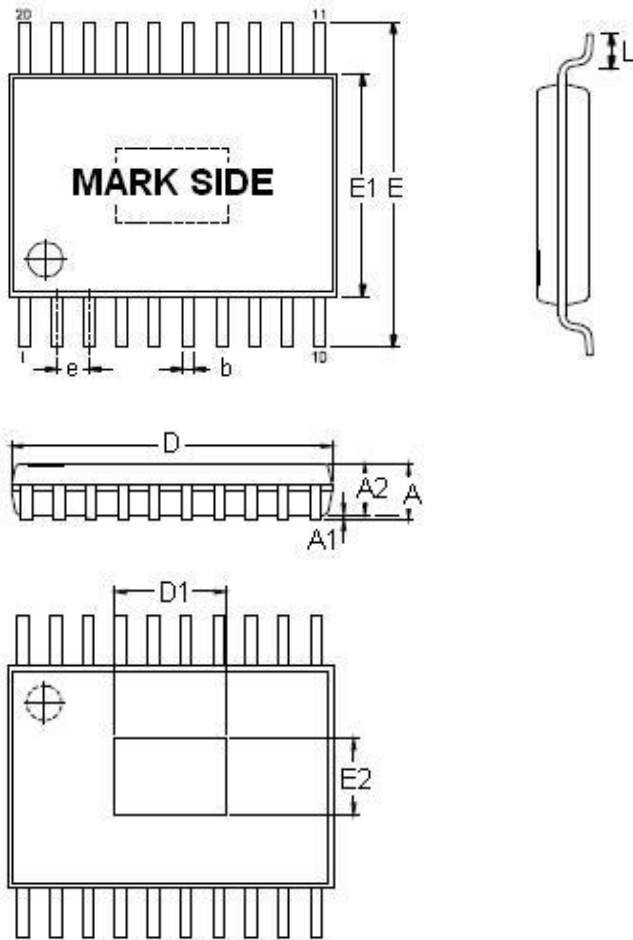


Figure 37

Outline Information

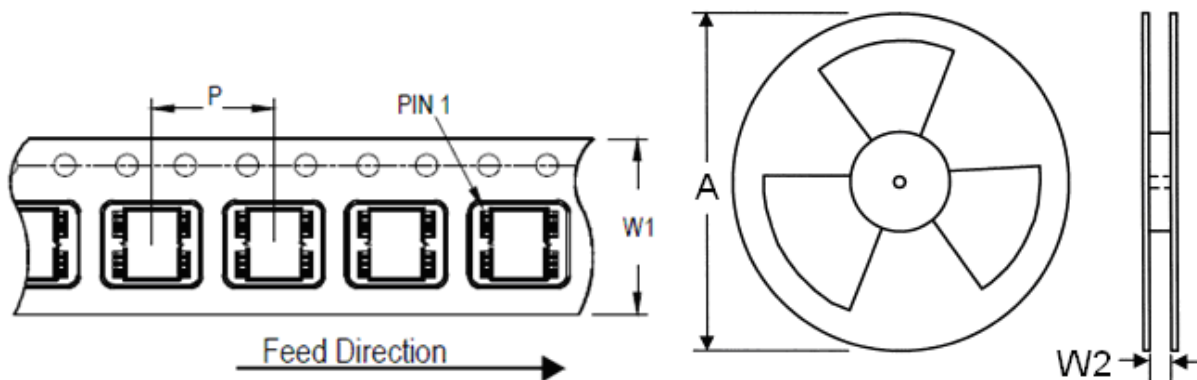
TSSOP-20 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.80	1.20
A1	0.00	0.15
A2	0.80	1.05
b	0.19	0.30
D	6.40	6.60
E1	4.30	4.50
E	6.20	6.60
e	0.55	0.75
L	0.45	0.75
D1	3.40	3.80
E2	2.50	3.20

Note : Followed From JEDEC MO-153-F.

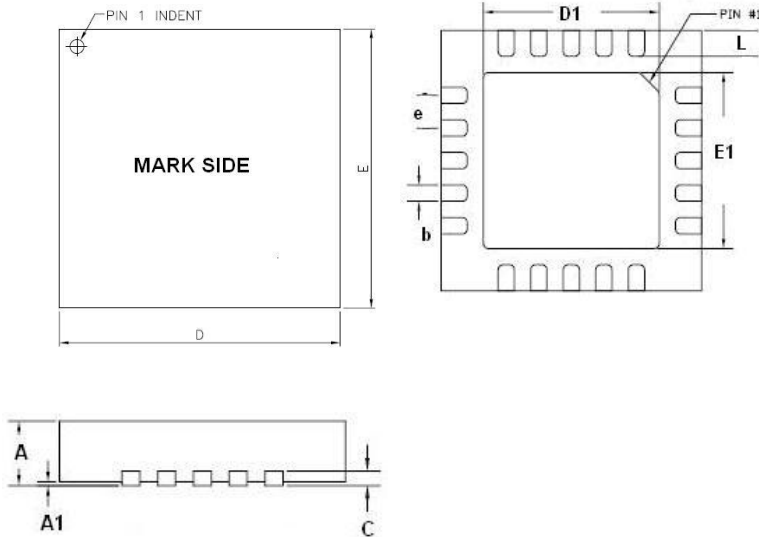
Carrier dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
16	8	13	330	16.4	400~1000	2,500

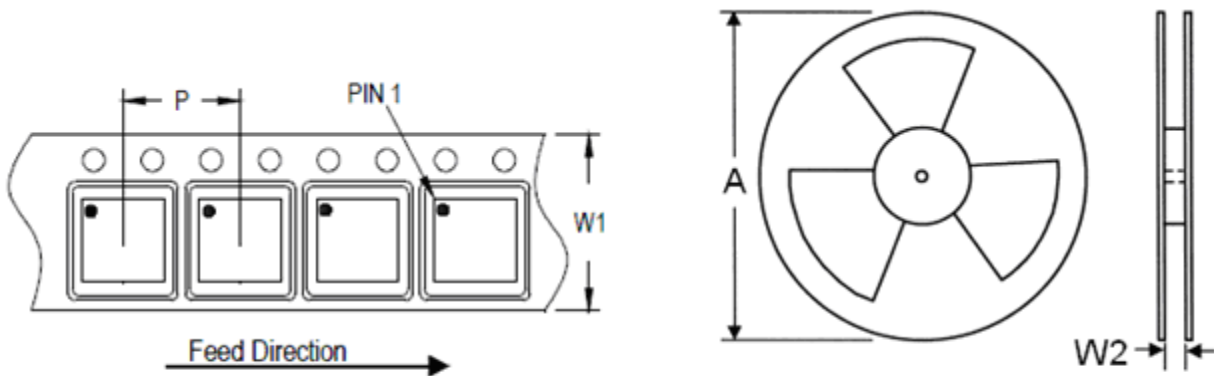
Outline Information (Continued)

TQFN-20, 4mm x 4mm Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
C	0.18	0.30
E	3.95	4.05
E1	2.10	2.80
D	3.95	4.05
D1	2.10	2.80
L	0.30	0.45
b	0.18	0.30
e	0.45	0.55

Carrier dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	3,000

Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.