Microprocessor Reset Circuits with Short Delay Time

Description

The FP6808 is a cost-effective system supervisor circuit designed to monitor microprocessor voltage and V_{DD} in digital systems. This device provides a reset signal to the host processor when necessary.

The circuit asserts a reset signal whenever the V_{DD} supply voltage declines below a preset threshold. It keeps reset signal asserted for at least 20ms after V_{DD} has risen above the reset threshold.

The FP6808-N has an open-drain active-low output stage, while FP6808-C has a push-pull active-low output. The FP6808-N's open-drain output requires a pull-up resistor.

The FP6808 is optimized to reject fast transient glitches on the V_{DD} line. Low supply current makes this device suitable for portable equipment.

Features

- Precision V_{DD} Monitor for 2.5V, 3.0V, 3.3V and 5.0V Supplies
- Precision Monitoring Voltages from 1.6V to 5.0V Available in 100mV Steps
- 20ms Guaranteed Minimum Reset Output Duration
- Low Supply Current
- ±2% High Precision Detection Voltage
- V_{DD} Transient Immunity
- No External Components
- Guaranteed Reset Valid to V_{DD}=1V
- Available in Two Output Configurations
  - Open-Drain Output (FP6808-N)
  - Push-Pull Output (FP6808-C)
- RoHS Compliant
- Small SOT-23-5 Package

Applications

- Computer
- Battery Powered Equipment
- Microprocessor Power Supply Monitoring
- Controller
- Embedded System
- Automotive

Pin Assignments

S5 Package (SOT-23-5)

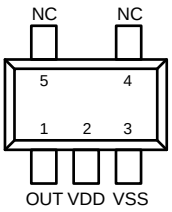


Figure 1. Pin Assignment of FP6808

SOT-23-5 Marking

Part Number	Product Code	Part Number	Product Code
FP6808-23NS5P	**Ca**	FP6808-23CS5P	**Ck**
FP6808-26NS5P	**Cb**	FP6808-26CS5P	**Cm**
FP6808-29NS5P	**Cd**	FP6808-29CS5P	**Cn**
FP6808-31NS5P	**Ce**	FP6808-31CS5P	**Cr**
FP6808-40NS5P	**Cf**	FP6808-40CS5P	**Cs**
FP6808-44NS5P	**Ch**	FP6808-44CS5P	**Ct**
FP6808-46NS5P	**Ci**	FP6808-46CS5P	**Cu**

Ordering Information

FP6808-□□□□□

- TR: Tape/Reel
  Blank: Tube
- P: Green
- Package Type
  S5: SOT-23-5
- C: Push-Pull
  N: Open-Drain
- Reset Voltage
  23: 2.3V
  26: 2.6V
  29: 2.9V
  31: 3.1V
  40: 4.0V
  44: 4.4V
  46: 4.6V

Typical Application Circuit

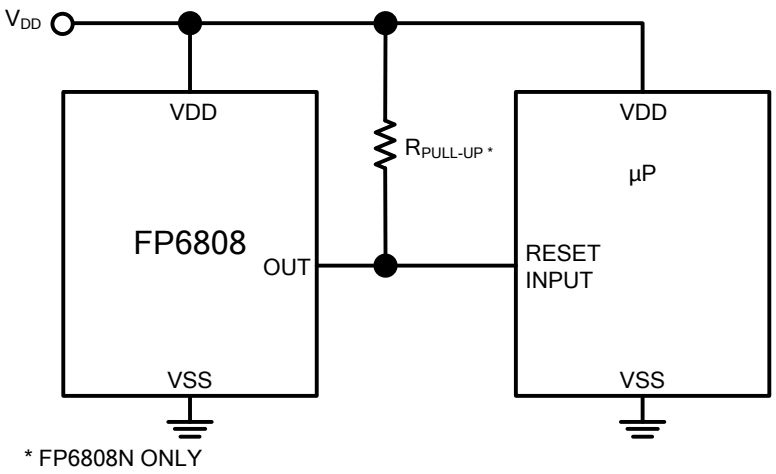


Figure 2. Typical Application Circuit of FP6808

Functional Pin Description

Pin Name	Pin Function
OUT	Voltage Detection Output Pin.
VDD	Voltage Input Pin.
VSS	GND Pin.
NC*1	No Connection.

Note: *1. The NC pin is electrically open. The NC pin can be connected to VDD or VSS

Block Diagram

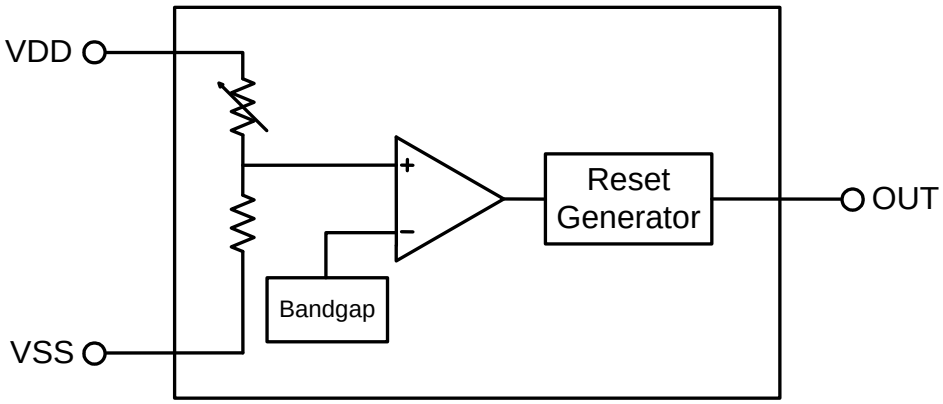


Figure 3. Block Diagram of FP6808

Absolute Maximum Ratings

- Supply Voltage (V_{DD} to V_{SS}) ---------- -0.3V to +6V
- Output Voltage (Push-Pull) ---------- -0.3 to (V_{DD}+0.3V)
- Output Voltage (Open Drain) ---------- -0.3V to (V_{DD}+0.3V)
- Input Current (V_{DD}) ---------- 20mA
- Output Current (I_{OUT}) ---------- 20mA
- Rate of Rise (V_{DD}) ---------- 100V/μs
- Power Dissipation, P_D @T_A=25ºC

  SOT-23-5 ---------- +400mW
- Operating Temperature Range (T_A) ---------- -40°C to +105°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10s) ---------- +300°C

Note：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage (V_{DD} to V_{SS}) ---------- +1.0V to +5.5V
- Operation Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{DD} =full range, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
V_{DD} Range	V_{DD}		1.0		5.5	µA
Supply Current	I_{DD}	V_{DD} <5.5V, FP6808-46/44/40		3		µA
		V_{DD} <3.6V, FP6808-23/26/29/31		3		
Reset Threshold	V_{TH}	FP6808-46	4.54	4.63	4.72	V
		FP6808-44	4.29	4.38	4.47	
		FP6808-40	3.92	4.00	4.08	
		FP6808-31	3.02	3.08	3.14	
Reset Threshold	V_{TH}	FP6808-29	2.87	2.93	2.99	V
		FP6808-26	2.58	2.63	2.68	
		FP6808-23	2.27	2.32	2.37	
Reset Threshold Tempco				30		ppm/°C
V_{DD} to Reset Delay		V_{DD} =V_{TH} to (Vth-100mV)		20		µs
Reset Active Timeout Period			20	40	60	ms
Output Voltage Low (Push-Pull and Open-Drain)	V_{OL}	V_{DD} =V_{TH} min, I_{SINK}=1.2mA, FP6808-23/26/29/31			0.3	V
		V_{DD} =V_{TH} min, I_{SINK}=3.2mA, FP6808-44/46			0.4	
		V_{DD} >1.0V, I_{SINK}=50µA			0.3	
Output Voltage High (push-pull)	V_{OH}	V_{DD} > V_{TH} max, I_{SOURCE}=500µA, FP6808-23/26/29/31	0.8 V_{DD}			
		V_{DD} > V_{TH} max, I_{SOURCE}=800µA, FP6808-44/46	V_{DD} -1.5			
Output Open-Drain Output Leakage Current (FP6808-N)		V_{DD} > V_{TH}, RESET deasserted				µA

Typical Performance Curves

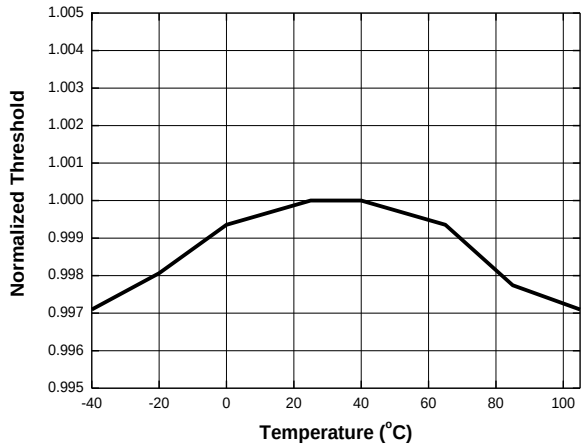


Figure 4. Normalized Reset Threshold vs. Temperature

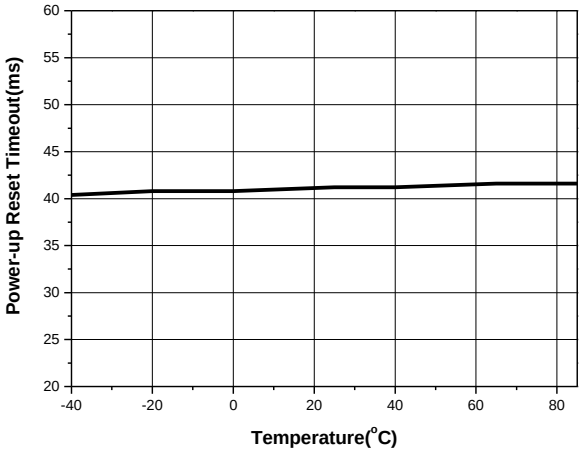


Figure 5. Power-up Timeout vs. Temperature

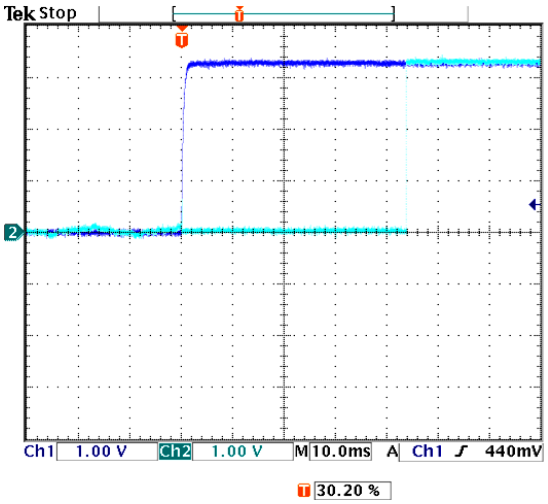


Figure 6. Power-Up $\overline{\text{RESET}}$ Timeout Waveforms;
Ch1: VDD Ch2: OUT

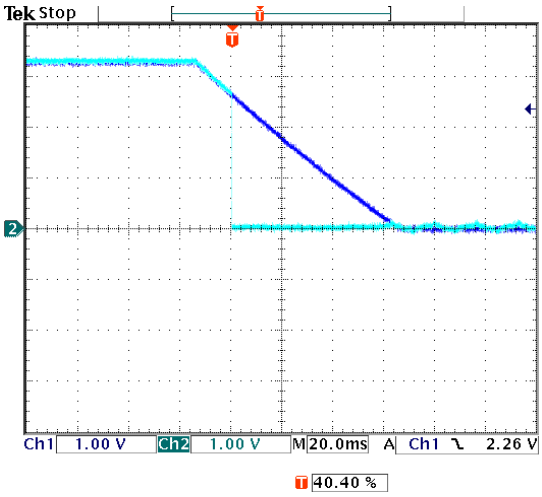


Figure 7. Power-Down $\overline{\text{RESET}}$ Delay Waveforms;
Ch1: VDD Ch2: OUT

Typical Performance Curves (Continued)

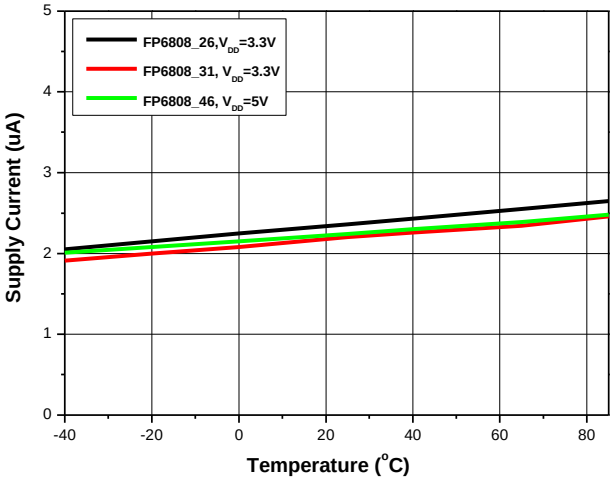


Figure 8. Supply Current vs. Temperature

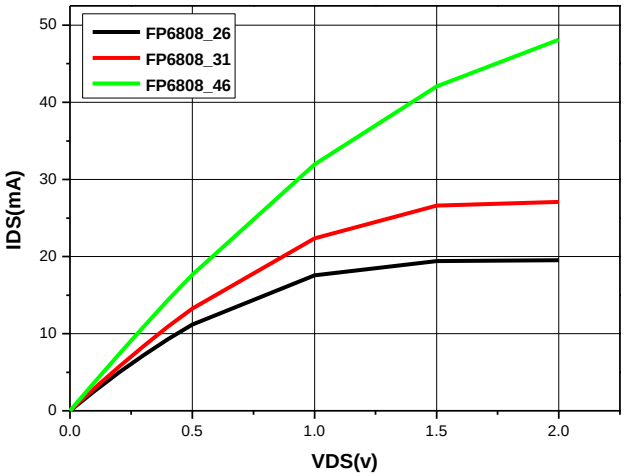


Figure 9. Output Sinking Capability

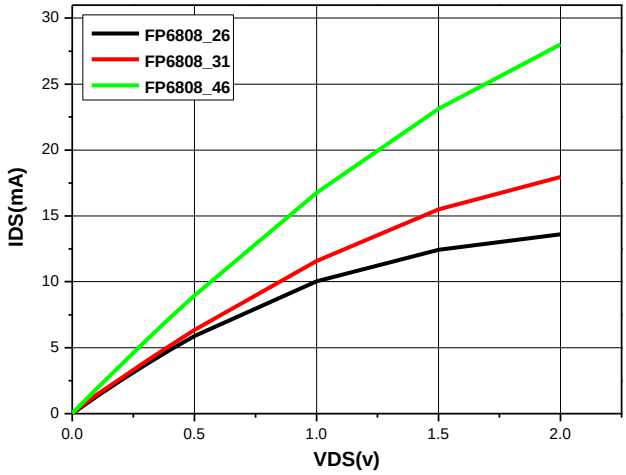


Figure 10. Output Sourcing Capability

Functional Description

FP6808 is supervisory circuit, monitoring critical voltages and asserting reset signal to the subsequent devices. The reset signal can start the microprocessor in a known state, avoiding code-execution errors during power-up, power-down or brownout conditions. OUT is guaranteed to be a logic low for $V_{TH} > V_{CC} > 0.9V$. Once V_{CC} exceeds the reset threshold, an internal timer will keep OUT low for the reset timeout. After this period, OUT will go high. If V_{CC} falls below the reset threshold, OUT will go low immediately.

Whenever V_{CC} drops below V_{TH}, the internal timer will reset to zero and OUT will go low. The internal timer will keep activated only when $V_{CC} > V_{TH}$, and OUT remains low for the reset timeout interval.

Application Information

Benefits of Highly Accurate Reset Threshold

Most microprocessor supervisor ICs has reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when supply is 10% below nominal. In other words, the reset is guaranteed to assert after the power supply falls out of regulation, but keeps inactive even when power is at the minimum specified operating voltage of the system ICs.

Negative-Going V_{DD} Transients

In addition to issuing a reset to microprocessor during power-up, power-down and brownout conditions, FP6808 is relatively immune to short-duration negative-going V_{CC} transients (glitches). Figure 11 shows typical transient duration vs. reset comparator overdrive, for which the FP6808 does not generate a reset signal. The graph was generated by using a negative-going pulse applied to V_{DD}, as shown in Figure 12, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator over-drive). The graph indicates that the maximum pulse width a negative-going V_{DD} transient can have without causing a reset signal. As the reset comparator overdrive increases, the maximum allowable pulse width decreases. A typical 0.1µF bypass capacitor mounted as close to the V_{DD} pin as possible provides additional transient immunity.

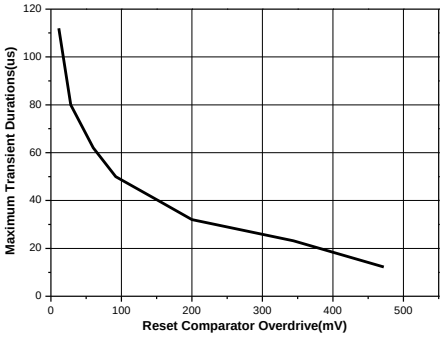


Figure 11. Maximum Transient Durations Without Causing a Reset Pulse vs. Reset Comparator Overdrive

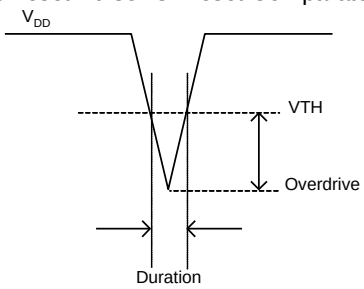


Figure 12. The V_{DD} with Negative Going Transients

Ensuring a Valid Reset Output Down to V_{DD}=0

When V_{DD} falls below 1V, the FP6808 no longer sinks current, it will become an open circuit. Therefore, high-impedance CMOS logic inputs connected to OUT can drift to undetermined voltages. This presents no problem in most applications for microprocessor's inoperative condition with V_{DD} below 1V. However, in applications where OUT must be valid down to 0V, adding a pull-down resistor to OUT causes stray leakage currents to flow to ground, providing some impedance between OUT and ground (Figure 13). R1 is recommended around 100kΩ.

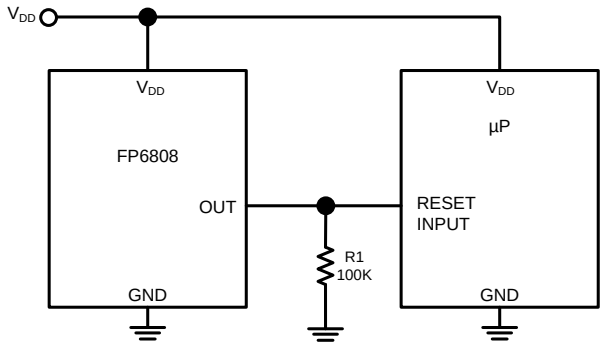


Figure 13. OUT Valid to V_{DD}=Ground Circuit

Interfacing to µPs with Bidirectional Reset Pins

Since the output of FP6808N is open drain, this device interfaces easily with microprocessor that has bidirectional reset pins. Connecting the FP6808N's output directly to the micro-controller's RESET pin with a single pull-up resistor allows either device to assert reset (Figure 14).

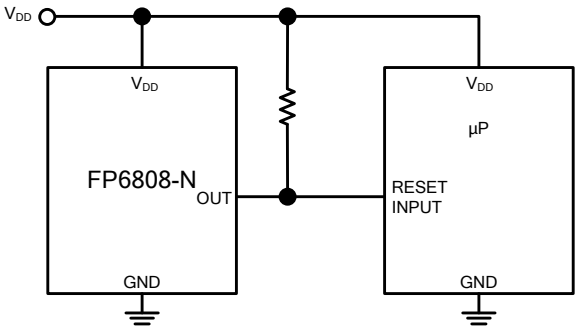
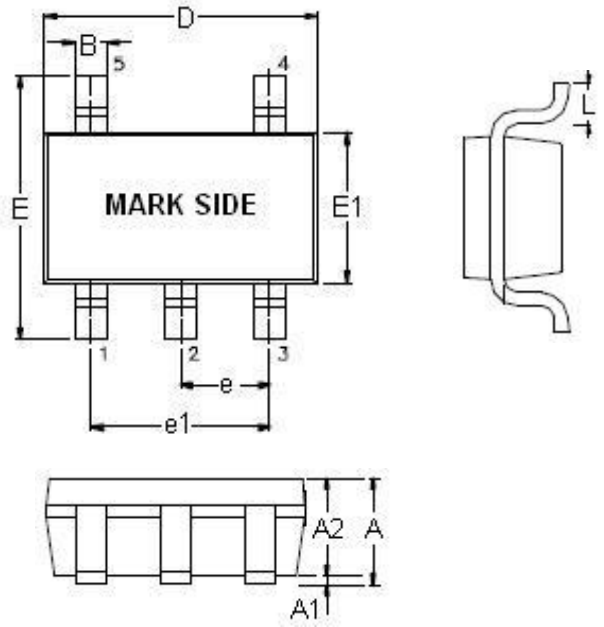


Figure 14. Interfacing to µPs with Bidirectional Reset I/O

Outline Information

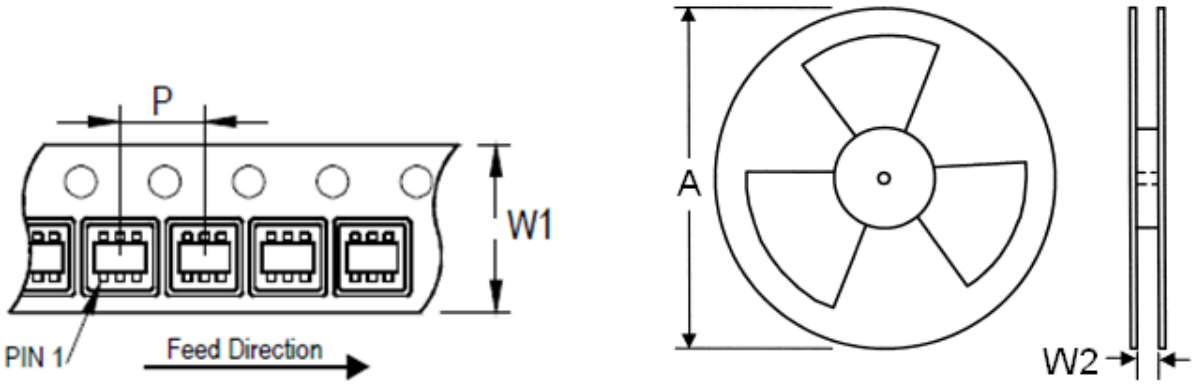
SOT-23-5 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
L	0.30	0.60

Note：Followed From JEDEC MO-178-C.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Life Support Policy
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