# 21V, 3A, 1.2MHz Synchronous Step-Down DC/DC Converter

## Description

The FR9888A is a synchronous step-down DC/DC converter that provides wide input voltage range and 3A continuous load current capability.

The FR9888A fault protection includes cycle-by-cycle current limit, UVLO, output overvoltage protection and thermal shutdown. The adjustable soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. Internal compensation function reduces external compensation components and simplifies the design process. In shutdown mode, the supply current is less than 1μA.

The FR9888A is available in a SOP-8 exposed pad package, and provides good thermal conductance.

## Features

- High Efficiency up to 91%
- Low $R_{DS}$(ON) Integrated Power MOSFET
- Internal Compensation Function
- Wide Input Voltage Range up to 21V
- Adjustable Output Voltage from 0.925V to 14.5V
- 3A Output Current
- Fixed 1.2MHz Switching Frequency
- Current Mode Operation
- Adjustable Soft-Start
- Cycle-by-Cycle Current Limit
- Over-Temperature Protection with Auto Recovery
- Output Overvoltage Protection
- Under Voltage Lockout
- <1μA Shutdown Current
- SOP-8 Exposed Pad Package

## Applications

- STB (Set-Top-Box)
- LCD Display, TV
- Distributed Power System
- Networking, XDSL Modem

## Pin Assignments

**SP Package (SOP-8 Exposed Pad)**

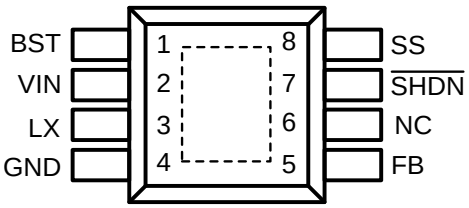
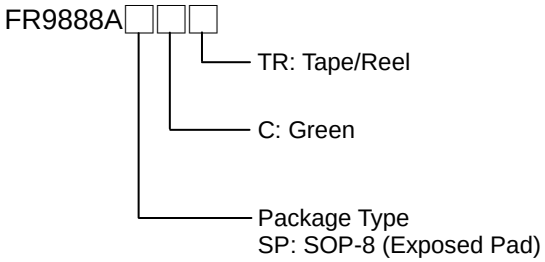



Figure 1. Pin Assignment of FR9888A

## Ordering Information



## Typical Application Circuit

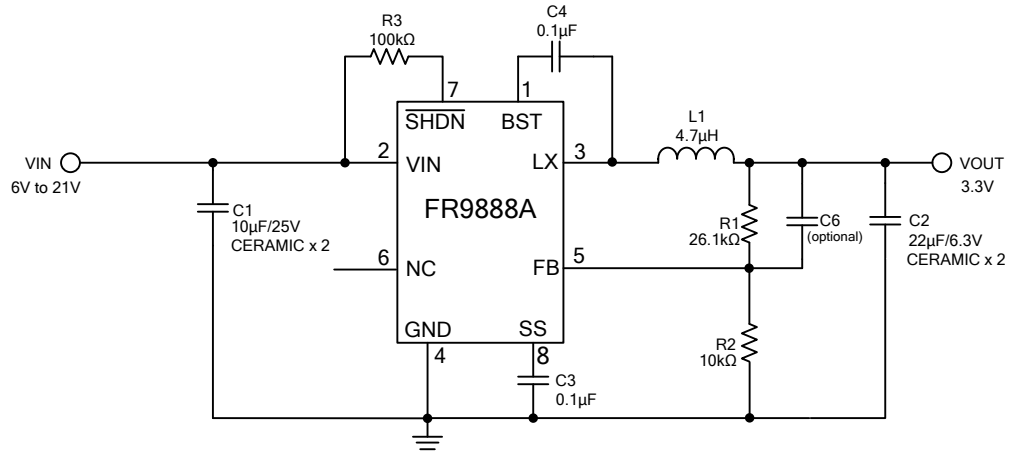



Figure 2. $C_{IN}$ /$C_{OUT}$ use Ceramic Capacitors Application Circuit

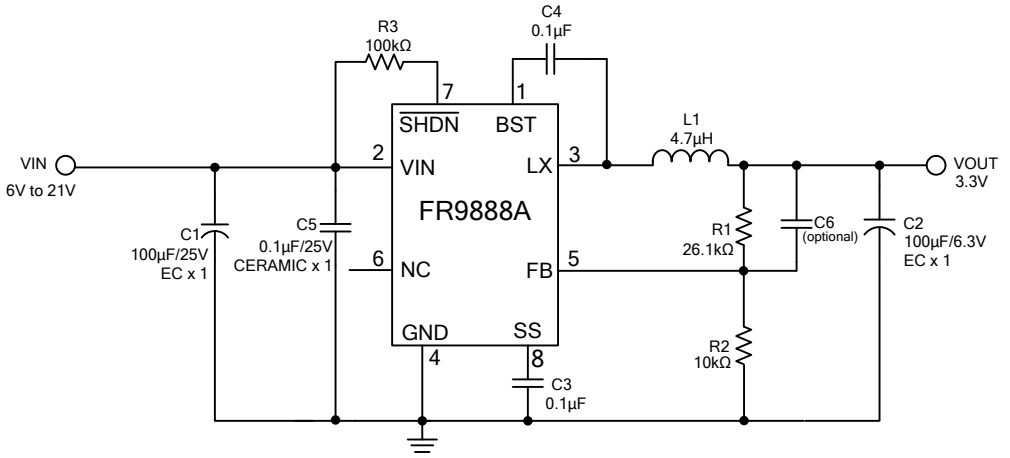



Figure 3. $C_{IN}$ /$C_{OUT}$ use Electrolytic Capacitors Application Circuit

| $V_{OUT}$ | R1 | R2 | C6 | L1 | $C_{OUT}$ |
|---|---|---|---|---|---|
| 1.2V | 3kΩ | 10kΩ | 10pF~1nF | 1.8µH | 22µF MLCC x2 |
| 1.8V | 9.53kΩ | 10kΩ | 10pF~1nF | 1.8µH | 22µF MLCC x2 |
| 2.5V | 16.9kΩ | 10kΩ | 10pF~1nF | 4.7µH | 22µF MLCC x2 |
| 3.3V | 26.1kΩ | 10kΩ | 10pF~1nF | 4.7µH | 22µF MLCC x2 |
| 5V | 44.2kΩ | 10kΩ | 10pF~1nF | 4.7µH | 22µF MLCC x2 |
| 1.2V | 3kΩ | 10kΩ | -- | 1.8µH | 100µF EC x1 |
| 1.8V | 9.53kΩ | 10kΩ | -- | 1.8µH | 100µF EC x1 |
| 2.5V | 16.9kΩ | 10kΩ | -- | 4.7µH | 100µF EC x1 |
| 3.3V | 26.1kΩ | 10kΩ | -- | 4.7µH | 100µF EC x1 |
| 5V | 44.2kΩ | 10kΩ | -- | 4.7µH | 100µF EC x1 |

Table 1. Recommended Component Values

## Functional Pin Description

| I/O | Pin Name | Pin No. | Pin Function |
|---|---|---|---|
| I | FB | 5 | Voltage Feedback Input Pin. Connect FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.925V. |
| I | VIN | 2 | Power Supply Input Pin. Drive VIN pin input voltage to power on the chip. |
| I | $\overline{\text{SHDN}}$ | 7 | Enable Input Pin. This pin is a digital control input that turns the converter on or off. Connect to VIN with a 100KΩ resistor for self-startup. |
| I | GND | 4 | Ground Pin. Connect GND to exposed pad. |
| O | LX | 3 | Power Switching Output. LX is the output of the internal high side NMOS switch. |
| O | SS | 8 | Soft-Start Pin. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft start period. |
| O | BST | 1 | High Side Gate Drive Boost Pin. A 0.1μF capacitor must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS. |
| O | NC | 6 | No connection. |

## Block Diagram

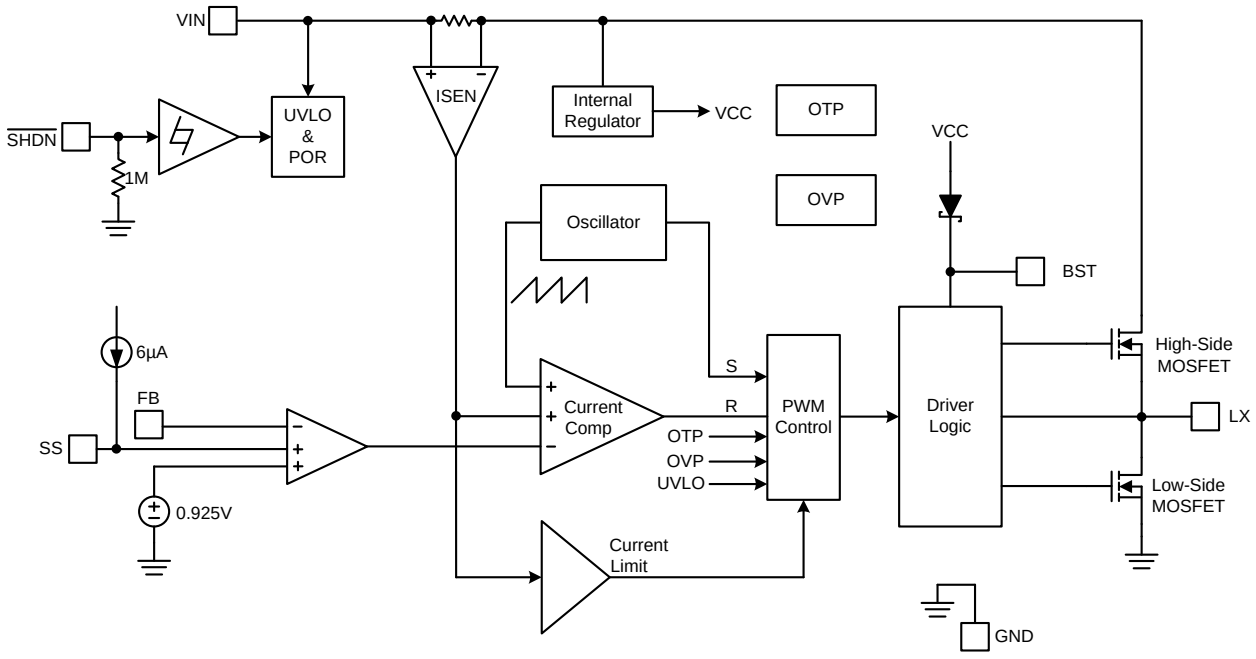



Figure 4. Block Diagram of FR9888A

## Absolute Maximum Ratings (Note1)

- Supply Voltage $V_{IN}$ ---------- -0.3V to +23V
- Enable Voltage $V_{\overline{SHDN}}$ ---------- -0.3V to +23V
- LX Voltage $V_{LX}$ (50ns) ---------- -1V to $V_{IN}$+0.3V
- BST Pin Voltage $V_{BST}$ ---------- $V_{LX}$-0.3V to $V_{LX}$+6V
- All Other Pins Voltage ---------- -0.3V to +6V
- Maximum Junction Temperature ($T_J$) ---------- +150°C
- Storage Temperature ($T_S$) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Power Dissipation @$T_A$=25°C, ($P_D$) (Note2)

  SOP-8 (Exposed Pad) ---------- 2.08W
- Package Thermal Resistance, ($\theta_{JA}$)

  SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, ($\theta_{JC}$)

  SOP-8 (Exposed Pad) ---------- 15°C/W

Note 1：Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2：PCB heat sink copper area = 10mm$^2$.

## Recommended Operating Conditions

- Supply Voltage $V_{IN}$ ---------- +6V to +21V
- Enable Voltage $V_{\overline{SHDN}}$ ---------- 0V to $V_{IN}$
- Operation Temperature Range ---------- -40°C to +85°C

## Electrical Characteristics

($V_{IN}$=12V, $T_A$=25°C, unless otherwise specified.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ Input Supply Voltage | $V_{IN}$ | | 6 | | 21 | V |
| $V_{IN}$ Quiescent Current | $I_{DDQ}$ | $V_{\overline{SHDN}}$=1.8V, $V_{FB}$=1.0V | | 3.5 | | mA |
| $V_{IN}$ Shutdown Supply Current | $I_{SD}$ | $V_{\overline{SHDN}}$=0V | | | 1 | μA |
| Feedback Voltage | $V_{FB}$ | 6V≦$V_{IN}$≦21V | 0.9 | 0.925 | 0.95 | V |
| Feedback OVP Threshold Voltage | $V_{OVP}$ | | | 1.5 | | V |
| High-Side MOSFET $R_{DS}$(ON) (Note 3) | $R_{DS(ON)}$ | | | 120 | | mΩ |
| Low-Side MOSFET $R_{DS}$(ON) (Note 3) | $R_{DS(ON)}$ | | | 100 | | mΩ |
| High-Side MOSFET Leakage Current | $I_{LX(leak)}$ | $V_{\overline{SHDN}}$=0V, $V_{LX}$=0V | | | 10 | μA |
| High-Side MOSFET Current Limit (Note 3) | $I_{LIMIT(HS)}$ | Minimum Duty | 3.5 | 4.5 | | A |
| Low-Side MOSFET Current Limit (Note 3) | $I_{LIMIT(LS)}$ | From Drain to Source | | 1.5 | | A |
| Error Amplifier Voltage Gain (Note 3) | | | | 400 | | V/V |
| Oscillation Frequency | $F_{OSC}$ | | 0.84 | 1.2 | 1.56 | MHz |
| Short Circuit Oscillation Frequency | $F_{OSC(short)}$ | $V_{FB}$=0V | | 170 | | KHz |
| Maximum Duty Cycle | $D_{MAX}$ | $V_{FB}$=0.8V | | 80 | | % |
| Minimum On Time (Note 3) | $T_{MIN}$ | | | 100 | | ns |
| Input UVLO Threshold | $V_{UVLO(Vth)}$ | $V_{IN}$ Rising | | 4.3 | | V |
| Under Voltage Lockout Threshold Hysteresis | $V_{UVLO(HYS)}$ | | | 400 | | mV |
| Soft-Start Current | $I_{SS}$ | $V_{SS}$=0V | | 6 | | μA |
| Soft-Start Period | $T_{SS}$ | $C_{SS}$=0.1μF | | 15 | | ms |
| $\overline{SHDN}$ Input Low Voltage | $V_{\overline{SHDN}}$ (L) | | | | 0.4 | V |
| $\overline{SHDN}$ Input High Voltage | $V_{\overline{SHDN}}$ (H) | | 2 | | | V |
| $\overline{SHDN}$ Input Current | $I_{\overline{SHDN}}$ | $V_{\overline{SHDN}}$=2V | | 2 | | μA |
| Thermal Shutdown Threshold (Note 3) | $T_{SD}$ | | | 170 | | °C |

Note 3：Not production tested.

## Typical Performance Curves

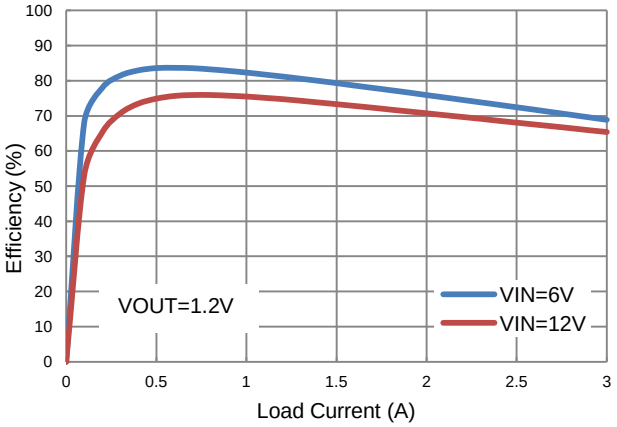



Figure 5. Efficiency vs. Loading

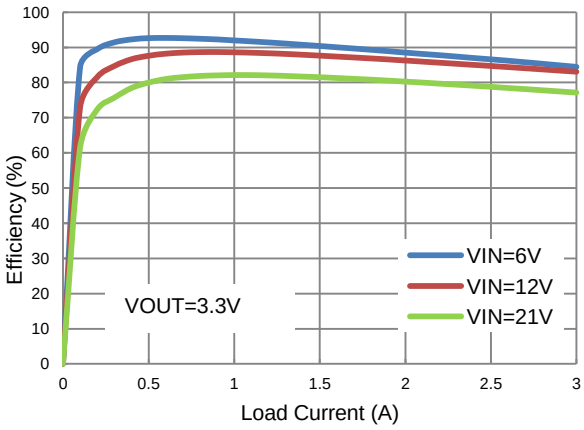



Figure 6. Efficiency vs. Loading

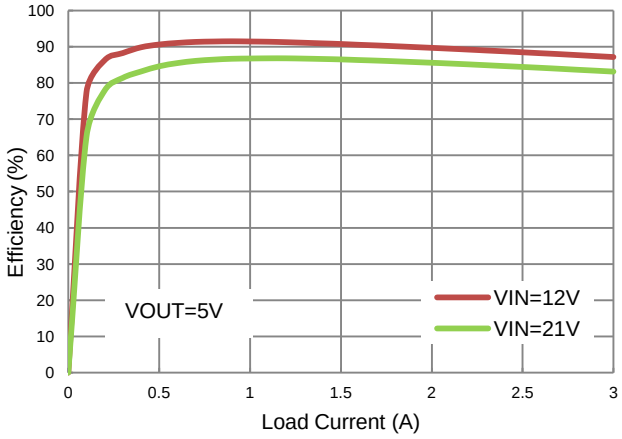



Figure 7. Efficiency vs. Loading

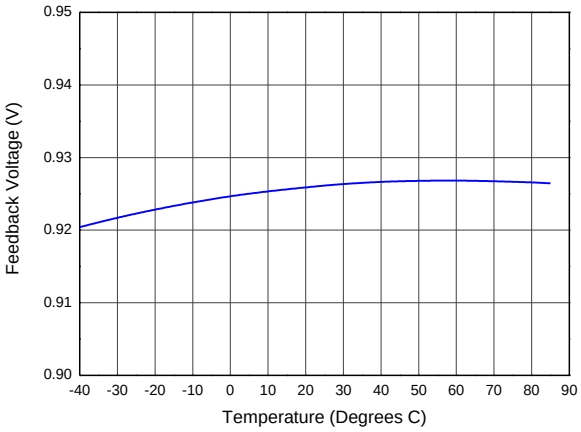



Figure 8. Feedback Voltage vs. Temperature

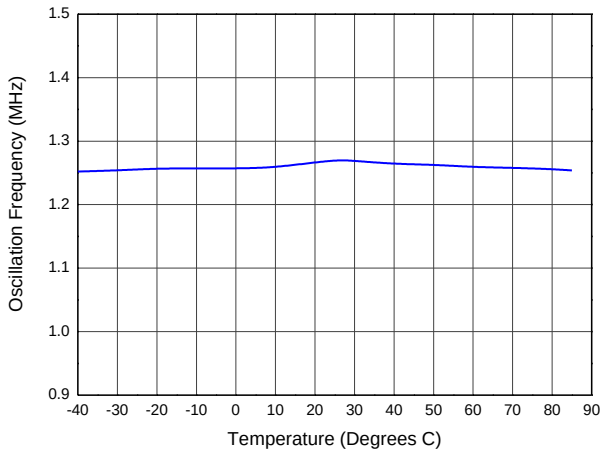
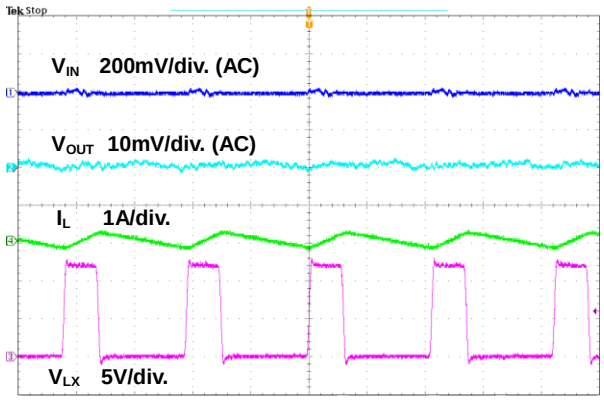



Figure 9. Oscillation Frequency vs. Temperature

## Typical Performance Curves (Continued)

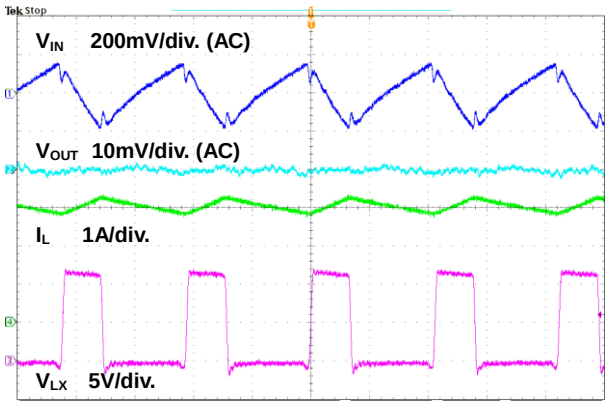
$I_{OUT}$=0A




400ns/div.

Figure 10. Steady State Waveform

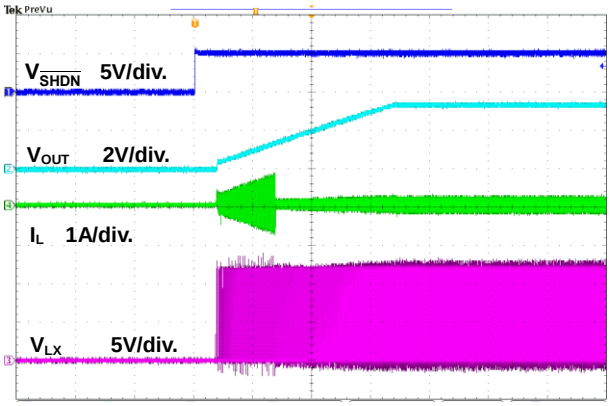
$I_{OUT}$=3A




400ns/div.

Figure 11. Steady State Waveform

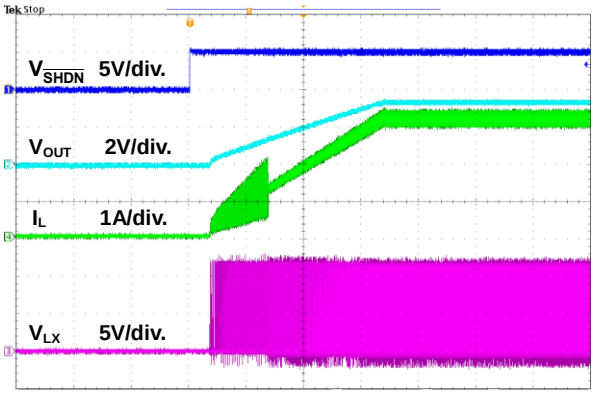
$I_{OUT}$=0A




4ms/div.

Figure 12. Startup Through $\overline{SHDN}$ Waveform

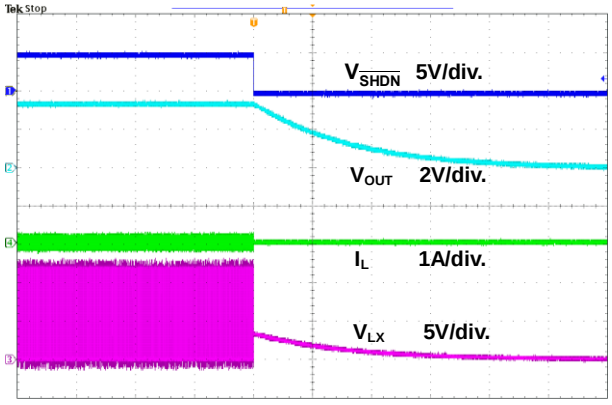
$I_{OUT}$=3A




4ms/div.

Figure 13. Startup Through $\overline{SHDN}$ Waveform

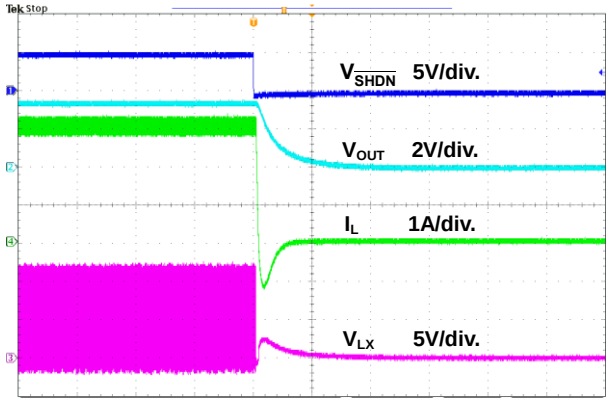
$I_{OUT}$=0A




100ms/div.

Figure 14. Shutdown Through $\overline{SHDN}$ Waveform

$I_{OUT}$=3A

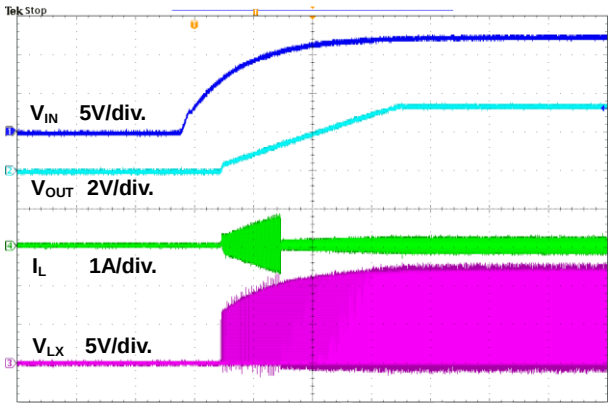



100µs/div.

Figure 15. Shutdown Through $\overline{SHDN}$ Waveform

## Typical Performance Curves (Continued)

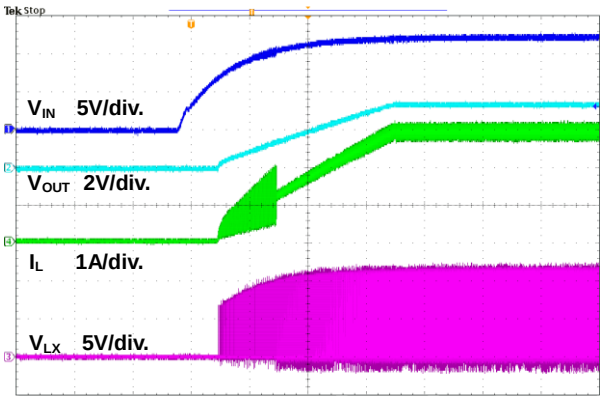
$I_{OUT}$=0A




4ms/div.

Figure 16. Startup Through VIN Waveform

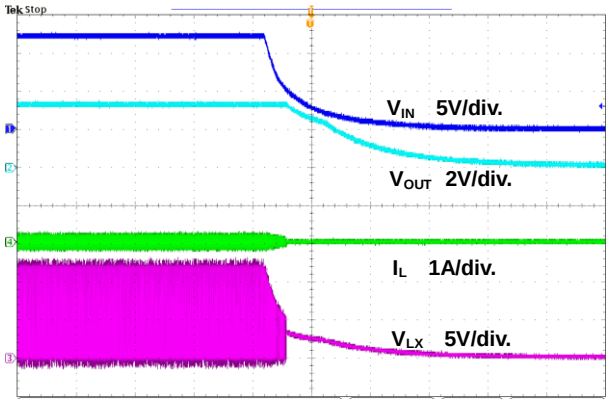
$I_{OUT}$=3A




4ms/div.

Figure 17. Startup Through VIN Waveform

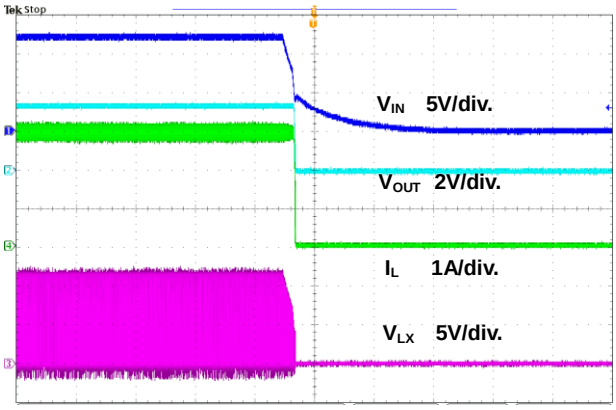
$I_{OUT}$=0A




400ms/div.

Figure 18. Shutdown Through VIN Waveform

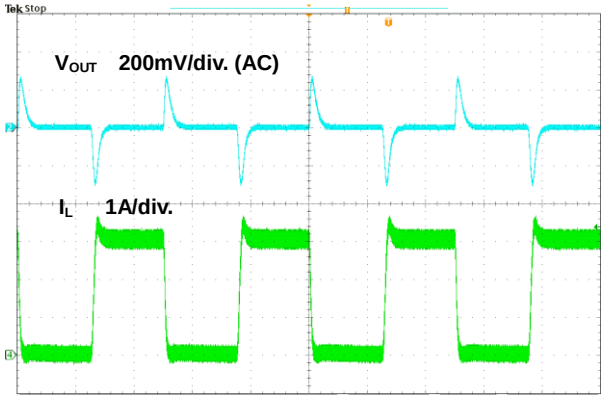
$I_{OUT}$=3A




400ms/div.

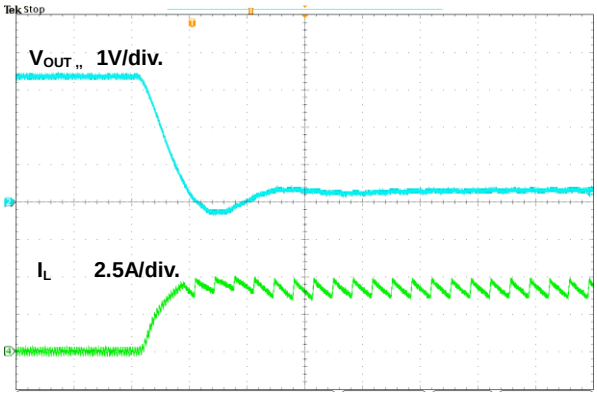
Figure 19. Shutdown Through VIN Waveform

$I_{OUT}$=0A to 3A step




400µs/div.

Figure 20. Load Transient Waveform




20µs/div.

Figure 21. Short Circuit Waveform

## Function Description

The FR9888A is a high efficiency, high frequency, internal compensation current mode synchronous step-down DC/DC converter. It supports 3A continuous output current and regulates output voltage low to 0.925V.

### Control Loop

Under normal operation, the output voltage is sensed by FB pin by a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output is compared to the switch current to control the RS latch. At the beginning of each clock cycle, the high-side NMOS turns on when the oscillator sets the RS latch, and turns off when current comparator resets the RS latch. Then the low-side NMOS will turn on until the clock period ends.

### Enable

The FR9888A $\overline{\text{SHDN}}$ pin provides digital control to turn on/off the regulator. When the voltage of $\overline{\text{SHDN}}$ exceeds the threshold voltage, the regulator will start the soft start function. If the $\overline{\text{SHDN}}$ pin voltage is below the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1μA. For auto start-up operation, connect $\overline{\text{SHDN}}$ to VIN through a 100KΩ resistor.

### Soft Start

The FR9888A employs adjustable soft start function to reduce input inrush current during start up. When the device turns on, a 6μA current will begin to charge the capacitor which is connected from SS pin to GND. The equation for the soft start time is shown as below:

$$T_{SS}(ms)=\frac{C_{SS}(nF)\times V_{FB}}{I_{SS}(\mu A)}$$

The $V_{FB}$ voltage is 0.925V and the $I_{SS}$ current is 6μA. If a 0.1μF capacitor is connected from SS pin to GND, the soft start time will be 15ms.

### Output Over Voltage Protection

When the FB pin voltage exceeds 1.5V, the output over voltage protection function will be triggered and turn off the high-side/low-side MOSFET.

### Input Under Voltage Lockout

When the FR9888A is power on, the internal circuits will be held inactive until $V_{IN}$ voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when $V_{IN}$ is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 400mV (typ).

### Short Circuit Protection

The FR9888A provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 0.4V, the oscillator frequency will be reduced to 170KHz to prevent the inductor current increasing beyond the current limit. In the meantime, the current limit will also be reduced to lower the short current. Once the short condition is removed, the frequency and current limit will return to normal.

### Over Current Protection

The FR9888A over current protection function is implemented using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

### Over Temperature Protections

The FR9888A incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 50°C (typ).

### Internal Compensation Function

The stability of the feedback circuit is controlled by internal compensation circuits. This internal compensation function is optimized for most applications and this function can reduce external R, C components.

# Application Information

### Output Voltage Setting

The output voltage $V_{OUT}$ is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.925V. Thus the output voltage is:

$$V_{OUT}=0.925V\times\left(1+\frac{R1}{R2}\right)$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

**Table 1 Recommended Resistance Values**

| $V_{OUT}$ | R1 | R2 |
|---|---|---|
| 5V | 44.2kΩ | 10kΩ |
| 3.3V | 26.1kΩ | 10kΩ |
| 2.5V | 16.9kΩ | 10kΩ |
| 1.8V | 9.53kΩ | 10kΩ |
| 1.2V | 3kΩ | 10kΩ |

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

### Input Capacitor Selection

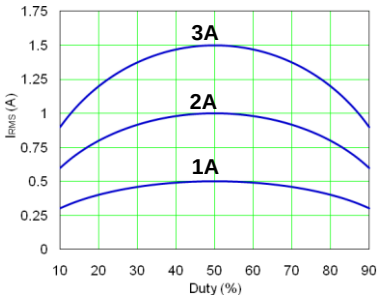
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.




A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

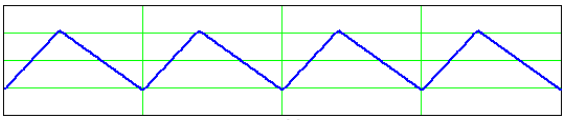
### Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)$$
$$+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

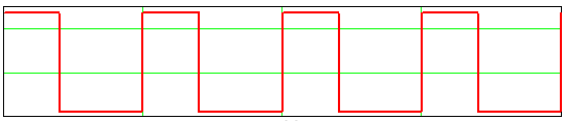
$V_{RIPPLE(ESR)}$ (t)



(t)

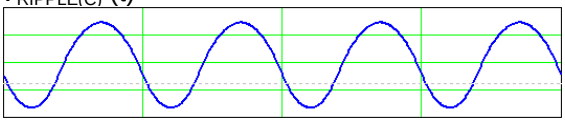
+

$V_{RIPPLE(ESL)}$ (t)



+ (t)

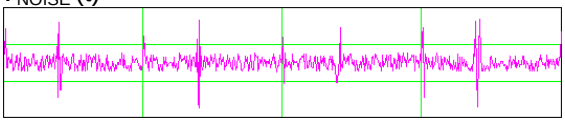
$V_{RIPPLE(C)}$ (t)



(t)

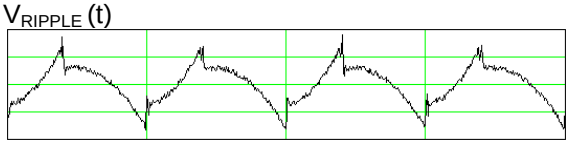
+

$V_{NOISE}$ (t)



=

$V_{RIPPLE}$ (t)



(t)

## Application Information

$$V_{RIPPLE(ESR,\ p\text{-}p)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

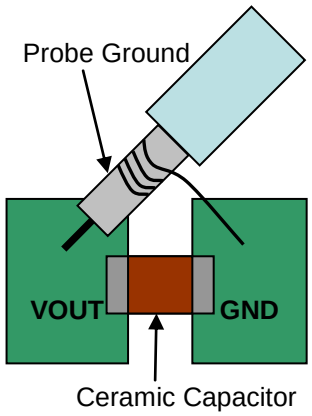
$$V_{RIPPLE(ESL,\ p\text{-}p)}=\frac{ESL}{L+ESL}\times V_{IN}$$

$$V_{RIPPLE(C,\ p\text{-}p)}=\frac{V_{OUT}}{8\times F_{OSC}^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where $F_{OSC}$ is the switching frequency, L is the inductance value, $V_{IN}$ is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the $C_{OUT}$ is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminating noise.



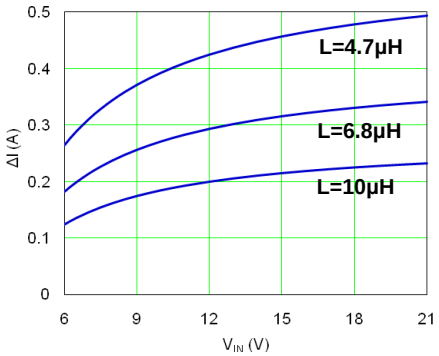

### Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The $\Delta I_L$ is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphically represent $\Delta I_L$ equation.




**$V_{OUT}$ =3.3V, $F_{OSC}$ =1.2MHz**

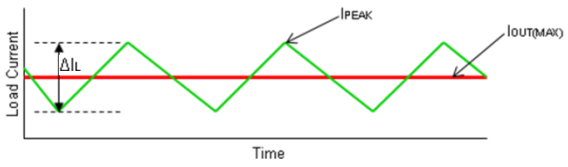
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current $\Delta I_L$ equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current $\Delta I_L$ between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FR9888A high-side MOSFET current limit. The peak inductor current is shown as below:

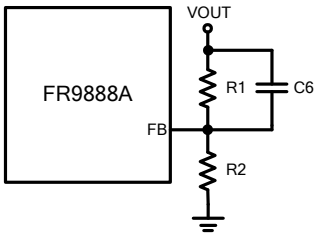
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



## Application Information

### Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C6 in the feedback network is recommended to improve the transient response or higher phase margin.




For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C6 can be calculated with the following equation:

$$C6=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where $F_{CROSS}$ is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decrease phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region. In general, the feedforward capacitor range is between 10pF to 1nF.

### PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

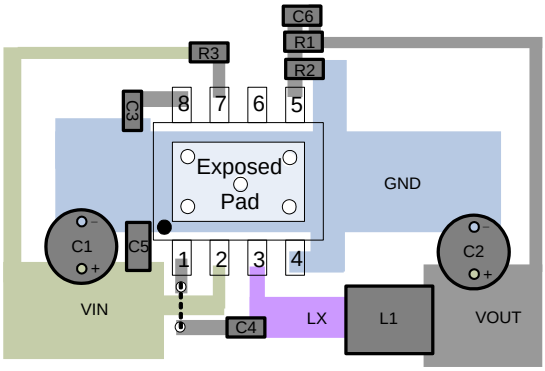
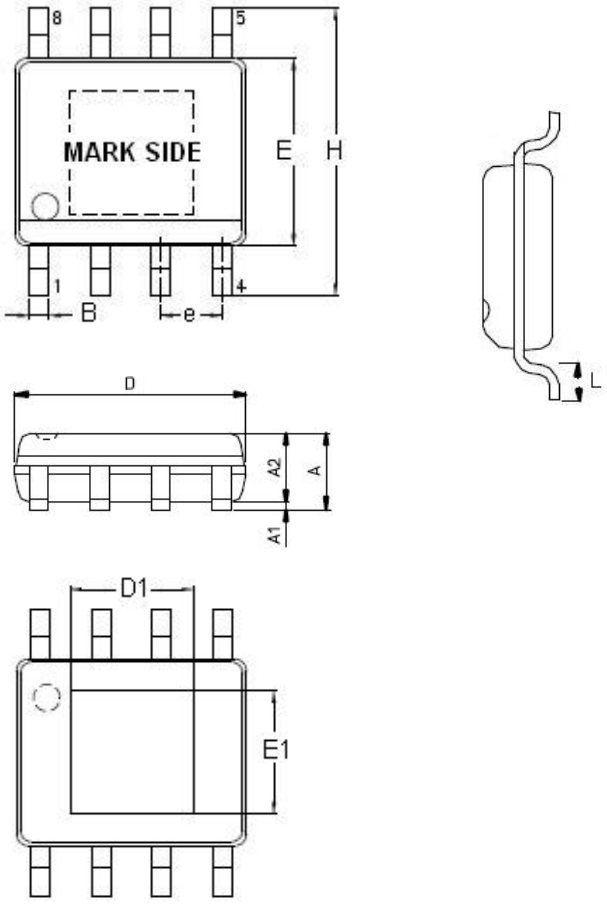



Figure 22. FR9888A Recommended PCB Layout Diagram

## Outline Information

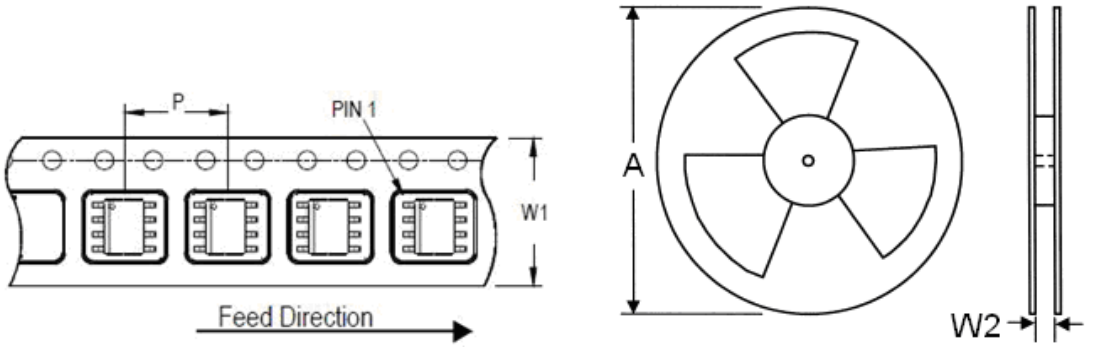
**SOP-8 (Exposed Pad) Package (Unit: mm)**




| SYMBOLS UNIT | DIMENSION IN MILLIME ER | |
|---|---|---|
| | MIN | MAX |
| A | 1.25 | 1.70 |
| A1 | 0.00 | 0.15 |
| A2 | 1.25 | 1.55 |
| B | 0.31 | 0.51 |
| D | 4.80 | 5.00 |
| D1 | 3.04 | 3.50 |
| E | 3.80 | 4.00 |
| E1 | 2.15 | 2.41 |
| e | 1.20 | 1.34 |
| H | 5.80 | 6.20 |
| L | 0.40 | 1.27 |

Note：Followed From JEDEC MO-012-E.

## Carrier Dimensions




| Tape Size (W1) mm | Pocket Pitch (P) mm | Reel Size (A) | | Reel Width (W2) mm | Empty Cavity Length mm | Units per Reel |
|---|---|---|---|---|---|---|
| | | in | mm | | | |
| 12 | 8 | 13 | 330 | 12.4 | 400~1000 | 2,500 |

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