1.product description

1.1.Features

- twenty fourNo missing codes,twenty twoBit effective precision
- analog-to-digital converter integration50Hz,60HzNotch (up to -
- 90dB) INLless than0.0015%
- Programmable gain (1~128)
- single clock cycle ready
- Programmable analog-to-digital conversion (ADC) data rate output
- The external reference voltage range can be0.1V~5V chip
- with calibration
- Integration CompatibleSPIbus interface
- Low power consumption, minimum0.6mW
- 4analog input channels
- Application
  - — Industrial Process Control
  - — weight meter
  - — Liquid/Gas Chemical Analysis
  - — blood meter
  - — Smart Converter
  - — Portable equipment
- package
  - — TSSOP16
  - — SSOP24

1.2.Product Description

CS1242It is a high-precision, low-power analog-to-digital conversion chip with a resolution of24bit, the effective resolution can reachtwenty twoIt can be widely used in the fields of process control, weighing, liquid/gas chemical analysis, blood analysis, intelligent transmitter, and portable measuring instruments.

1.3.Device overview

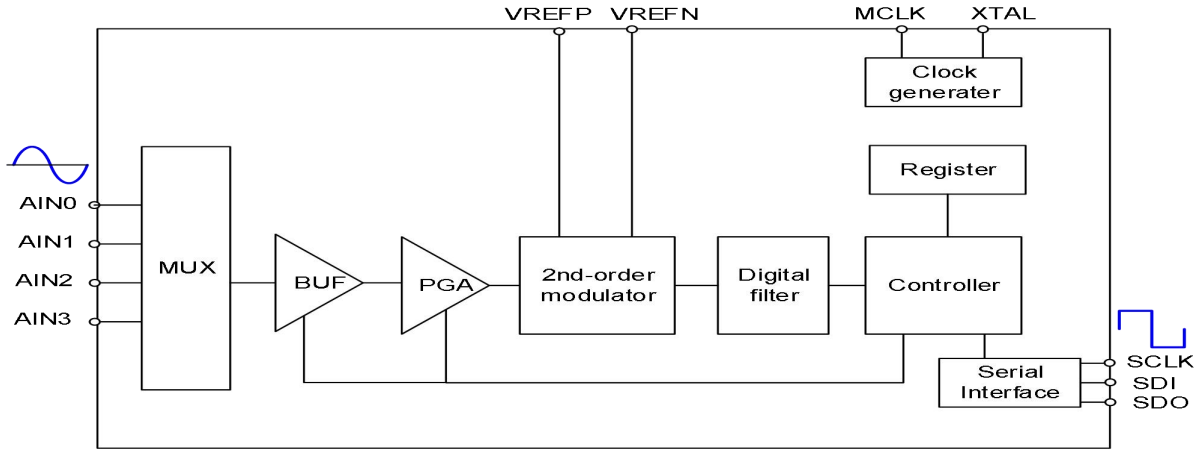
surface1Device overview

Product number	package	Package size (L×W×H)
CS1242-TSSOP16	TSSOP16	5.00mm×6.40mm×1.20mm
CS1242-SSOP24	SSOP24	9.50mm×8.20mm×2.00mm

NOTE: For the latest product, packaging, and ordering information, see page12Chapter "Ordering Information", or visit Chipsea's websitewww.chipsea.com .

1.4.Functional block diagram

picture1 CS1242



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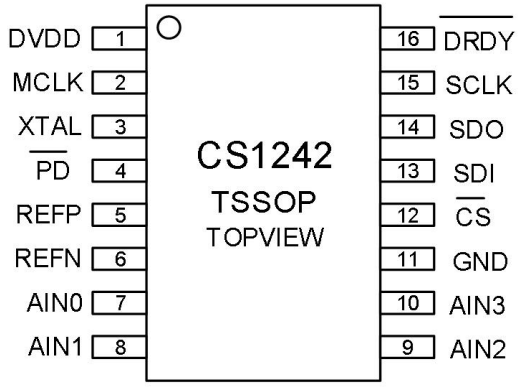
Version history

Version	Modify the content	time
V1.0	initial version	2012-12-19
V1.1	IncreaseTSSOP16package	2022-03-08

2.Pin description

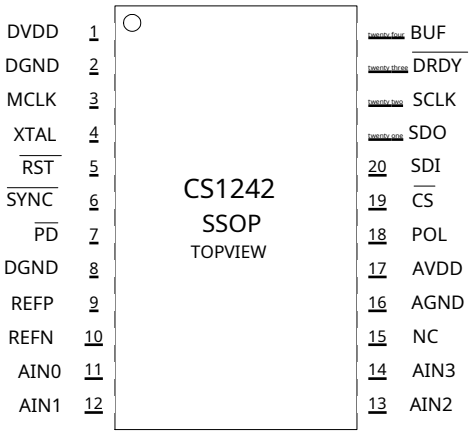
2.1. TSSOP16

picture2 CS1242_TSSOP16Chip Pin Diagram



2.2. SSOP24

picture3 CS1242_SSOP24Chip Pin Diagram



2.3.pin definition

surface2 CS1242pin definition

pin name	CS1242-TSSOP16 pin number	CS1242-SSOP twenty fourpin number	illustrate
DVDD	1	1	digital supply voltage,2.7~5.25V
DGND		2	digitally
MCLK	2	3	master clock input,1~10MHz
XTAL	3	4	Crystal drive pin2
$\overline{RST}$		5	Chip reset pin, active low
$\overline{SYNC}$		6	Synchronous control signal, active low
$\overline{PD}$	4	7	Power-down control signal, active low
DGND		8	digitally
REFP	5	9	Analog (positive) reference voltage input
REFN	6	10	Analog (negative) reference voltage input

AIN0	7	11	analog input0
AIN1	8	12	analog input1
AIN2	9	13	analog input2
AIN3	10	14	analog input3
NC		15	dead end
AGND/GND	11	16	Analogously
AVDD		17	Analog supply voltage2.7V~5.25V
POL		18	Serial Clock Polarity
$\overline{CS}$	12	19	Chip select signal, active low
SDI	13	20	Serial input data
SDO	14	twenty one	Serial output data
SCLK	15	twenty two	Serial port working clock, usingSchmitttrigger device
$\overline{DRDY}$	16	twenty three	Data ready indication signal, active low
BUF		twenty four	Analog input buffer enable signal, high with effect

3.Product function introduction

CS1242Yestwenty fourBit high precision, Low power consumptionSigma-DeltaAnalog-to-digital conversion chip, effective resolution up totwenty twobit, allowable2.7V~5.5V Operates under supply voltage conditions.

CS1242output channel, can select the input channel analog buffer (Buffer) or input the signal directly into the analog-to-digital converter (ADC), the analog buffer can effectively improve the input impedance of the chip.CS1242which provided1~128times programmable gain amplifier, the128times, CS1242Effective resolution up to18bit. The modulator is a second orderSigma-Deltamodulator, chipFIRfilter provided50Hz and60HzNotch filtering can effectively improve the anti-interference performance of the chip.

CS1242supplySPICompatible serial interface bus.

4.absolute maximum limit

surface3CS1242 Maximum limit value

name	symbol	minimum	maximum	unit	illustrate
Analog supply voltage	AVDD	- 0.3	6	V	AVDD to AGND
Digital supply voltage	DVDD	- 0.3	6	V	DVDD to DGND
pressure difference between ground	DVGND	- 0.3	0.3	V	DGND to AGND
Power instantaneous current			100	mA	Input Current momentary
Power constant current			10	mA	Input Current continuous
Digital pin input voltage		- 0.3	DVDD+0.3	V	Digital Output Voltage to DGND
Digital output pin voltage		- 0.3	DVDD+0.3	V	
Festival temperature			150	oC	Max. Junction Temperature
Operating temperature		- 40	85	oC	Operating Temperature
Storage temperature		- 60	150	oC	Storage Temperature
Chip pin soldering temperature			300	oC	Lead Temperature (Soldering, 10s)

5.digital logic characteristics

surface4CS1242 Digital Logic Features

parameter	minimum	typical	maximum	unit	Condition Description
VIH	0.8×DVDD		DVDD	V	
VIL	DGND		0.2×DVDD	V	
VOH	DVDD-0.4		DVDD+0.4	V	Ioh=1mA
VOL	DGND		DGND+0.4	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	- 10			μA	VI=DGND
fosc	1		5	MHz	
tosc	200		1000	ns	
illustrate:CS1242The digital interface isCMOSlogical interface.					

6.Electrical Characteristics

surface5CS1242 electrical characteristics when AVDD=5V

parameter		condition	minimum	Typical value	maximum value	unit
simulation enter	Analog input range	Bufferclosure	AGND-0.1		AVDD+0.1	V
		BufferOpen	AGND+0.4		AVDD-1.5	V

	Full-scale input voltage (AIN+) - (AIN-)	RAN=0			± VREF/PGA	V
		RAN=1			±VREF/(2 ×PGA)	V
	Differential input impedance	Bufferclosure		5/PGA		MΩ
		BufferOpen		5		GΩ
	bandwidth(-3dB)	fDATA = 3.75Hz		1.65		Hz
		fDATA = 7.50Hz		3.44		Hz
		fDATA = 15.0Hz		3.7		Hz
	PGA	Selectable Gain Range	1		128	
	input capacitance			9		pF
	Input leakage current	modulator off,T = 25°C		5		pA
	Test current source			2		2μA
system performance	Resolution	No missing codes		twenty four		Bits
	Integral linearity				±0.0015	% of FS
	offset error			8		ppm of FS
	offset error drift			0.02		ppm of FS/°C
	gain error			0.005		%
	Gain Error Drift			0.5		ppm/°C
	Common Mode Rejection Ratio	DC	100			dB
		fCM = 60Hz,fDATA = 15Hz		130		dB
		fCM = 50Hz,fDATA = 15Hz		120		dB
	Notch rejection ratio	fCM = 60Hz,fDATA = 15Hz		100		dB
		FCM = 50Hz,fDATA = 15Hz		100		dB
	power supply rejection ratio	DC	80	95		dB
refer to Voltage enter	VREF≡REFP - REFN	RAN = 0	0.1	2.5	2.6	V
		RAN=1	0	2.5	AVDD	V
	REFP,REFN input range	RAN = 0	0		AVDD	V
		RAN=1	0.1		AVDD	V
	Common Mode Rejection Ratio	DC		120		dB
		fVREFCM = 60Hz		120		dB
	Bias current			1.3		μA
power supply	voltage	AVDD	4.75		5.25	V
	Analog partial current	$\overline{PD}$ = 0		1		nA
		PGA = 1,Bufferclosure		120		μA
		PGA = 1,BufferOpen		160		μA
		PGA = 128,Bufferclosure		400		μA
		PGA = 128,BufferOpen		760		μA
	Digital part current (DVDD = 5V)	normal mode		2		mA
		Continuous read data mode		2.2		mA
		$\overline{PD}$ = 0		0.5		nA

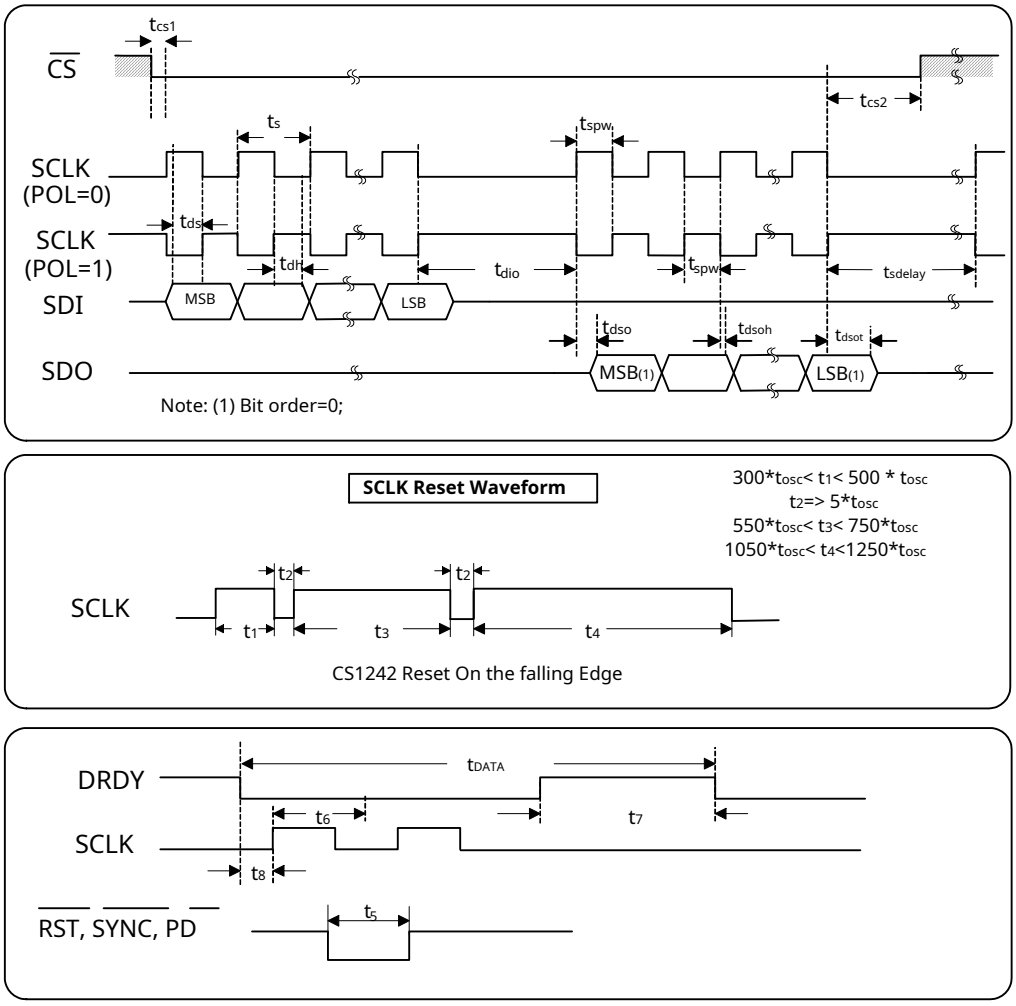
surface6CS1242 electrical characteristics when AVDD=3V

parameter		condition	minimum	Typical value	maximum value	unit
simulation enter	Analog input range	Bufferclosure	AGND-0.1		AVDD+0.1	V
		BufferOpen	AGND+0.3		AVDD-1.5	V
	Full-scale input voltage (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2× PGA)	V
	Differential input impedance	Bufferclosure		5/PGA		MΩ
		BufferOpen		5		GΩ
	bandwidth(-3dB)	fDATA= 3.75Hz		1.65		Hz
		fDATA= 7.50Hz		3.44		Hz
		fDATA= 15.0Hz		14.6		Hz
	PGA	Selectable Gain Range	1		128	
	input capacitance			9		pF
	Input leakage current	modulator off,T = 25°C		5		pA
	Test current source			2		2μA
system performance	Resolution	No missing codes		twenty four		Bits
	Integral linearity				±0.0015	% of FS
	offset error			15		ppm of FS
	offset error drift			0.04		ppm of FS/°C
	gain error			0.01		%
	Gain Error Drift			1.0		ppm/°C
	Common Mode Rejection Ratio	DC	100			dB
		fCM = 60Hz,fDATA = 15Hz		130		dB
		fCM = 50Hz,fDATA = 15Hz		120		dB
	Notch rejection ratio	fCM = 60Hz,fDATA = 15Hz		100		dB
		fSIG = 50Hz,fDATA = 15Hz		100		dB
	power supply rejection ratio	DC	75	90		dB
refer to Voltage enter	VREF≡REFP - REFN	RAN = 0	0.1	1.25	1.30	V
		RAN=1	0	2.5	2.6	V
	REFP,REFN input range	RAN = 0	0		AVDD	V
		RAN=1	0.1		AVDD	V
	Common Mode Rejection Ratio	DC		120		dB
		fVREFCM = 60Hz		120		dB
	Bias current			0.65		μA
power supply	voltage	AVDD	2.7		3.3	V
	Analog partial current	$\overline{PD}$ = 0		1		nA
		PGA = 1,Bufferclosure		107		μA
		PGA = 1,BufferOpen		118		μA
		PGA = 128,Buffer closure		360		μA

		PGA = 128,Buffer Open		500		μA
	Digital part current (DVDD = 3V)	normal mode		2		mA
		Continuous read data mode		2.2		mA
		$\overline{PD}$ = 0		0.5		nA

7.Communication timing

picture4 CS1242Timing diagram



surface7 CS1242 Timing Chart

parameter	describe	minimum	maximum value	unit
ts	SCLKclock cycle	4		tosccycle
tspw	SCLKPulse width, high level and low level	200		ns
tcs1	Chip select signalCSfalling edge with the firstSCLKedge setup time	0		ns
tds	SDIData creation time (withSCLKDelay)	50		ns
tdsh	efficientSDIdata retention time	50		ns
tdio	When issuing the following commandSDIthe last ofSCLKclock edge with SDO the firstSCLKClock edge:	50		tosccycle

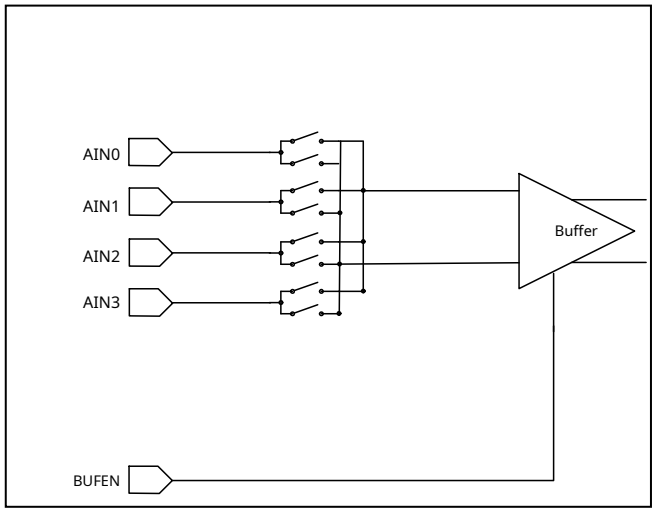
	RDATA,RDATAC,RREG,WREG				
tdso	SDOoutput data withSCLKdelay time			50	ns
tdsoh	SDOdata retention time		0		
tdsot	SDObecomes tri-stated withSCLKclock edge delay		6	10	tosccycle
tcs2	Chip select signalCShold low time with the lastSCLKclock edge		0		ns
tsdelay	the most current command last oneSCLKTime clock edge to next the first command SCLKClock edge:	RREG,WREG,SYNC,SLEEP, RDATA, RDATAC,STOPC	4		tosccycle
		GCALSELF,SELFOCA,OCALSYS, GCALSYS	8		DRDYcycle
		CALSELF	15		DRDYcycle
		RESET(or viaSCLKor RSTpin outRESETinstruction)	16		tosccycle
t5	Pulse Width		4		tosccycle
t6	Allowable analog input signal change to the next valid conversion			5000	tosccycle
t7	DORrenew,DORinvalid		4		tosccycle
t8	DRDYsignal change first after low SCLKclock	RDATACmodel	10		tosccycle
		other modes	0		tosccycle

8.Function module description

8.1.Input multiplexer (Input Multiplexer)

CS1242The input signal channels can be combined arbitrarily, and the schematic diagram of multi-input selection is shown in the figure.5shown.

picture5Block diagram of multiple input selection



CS1242Can be configured up to2for differential inputs or multiple single-ended inputs (CS1242-TSSOP16support up to4single-ended input, CS1242-SSOP24 support up to3single-ended input). For example, if you chooseAIN1It is one input terminal of the differential positive (negative) signal, and any other input terminal can be selected as the negative (positive) terminal input.

CS1242It can realize the selection and switching of the input signal and the stable output of the internal digital filter within a single clock cycle. In order to reduce the switching error, it is required toDRDYConfigured as soon as the signal goes lowMUXregister.

8.2.Input analog buffer (Buffer)

When the analog input buffer is not enabled (Buffer), the input impedance is approximately5M-/PGA. When the system requires a higher input impedance, the analog input buffer can be enabled, and the input impedance can be increased to about5G-.

The buffer enable signal can be set byBUFpin or internal registerACRcontrol. When the input pinBUFis high orACRregisterBUFWhen high, the input buffer is enabled, effectively increasing the input impedance.

If the buffer is enabled, the chip adds additional power consumption. The size of the power consumption andPGAis related to the gain, PGA=1, increase about50μAcurrent, whilePGA=128, the increased current is150μA.

When the buffer is turned on, the range of the input signal is required. At this time, the range of the input signal is required to beAGND+0.3V~ AVDD-1.5V.

8.3.Programmable Gain Amplifier (PGA)

The internal voltage gain amplifier can be programmed with a gain of1,2,4,8,16,32,64,128. by usingPGAThe effective conversion precision can be improved. E.g,PGA=1,5VFull-scale analog-to-digital conversion, the effective identification voltage is1μV,but ifPGA=128, 39mVDuring full-scale analog-to-digital conversion, the minimum can be identified75nVInput voltage.

8.4.Modulator(Modulator)

CS1242The modulator is a single loopback,2order-modulator, the sampling frequency of the modulator can be passed throughSPEED(ACRregister bit 5) control, as shown in the following table:

surface8Modulator Sampling Frequency Table

Crystal frequency (MHz)	SPEED	ADCSampling frequency (KHz)	Data output rate (Hz)			Notch frequency (Hz)
			DR=00	DR=01	DR=10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

8.5.Error correction (Calibration)

Chip calibration is divided into self-calibration and external system calibration. The calibration includes analog-to-digital converter offset error correction (OCAL), analog-to-digital converter gain correction (GCAL). While calibrating,DRDYmaintained high, indicating that nowADThe result of the conversion is not available.

After the chip is powered on again, the external ambient temperature changes, the gain (PGA) is changed to perform error correction to ensure the correct analog-to-digital conversion. After calibrationDRDYpin goes low, i.e.DRDYWhen the output is low, it means that the chip has completed the calibration. The first output data after the calibration is completed is incorrect due to the delay of the internal circuit operation and cannot be used as normal analog-to-digital conversion data. The second transform output data is normal and can be used.

8.5.1. self-calibration (Self Calibration)

CS1242self-calibration throughCALSELF,GCALSELF,OCALSELFThree instructions to control completion. implementCALSELF command, offset error correction can be done simultaneously (Offset Calibration) and gain error correction (Gain Calibration).GCALSELF The command only controls the chip to complete the gain correction, whileOCALSELFThen the control chip completes the offset correction. Gain correction, offset correction are in8 indivual TDATAcycle(ADcycle) is completed,TDATAThe period is the inverse of the output data rate. If you executeSEFLCALcommand, you need15indivualTDATA cycle.

During self-calibration,CS1242Automatically disconnect the external input signal and connect the internal voltage. When performing gain error correction,CS1242automatic firstPGAset as1, after performing gain error correctionCS1242willPGAThe value is restored to the value set by the user. However, during the execution of offset error correction,PGAsettings have not changed. (Note: If the external reference voltage is higher thanAVDD - 1.5V, the input analog buffer must be turned off.)

8.5.2. System calibration (System Calibration)

System calibration can correct the offset error and gain error inside the chip and the system. The calibration must require the correct input signal.

conduct. System calibration instructions includeOCALSYS,GCALSYS,inOCALSYSPerform offset error correction,GCALSYSPerform gain error correction, offset error correction and gain error correction respectively in8indivualTDADAcompleted within the data cycle.

During offset error correction (OCALSYS), the input must be required to be a differential voltage of0,CS1242Calculate the offset error value of the system and writeOCCregister,CS1242This is offset by internal calculations during normal conversions.

While performing gain error correction (SYSGCAL), a positive full-scale voltage must be input,CS1242Calculate the gain error of the system and writeGCCregister,CS1242This is offset by internal calculations during normal conversions.

8.6.External reference voltage (External Voltage Reference)

CS1242An external reference voltage is required, and the specific value is passed throughACRregister configuration. The reference voltage is connected toREFPandREFNOn the pins, the voltage cannot exceed the power supply voltage of the chip. The specific voltage values are as follows:

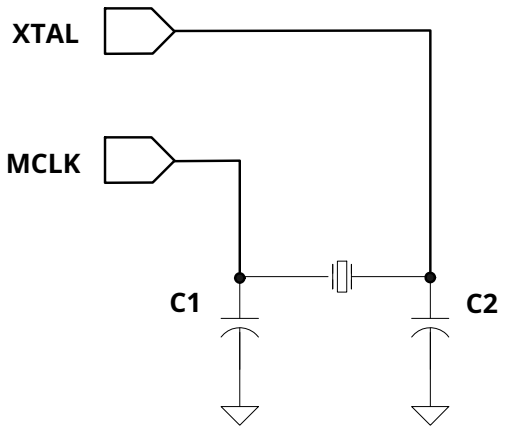
surface9external reference voltage andRANrelation table

RAN(ACR.2)	voltage(V)	Reference differential voltage (V)	Remark
0	5	<=2.5	
1	5	<=5	
0	3.0	<=1.25	
1	3.0	<=2.5	

8.7.clock unit (Clock Unit)

CS1242An external crystal, oscillator or clock can be connected. If connected to an external clock, thenMCLKpin input, this timeXTALdangling. If an external crystal is connected, the circuit requirements are as follows: (required inMCLKandXTALconnected to the pins at the same time10~20pFcapacitor)

picture6External crystal oscillator connection diagram



8.8.digital filter (FIR)

CS1242with a programmableFIRfilter.FIRFilters can be configured for different output rates. when using2.4576M the clock,CS1242The rate of output data can be configured as15Hz,7.5Hzor3.75Hz. at this time,FIRThe filter can simultaneously 50Hzand60HzThe clutter signal is notch filtered.

If other output data rates are desired, other clock frequencies must be used. At this time, the notch frequency is also changed at the same time. For example, when using the default register configuration, the clock frequency is3.6864Mwhen:

The output data frequency is:

(3.6864MHz/2.4576MHz)×15Hz = 22.5Hz The notch

frequency is:

(3.6864MHz/2.4576MHz)×(50Hzand60Hz)= (75Hzand90Hz)

8.9.Serial bus interface (SPI)

CS1242passSPIThe bus communicates with external controllers.CS1242Can only be used in slave mode. The bus interface is a standard quad

WireSPIbus, includingCS,SCLK,SDIandSDOplus a control clock polarityPOL. The bus supports bipolar clocks, the polarity of which is determined byPOLto control.

8.9.1. Chip select signal (CS)

in withCS1242Before communication, the external controller must sendCSChip select signal. During the entire communication period,CSThe signal must be held low. whenCSAfter the signal goes high, the entireSPIThe bus will be reset.CSThe signal can also be tied normally low. whenCSsignal is pulled normally low,SPIThe bus can work in three-wire mode.

8.9.2. serial clock (SCLK)

SCLKis a Schmitt trigger, used toSDIandSDOThe signal is sampled. To prevent wrong sampling data,SCLKMust be very clean. if in3indivualDRDYno periodSCLKthe clock appears, then in the nextSCLKwhen it comes,SPIThe bus will be reset and the next communication cycle will begin.SCLKA specific waveform on can reset the entire chip.

8.9.3. Clock Polarity Control (POL)

POLcontrolled serial clockSCLKpolarity. whenPOLis low, the data is inSCLKThe falling edge of is sampled. If there is no clock pulse, thenSCLKshould be kept low. whenPOLWhen high, the data is inSCLKThe rising edge of is sampled, if there is no clock pulse, SCLKshould remain high.

8.9.4. data input(SDI)and data output (SDO)

SDIandSDOThe pins are used to input and output data, respectively. When not in use,SDOis high impedance, which allows theSDI and SDOconnected together and drive it through a bidirectional bus. It should be noted that in this case it is not suitable toCS1242issueRDATAC instruction. becauseRDATACcommand needs to useSTOPCinstruction orRESETcommand to terminate. while inRDATACIn mode, this two-way bus will always be occupied to send data to the outside, so it is not possible to send data to the outside through the bus at this time.CS1242 sendSTOPC instruction orRESETinstruction, so it cannot be terminatedRDATACstatus, except at this timeSDOThe data sent containsSTOPCor RESETinstruction. at this timeSDIwill detectSTOPCorRESETinstruction, which terminatesRDATACstate.

8.9.5. data ready (DRDY)

DRDYSignals are used to indicate the state of the internal data registers. When the internal data registerDORWhen the new data is ready, DRDYThe signal will go low. When executing a slave internal data registerDORAfter a read operation to read data,DRDYThe signal will go high. existDORWhen register data is ready to be updatedDRDYThe signal will also go high, indicating that at this timeDORThe data in the register is not available, preventing theDORregisters are updated fromDORRead data in the register.

DRDYThe signal can also be obtained fromACRregisterbit 7to obtain.

8.10.data synchronization(SYNC)

CS1242able to passSYNCpin orSYNCcommand to synchronize data. when usingSYNCpin for data synchronization, the digital circuitry willSYNCreset on the falling edge. whenSYNCAfter going low, the serial interface is in an inactive state. whenSYNCAfter going high, the digital circuit will change fromRESETout of state, the data will be synchronized on the subsequent rising edge of the system clock.

when usingSYNCWhen the instruction performs data synchronization, the digital filter isSYNClast commandSCLKedge of the clock is reset, the modulator will be inRESETstate until the nextSCLKThe clock edge is detected. existSYNCthe first afterSCLK Within the rising edge of the system clock, the data will be synchronized.

8.11.Power-on reset and chip reset

There are three ways toCS1242To reset: pull the pin low, sendRESETinstruction, inSCLKsend a specific waveform on (SCLK RESETwaveform, refer to p.7Chapter "Communication Timing").

9.register description

CS1242The working mode is configured through a series of control registers, which include data format, multiplexing signal input, analog-to-digital conversion data output rate, correction control, etc.

9.1.register list

surface10Detailed List of Internal Registers

address(h)	register	the first7bit	the first6bit	the first5bit	the first4bit	the first3bit	the first2bit	the first1bit	the first0bit
00	SETUP	ID3	ID2	ID1	ID0	reserve	PGA2	PGA1	PGA0
01	MUX	PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0
02	ACR	$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUF	BITOR	RAN	DR1	DR0
03	ODAC	reserve	CHSEL	ISET1	ISET0	reserve	reserve	reserve	reserve
04	reserve								
05	reserve								
06	reserve								
07	OCC0	OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
08	OCC1	OCC17	OCC16	OCC15	OCC14	OCC13	OCC12	OCC11	OCC10
09	OCC2	OCC27	OCC26	OCC25	OCC24	OCC23	OCC22	OCC21	OCC20
0A	GCC0	GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
0B	GCC1	GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
0C	GCC2	GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
0D	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0E	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0F	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

9.2.Register Details

SETUPregister(address=00H, reset value =xxxx0000)PGAcontrol(SETUP REGISTER)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	reserve	PGA2	PGA1	PGA0

SETUP. 7-4 ： chipIDnumber, for manufacturer use

SETUP.3 ： reserve

SETU.2-0 ： PGA2/PGA1/PGA0, programmable gain amplifier gain selection (Programmable Gain Amplifier Gain Selection)

000=1(Defaults)
001=2
010=4
011=8
100=16
101=32
110=64
111=128

MUXregister(address=01H, reset value =01H) input channel selection (Multiplexer Control Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0

MUX.7-4 ： PS3~0, positive input channel selection (Positive Channel Selection)

0000=ADIN0(Defaults)
0001=ADIN1
0010=ADIN2
0011=ADIN3
rest = reserved (Reserved)

MUX.3-0 ： NS3~0, negative input channel selection (Negative Channel Selection)

0000=ADIN0
0001=ADIN1(Defaults)
0010=ADIN2
0011=ADIN3
rest = reserved (Reserved)

ACRregister(address=02H,reset value =00H) analog circuit control (Analog Control Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUF	BITOR	RAN	DR1	DR0

ACR.7 : $\overline{DRDY}$, the data is ready (Data Ready, read only), with output pins$\overline{DRDY}$same value

ACR.6 : U/$\overline{B}$,Data Format(Data Format)

0= bipolar (default)

+FSRoutput0x7FFFFFH,ZERO=0x00000H, -FSR=0x800000H 1= Unipolar

+FSRoutput0xFFFFFFH,ZERO=0x00000H, -FSR=0x000000H

ACR.5 : SPEED, the analog-to-digital converter sampling frequency control (Modulator Clock Speed)

0=fosc/128(Defaults) 1 =fosc/256

ACR.4 : BUF, the input buffer is enabled (Buffer Enable)

0=disabled (default)

1= enable

ACR.3 : BITOR,Output Databitorder

0 =Big order first (default)

1 =low first

ACR.2 : RAN, conversion range selection (Select)

0= full scale input (Full Scale) is +/-V_{REF}(Defaults) 1= full scale input (Full Scale) is +/-V_{REF}/2

ACR.1-0 : DR1/DR0, the data output rate (Data Rate)

00=15Hz(Defaults)

01=7.5Hz

10=3.75Hz

11=reserve(Reserved)

ODACregister(address=03H,reset value =00H)Offset DACset up

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
invalid	CHSEL	ISET1	ISET0	invalid	invalid	invalid	invalid

ISET1-0 : Analog circuit bias current selection,

00= Bias current is10μA(Defaults) 01or10= Bias current increases25% 11= Bias current increases50%

When using higher clock frequencies, increasing the analog circuit bias current can help improveCS1242performance. Chopping -

CHSEL : modulation mode selection.

0= Chopping frequency is the sampling frequency of the modulator1/2,PGA=1~128available (default) 1= the chopping frequency is equal to the modulator sampling frequency,PGA=2~128when available in general CHSELSet as0That's enough, but in some cases (related to the peripheral application circuit) some high-frequency noise may be coupled to the low-frequency band, you can set theCHSELfor1, note that this will lead to some increase in offset voltage and noise.

OCC0register(address=07H,reset value =00H), the offset error coefficient (Offset Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23YesMSB,OCC00 YesLSB) to correct the offset error.							

OCC1register(address=08H,reset value =00H) offset error positive coefficient (Offset Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23YesMSB,OCC00 YesLSB) to correct the offset error.							

OCC2register(address=09H,reset value =00H) offset error correction factor (Offset Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23YesMSB,OCC00 YesLSB) to correct the offset error.							

GCC0register(address=0AH,reset value =59H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23YesMSB, GCC00 YesLSB) to correct the gain error.							

GCC1register(address=0BH,reset value =55H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23YesMSB, GCC00 YesLSB) to correct the gain error.							

GCC2register(address=0CH,reset value =55H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23YesMSB, GCC00 YesLSB) to correct the gain error.							

DOR2register(address=0DH, reset value =00H) analog-to-digital data (Data Output Register)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR 23	DOR22	DOR 21	DOR 20	DOR 19	DOR 18	DOR 17	DOR 16
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB,DOR00 YesLSB).							

DOR1register(address=0EHreset value =00H) analog-to-digital data (Data Output Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB,DOR00 YesLSB).							

DOR0register(address=0FH,reset value =00H) analog-to-digital data (Data Output Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB,DOR00 YesLSB).							

10.Instruction description

CS1242A series of instructions are used, and the instructions complete the working mode control, working speed control, error correction and so on of the chip. Some of these instructions are single (such asRESET), some require additional operands (such asWREGWait).

Operands:

n =quantity(0arrive127) r =

register (0arrive15) x =any

value

10.1. command list

surface11 CS1242Instruction description table

instruction	describe	opcode	operand
RDATA	fromDORread data from register	0000 0001 (01H)	- -
RDATAC	fromDORContinuously read data from registers	0000 0011 (03H)	- -
STOPC	stop fromDORContinuously read data from registers	0000 1111 (0FH)	- -
RREG	read register"rrrr"the value of	0001 rrrr (1XH)	xxxx_nnnn
WREG	write data to the register"rrrr"middle	0101 rrrr (5XH)	xxxx_nnnn
CALSELF	Corrects for chip offset and gain errors	1111 0000 (F0H)	
OCALSELF	Correct the offset error of the chip	1111 0001 (F1H)	
GCALSELF	Correct the gain error of the chip	1111 0010 (F2H)	
OCALSYS	Correct the offset error of the system	1111 0011 (F3H)	
GCALSYS	Correct the gain error of the system	1111 0100 (F4H)	
SYNC	rightDRDYto synchronize	1111 1100 (FCH)	
SLEEP	Put the chip into sleep mode	1111 1101 (FDH)	
RESET	Reset the chip to the state after power up	1111 1110 (FEH)	
Note: When receiving data, the high order is always first, and the format of sending data is determined byACRregisterBITORDERbit to decide.			

10.2. Instruction details

RDATA- read data

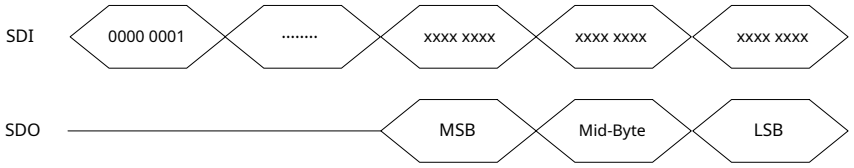
describe: fromDORThe latest read from the registerADThe converted value, this value is24bit. none

Operands:

byte: 1

coding: 0000 0001

Data transfer sequence:



RDATAC- Continuous read data command

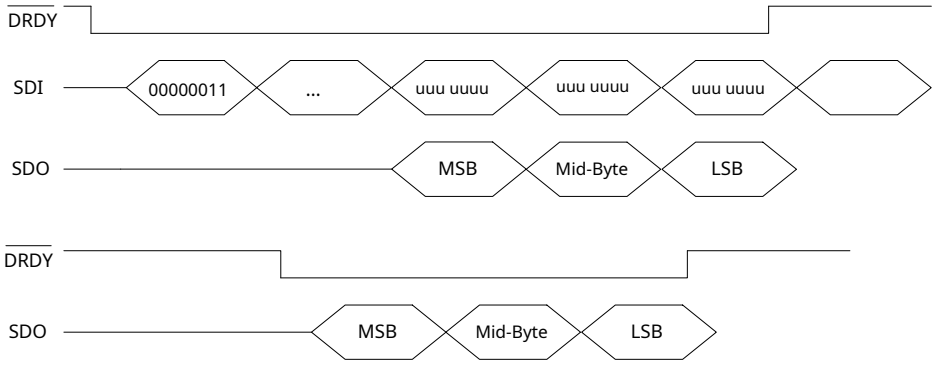
describe:RDATACallowed in eachDRDYContinuously from the signal periodDORThe register is read every timeADthe result of the conversion. This command does not need to be executed every timeDRDYSent when the signal goes lowRDATAinstruction. can be sent bySTOPCinstruction orRESET instruction to terminate the execution of this instruction. existDRDYAfter the signal goes low, wait at least until10indivualfOSCcycle to execute this instruction.

Operands: none

Character Festival: 1

edit code: 0000 0011

Data transfer sequence:



STOPC- Stop continuous read data command

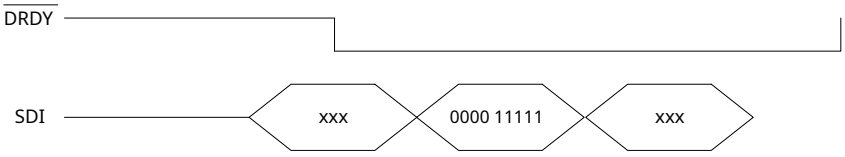
Description: Stop continuous read data mode. need inDRDYEmitted when the signal goes low.

Operands: none

Character Festival: 1

edit code: 0000 1111

Data transfer sequence:



RREG- read the value of the register

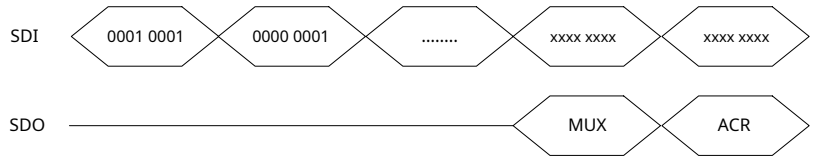
Description: output the most16value of a register. The address of the first register is determined by the first operand of the instruction. The number of registers read is added by the value of the second operand of the instruction1Decide. If this value exceeds the number of remaining registers, the address of the register goes to the first register.

Operands: r,n

Character Festival: 2

edit code: 0001 rrrr xxxx nnnn

Data transfer sequence: read the values of two registers, the address of the first register is01H (MUX)



WREG- write data to the register

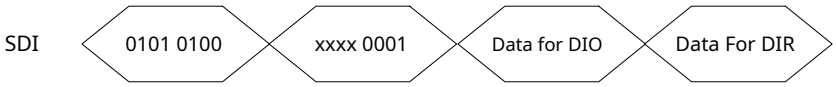
Description: Writes data to multiple registers. The address of the first register is determined by the first operand of the instruction. The number of registers read is added by the value of the second operand of the instruction1Decide.

Operands:r, n

byte: 2

coding: 0101 rrrr xxxx nnnn

Data transfer sequence: write data into two registers, the address of the first register is04H (DIO)



CALSELF- Self-correction of offset error and gain error

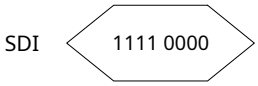
describe: Self-correct the chip. After doing this,OCCregister andGCCThe value of the register will be updated.

Operands: none

Character Festival: 1

edit code: 1111 0000

Data transfer sequence:



OCALSELF- Self-correction of offset errors

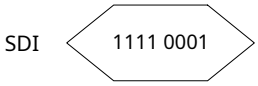
describe: Offset error self-correction for the chip. After doing this,OCCThe value of the register will be updated.

Operands: none

Character Festival: 1

edit code: 1111 0001

Data transfer sequence:



GCALSELF- Self-correction of gain error

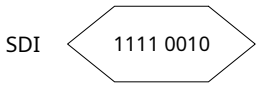
describe: Gain error self-correction for the chip. After doing this,GCCThe value of the register will be updated.

Operands: none

Character Festival: 1

edit code: 1111 0010

Data transfer sequence:



OCALSYS- Correct the offset error of the system

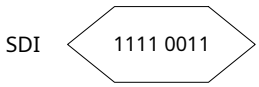
Description: Corrects the offset error of the system. At this time, the input signal of the system should be0,CS1242CalculateOCC The value of , compensates for the offset error. After doing this,OCCThe value of the register will be updated. The user must enter the correct analog input0SignalOCCThe registers are automatically updated.

Operands: None

Character Festival: 1

edit code: 1111 0011

Data transfer sequence:



GCALSYS- Correct the gain error of the system

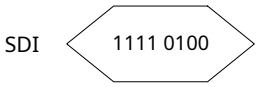
Description: Correct the gain error of the system. At this time, the input signal of the system should be full-scale voltage,CS1242Calculate GCCThe value of , compensates for the gain error. After doing this,OCCThe value of the register will be updated. The user must input the full scale signal on the correct analog input.GCCThe registers are automatically updated.

Operands: none

Character Festival: 1

edit code: 1111 0100

Data transfer sequence:



SYNC-rightDRDYsignal to synchronize

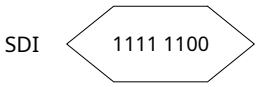
describe: SynchronizeCS1242The data

Operands: none

Character Festival: 1

edit code: 1111 1100

Data transfer sequence:



SLEEP- Put the chip into sleep mode

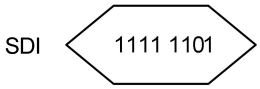
describe: MakeCS1242Enter sleep mode. To wake up from sleep mode, useWAKEUPinstruction

Operands: none

Character Festival: 1

edit code: 1111 1101

Data transfer sequence:



RESET- Reset the chip to the default state

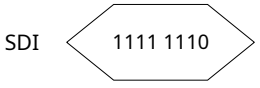
describe: Resets all register values to their state after power-up. This command can terminateRDATACinstruction

Operands: none

Character Festival: 1

edit code: 1111 1110

Data transfer sequence:

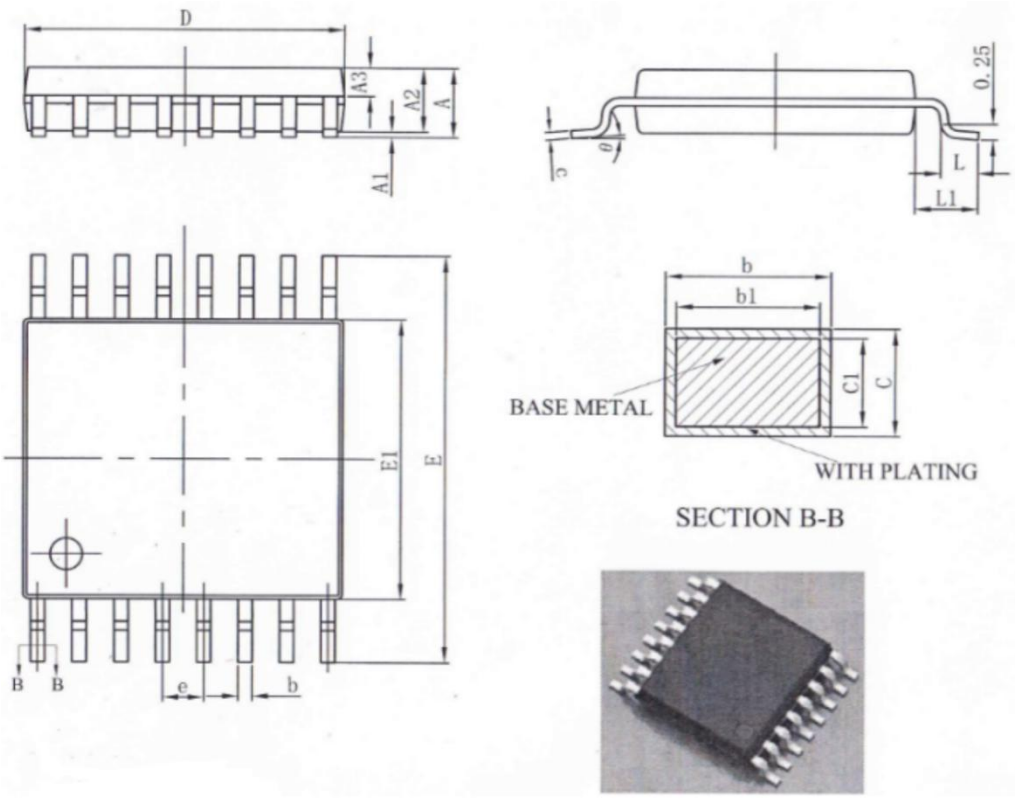


11.Package information

CS1242useTSSOP16,SSOP24package.

11.1. TSSOP16

Figure 7 TSSOP16 package outline



surface12 TSSOP16Package Size Information

SYMBOLS	MIN	NOR	MAX
	mm		
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
B	0.330	0.406	0.508
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	- .14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ°	0°	-	8°

11.2. SSOP24

Figure 8 SSOP24 package outline

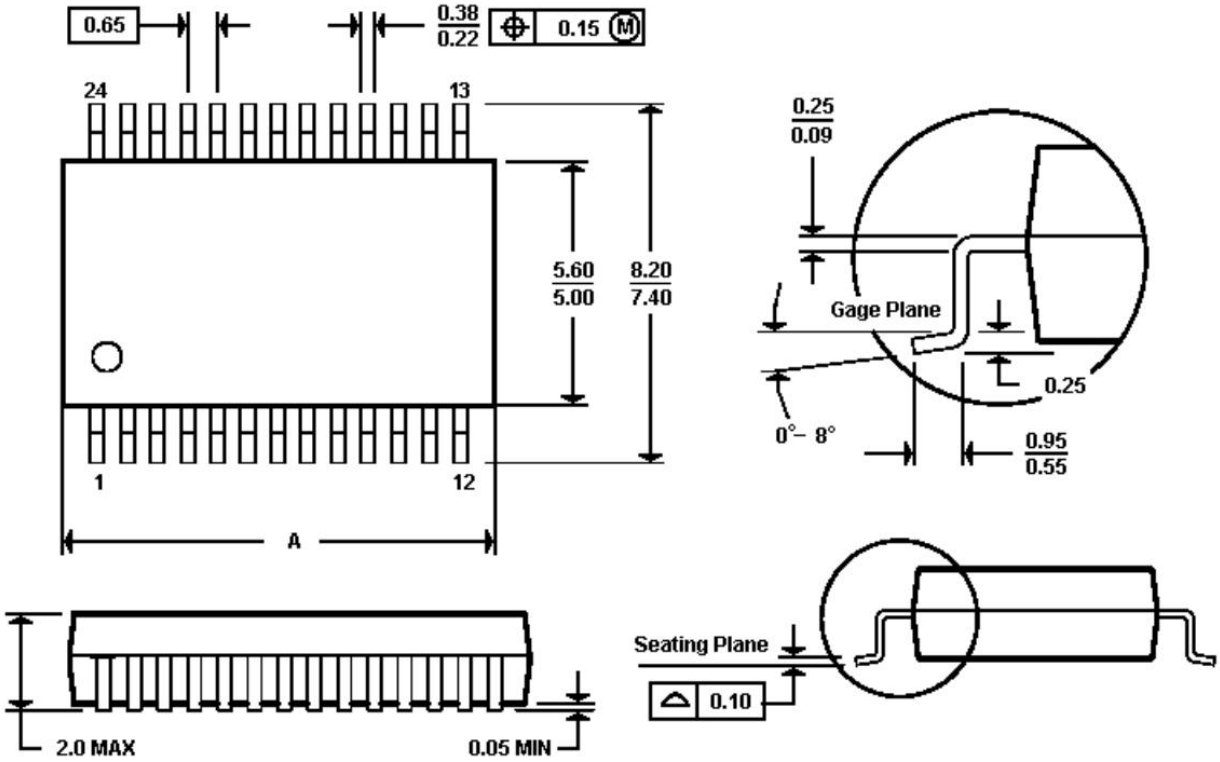


Table 13 SSOP24 package size information

SYMBOLS	MIN	NOR	MAX
	mm		
A	7.90	0.35	9.50

12.Order information

Table 14 Ordering Information

Product number	pin	package type	Package	Packaging Quantity	Operating temperature (°C)	MSL	silk screen
CS1242-TSSOP16	16	TSSOP	Tube	5000 (50pcs/Tube,100tube/box)	- 40 ~85	3	CS1242-TS
CS1242-SSOP24	twenty four	SSOP	Tube	5000 (50pcs/Tube,100tube/box)	- 40 ~85	3	CS1242

Note: There is currently no fixed code to distinguish different packaging methods for the same chip package. Customers need to note the packaging method when placing an order.

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CHIPSEA

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