芯海科技
CHIPSEA

CS1232User Manual

24-bit Sigma-Delta ADC

Rev 1.5

Mailing address: 9th Floor, Block A, Garden City Digital Building, No. 1079 Nanhai Avenue, Shekou, Nanshan District, Shenzhen

Postal Code: 518067

Company Tel: +(86 755)86169257

Fax: +(86 755)86169057

Company website: www.chipsea.com

WeChat ID: Chipsea Technology

Wechat QR code:

Version history

historic version	Modify the content	version date
REV 1.0	initial version	2011-08-25
REV 1.1	Changed clock description, added temperature sensor description	2011-09-20
REV 1.2	Change package data	2011-11-30
REV 1.3	Change the electrical characteristics table	2012-05-20
REV 1.4	modify readADTiming of Values: Section25indivualSCLKWillDRDYPull up	2012-07-09
REV 1.5	replace with newlogo,Republish	2014-10-17

Table of contents

Figure Catalog

table directory

1Chip function description

CS1232It is a high-precision, low-power analog-to-digital conversion chip. Its resolution is24bit, the effective resolution can reach20.8bit. Can Widely used in process control, gravimetric, liquid/gas chemical analysis, blood analysis, smart transmitters, portable measuring instruments field

1.1The main functional characteristics of the chip

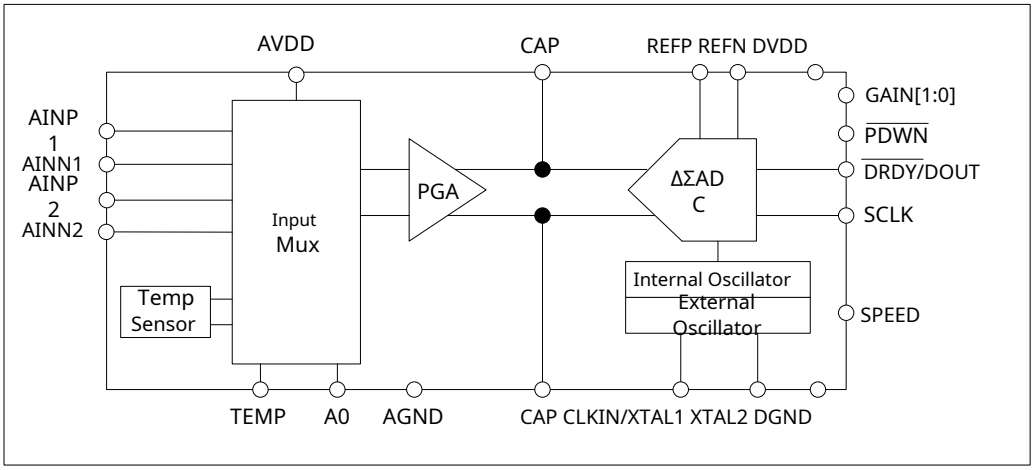
- Integrated low noisePGA, the magnification is optional1,2,64,128
- integrated2aisletwenty fourDifferential input with no missing codesADC,PGA=128TimeENOBfor20.8bit
- PPnoise:10Hz:139nV;80Hz:298nV
- integratedRCoscillator (±8%), or external crystal oscillator or clock input
- output rate10Hz/80Hzoptional
- integrated2WireSPICommunication Interface
- Integrated temperature sensor
- INLless than0.001%

1.2Chip applications

- Industrial Process Control
- electronic scale
- Liquid/Gas Chemical Analysis
- blood meter
- Smart Converter
- portable device

1.3Chip basic structure and function description

CS1232It is a high precision, low power consumptionSigma-DeltaAnalog-to-digital conversion chip, built-in1roadSigma-Delta ADCs. ADCthird-orderSigma-DeltaModulator, implemented with a low-noise instrumentation amplifier structurePGAmagnify, magnify optional1,2,64,128. existPGA=128, the effective resolution can reach20.8bit.CS1232output rate 10Hz/80HzOptional.CS1232built-inRCOscillator, you can use an external crystal oscillator, or you can use the pin CKIN/XTAL1Input the clock directly.CS1232haveStandby,Power downand other lower power modes.



picture1 CS1232Schematic diagram

1.4Chip maximum limit

surface1 CS1232limit value

name	symbol	minimum	maximum	unit
Analog supply voltage	AVDD	- 0.3	6	V
Digital supply voltage	DVDD	- 0.3	6	V
Voltage difference between digital ground and analog ground		- 0.3	0.3	V
Power instantaneous current			100	mA
Power constant current			10	mA
Digital pin input voltage		- 0.3	DVDD+0.3	V
Analog pin input voltage		- 0.3	AVDD+0.3	V
Festival temperature			150	°C
Operating temperature		- 40	105	°C
Storage temperature		- 60	150	°C
Chip pin soldering temperature			240	°C

1.5digital logic characteristics

surface2 CS1232digital logic characteristics

parameter	minimum	typical	maximum	unit	Condition Description
VIH	0.7×DVDD		DVDD+0.1	V	
VIL	DGND		0.3×DVDD	V	
VIH(PWDN)	0.8×DVDD		DVDD+0.1	V	
VIL(PWDN)	DGND		0.2×DVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2×DVDD	V	IoL=1mA
IIH			10	uA	VI=DVDD
IIL	- 10			uA	VI=DGND
External clock operating frequency range(1)	0.2	4.9152	8	MHz	
Serial port clock operating frequency range(2)			2	MHz	

(1) Chip operating clock frequency

(2) Frequency of serial communication clock SCLK

1.6Electrical Characteristics

All parameters tested at ambient temperature-20~85°C,AVDD = DVDD = 5V,REFP = 5V,REFN = 0V conditions, unless otherwise noted.

surface3 CS1232Electrical Characteristics (AVDD = DVDD = 5V)

parameter	condition	minimum	Typical value	maximum value	unit
analog input					
Full-scale input voltage (AINP-AIN)			±0.5VREF/PGA		V
Common Mode Input Voltage	PGA=1,2	AGND-0.1		AVDD+0.1	V
	PGA=64,128	AGND+1.5		AVDD-1.5	V
Common Mode Voltage Rejection Ratio			125		dB
Differential input impedance	PGA=64,128		> 1		GΩ
	PGA=1,2		> 1		GΩ
System performance					
Resolution	No missing codes		twenty four		Bits
ADrate	clock for4.9152MHz		10	80	Hz
Build time	full build		4		conversion cycle
PPnoise	PGA=128,DR=10Hz		139		nv
Integral linearity	PGA=128		±6		ppm
offset error	PGA=128		- 1		uV
offset error drift	PGA=128		25		nv/°C
gain error	PGA=128		±0.1		%
Gain Error Drift	PGA=128		6		ppm/°C
Reference voltage input					
Negative reference voltage input	REFN	AGND-0.1		AGND+0.6	V
Positive reference voltage input	REFP	REFN +2.5		AVDD+0.1	V
REFP-REFN		2.5	AVDD	AVDD+0.1	V
Reference Voltage Rejection Ratio			54		dB
power supply					
Analog supply voltage	AVDD	2.8	5	5.5	V
Digital supply voltage	DVDD	2.8	5	5.5	V
Supply Voltage Rejection Ratio	PGA=1,2		90		dB
	PGA=64,128		110		dB
Analog partial current	ordinary model PGA=1,2		2		mA
	ordinary model PGA=64,128		3		mA
	Standby mode		6		uA
	Power down		0.1		uA
Digital part current	normal mode		400		uA
	Standby mode		150		uA
	Power down		1.5		uA
clock					
Internal oscillator frequency		4.6	5	5.4	MHz
Built-in clock temperature drift			250		ppm/°C
External clock frequency		0.2	4.9152	8	MHz

All parameters tested at ambient temperature-20~85°C,AVDD = DVDD = 3V,REFP = 3V,REFN = 0Vconditions, unless otherwise noted.

surface4 CS1232Electrical Characteristics (AVDD = DVDD = 3V)

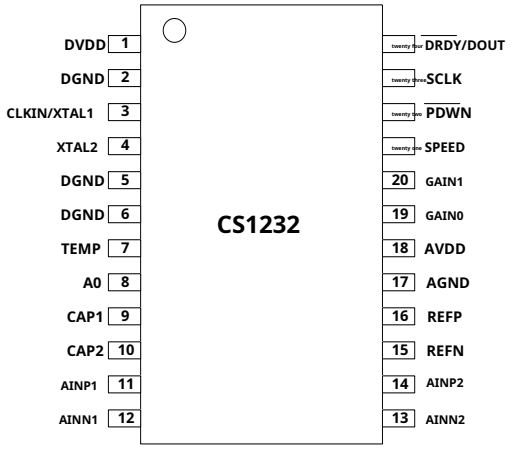
parameter	condition		minimum	Typical value	maximum value	unit
analog input						
Full-scale input voltage (AINP-AIN)				0.5VREF/PGA		V
Common Mode Input Voltage	PGA=1,2		AGND-0.1		AVDD+0.1	V
	PGA=64,128		AGND+1.5		AVDD-1.5	V
Common Mode Voltage Rejection Ratio				125		dB
Differential input impedance	PGA=64,128			> 1		GΩ
	PGA=1,2			> 1		GΩ
System performance						
Resolution	No missing codes			twenty four		Bits
ADrate	clock for4.9152MHz			10	80	Hz
Build time	full build			4		conversion cycle
PPnoise	PGA=128,DR=10Hz			145		nv
Integral linearity	PGA=128			±6		ppm
offset error	PGA=128			- 1		uV
offset error drift	PGA=128			25		nv/°C
gain error	PGA=128			±0.1		%
Gain Error Drift	PGA=128			6		ppm/°C
Reference voltage input						
Negative reference voltage input	REFN		AGND-0.1		AGND+0.6	V
Positive reference voltage input	REFP		REFN +1.5		AVDD+0.1	V
REFP-REFN			1.5	AVDD	AVDD+0.1	V
Reference Voltage Rejection Ratio				54		dB
power supply						
Analog supply voltage	AVDD		2.8	5	5.5	V
Digital supply voltage	DVDD		2.8	5	5.5	V
Supply Voltage Rejection Ratio	PGA=1,2			90		dB
	PGA=64,128			110		dB
Analog partial current	ordinary model	PGA=1,2		1.8		mA
		PGA=64,128		2.7		mA
	Standby mode			3		uA
	Power down			0.1		uA
Digital part current	normal mode			360		uA
	Standby mode			100		uA
	Power down			1.5		uA
clock						
Internal oscillator frequency			4.4	5	5.6	MHz
Built-in clock temperature drift				250		ppm/°C
External clock frequency			0.2	4.9152	8	MHz

1.7Noise performance

surface5Noise performance table

condition	speed	gain	RMSnoise	P-Pnoise	ENOB(RMS)	NOISE-FREE BITS
AVDD=5V VREF=5V	10Hz	1	400nV	1.69uV	23.6	21.5
		2	278nV	900nV	23.1	21.4
		64	23nV	149nV	21.7	19.0
		128	21nV	139nV	20.8	18.1
	80HZ	1	1.57uV	9.53uV	21.6	19
		2	903nV	5.87uV	21.4	18.7
		64	56nV	342nV	20.4	17.8
		128	56nV	298nV	19.4	17
AVDD=3V VREF=3V	10Hz	1	334nV	2.02uV	23.1	20.5
		2	291nV	1.43uV	22.3	20
		64	26nV	167nV	20.8	18.1
		128	23nV	145nV	20.0	17.3
	80HZ	1	2.02uV	11.44uV	20.5	18
		2	943nV	5.34uV	20.6	18.1
		64	63nV	383nV	19.5	16.9
		128	67nV	358nV	18.4	16

1.8chip pin



picture2 CS1232Chip Pin Diagram

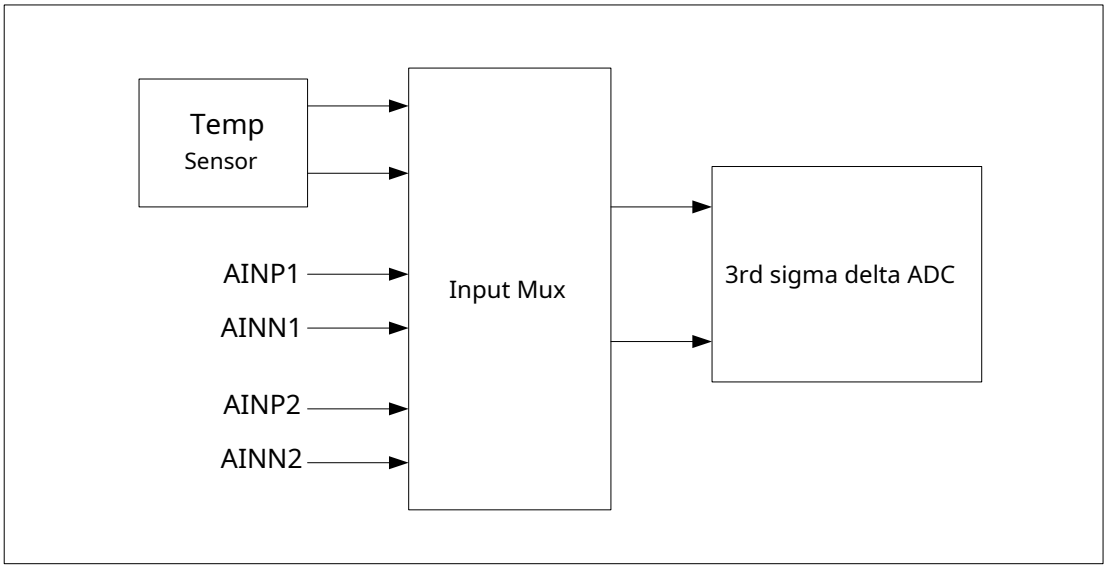
surface6 PINfoot description

serial number	pin name	input Output	illustrate
1	DVDD	P	digital power
2	DGND	P	digitally
3	CLKIN/XTAL1	DI	External crystal oscillator port, can provide external clock input
4	XTAL2	DI	External crystal oscillator port
5	DGND	P	digitally
6	DGND	P	digitally
7	TEMP	DI	Internal temperature sensor control:0: Disable;1:Enable
8	A0	AI	Channel selection:0: select channel1;1: select channel2
9	CAP1	AI	PGAamplifier output,CAP1,CAP2external connection between0.1uFcapacitance
10	CAP2	AI	
11	AINP1	AI	aisle1positive input
12	AINN1	AI	aisle1negative input
13	AINN2	AI	aisle2negative input
14	AINP2	AI	aisle2positive input
15	REFN	AI	Reference voltage negative input
16	REFP	AI	Reference voltage positive input
17	AGND	P	Analogously
18	AVDD	P	analog power
19	GAIN0	AI	PGAchoose GAIN1 / GAIN0 / GAIN 0 / 0 / 1 0 / 1 / 2 1 / 0 / 64 1 / 1 / 128
20	GAIN1	AI	
twenty one	SPEED	DI	Output rate selection: speed=0,10Hz;speed=1,80Hz
twenty two	$\overline{PWDN}$	DI	power downControl port (active low)
twenty three	SCLK	DI	SPIclock input port
twenty four	$\overline{DRDY}$/DOUT	DO	SPIData input/output port

2Chip function module description

2.1Analog input front end

CS1232have1roadADC,integrated2Channel differential input, signal input can be differential input signalAINP1, AINN1orAINP2,AINN2, can also be switched to the output signal of the temperature sensor.AINP1,AINN1or AINP2,AINN2switching byA0control, the switching of the temperature sensor is made byTEMPpin control. Its basic structure is As shown below:



picture3Analog Input Block Diagram

2.2Temperature Sensor

The temperature measurement function is provided inside the chip. whenPINfootTEMPWhen connected high,ADCThe analog signal input is connected to the internal temperature sensor, other analog input signals are invalid.ADCDerive by measuring the voltage difference output by the internal temperature sensor the actual temperature value. whenTEMP=1hour,ADConly supportPGA=1andPGA=2. when the pinGAIN0=0, TEMP=1, at this time the temperature sensorPGA=1. when the pinGAIN0=1,TEMP=1, at this time the temperature sensor ofPGA=2.

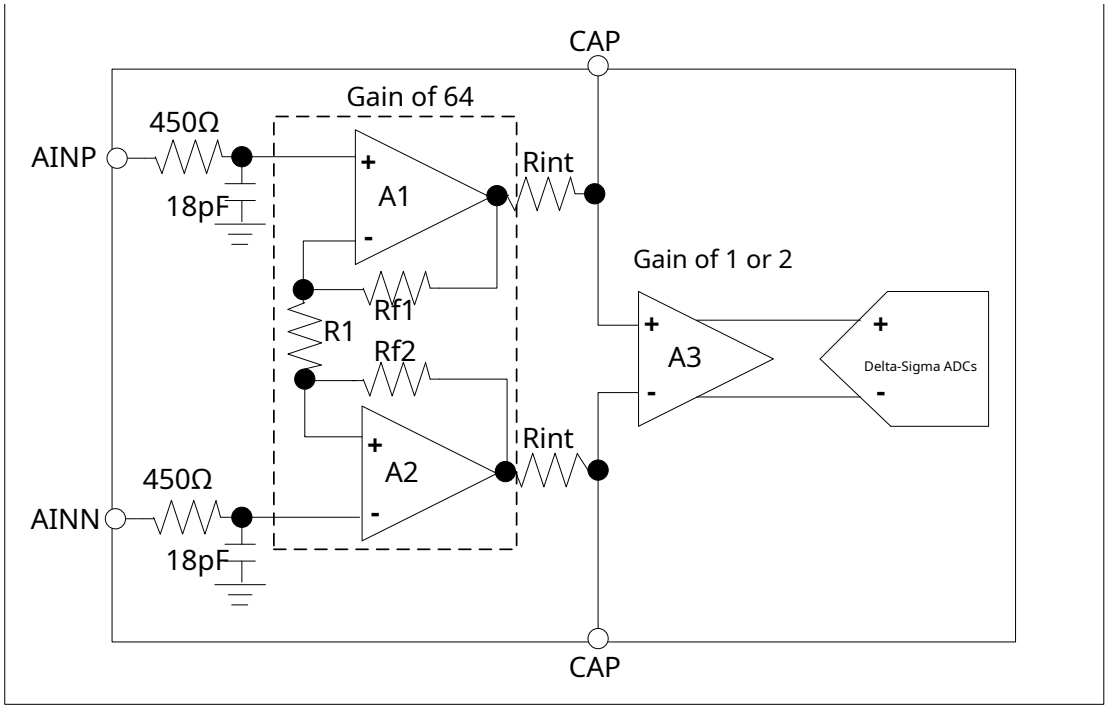
The temperature sensor requires a single point calibration. Correction method: at a certain temperature pointA, use the temperature sensor to measure get code valueYa.

Then other temperature pointsBcorresponding temperature =Yb*(273.15+A)/Ya-273.15

AThe unit of temperature is Celsius.YaYesAThe point corresponds to the temperature code value.YbYesBThe point corresponds to the temperature code value.

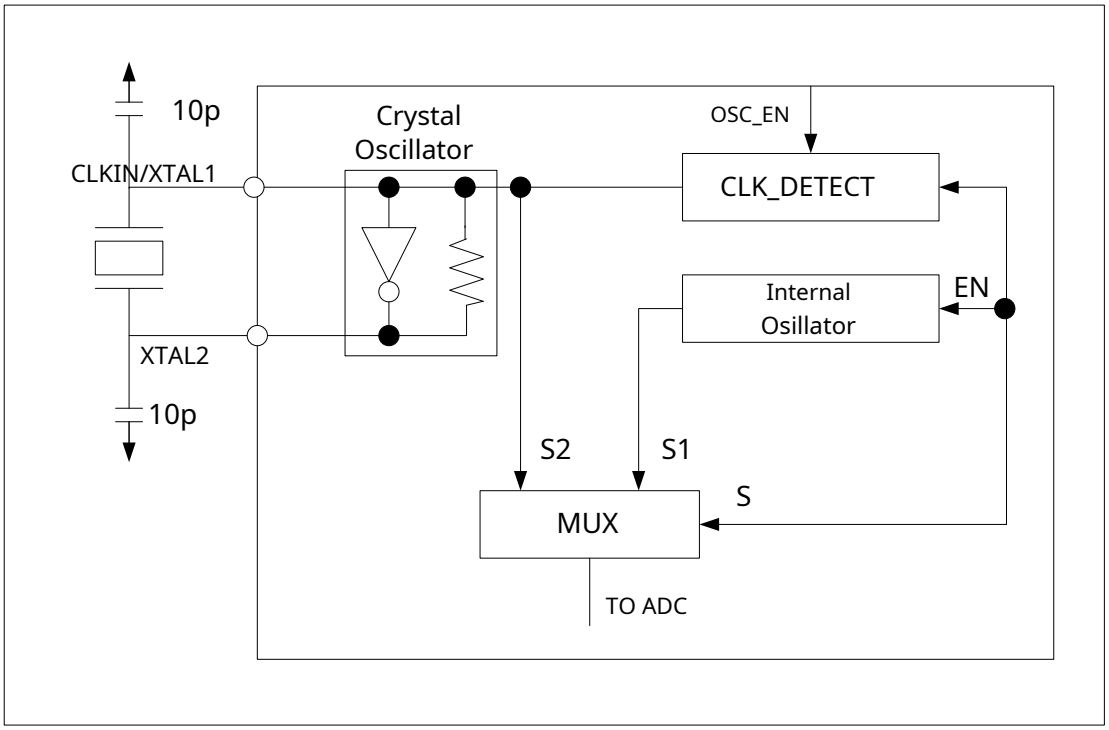
2.3low noisePGAamplifier

CS1232Integrated low noise, low driftPGAThe amplifier is connected to the differential output of the bridge sensor, and its internal basic structure is shown in the figure4shown, the pre-resistanceEMIfilter circuitR=450Ω,C=18pFaccomplish20MHigh frequency filtering. low noisePGAAmplifier throughRF1,R1,RF2accomplish64multiplied, and composed of the post-stage circuit 64and128ofPGAenlarge. through the pinGAIN1,GAIN0control to choose1times,2times,64times,128different gain multiples. when using PGA=1,2hour,64twice as low noisePGAThe amplifier is turned off to save power. existCAPconnect an external 0.1uF capacitor, with built-in2KOhm resistanceRINTform a low-pass filter circuit for low noisePGAhigh-frequency filtering of the amplifier output signal, while the low-pass filter can also be used asADCanti-aliasing filter.



picture4 PGAsStructure diagram

2.4clock source



picture5 CS1232clock signal

CS1232An external input clock, external crystal oscillator or built-in oscillator circuit can be used to provide the clock frequency required by the system, picture5forCS1232The basic structure diagram of the clock system,CLK_DETECTUsed to detect the presence of an external clock to determine turn off or turn on the built-in oscillator circuit, whenCLKIN/XTAL1frequency of more than200kHzhour,CLK_DETECTlose output low to turn off the built-in oscillator circuit, whenCLKIN/XTAL1frequency is less than200kHzhour,CLK_DETECTof Set the output high to turn on the built-in oscillator circuit, it is recommended to use the built-in oscillator circuit toCLKIN/XTAL1set low.

When using an external crystal, connect the crystal to the pinCLKIN/XTAL1andXTAL2, and inCLKIN/XTAL1and XTAL2pin connection10pcapacitor to ground.

2.5reset and power down (POR & power down)

When the chip is powered on, the built-in power-on reset circuit will automatically reset the chip. the pin$\overline{PDWN}$port is pulled low to enable Entire system entersPower downstate, when the power consumption is lower than1.6uA, in normal use the$\overline{PDWN}$Pull high.

2.6 SPISerial communication

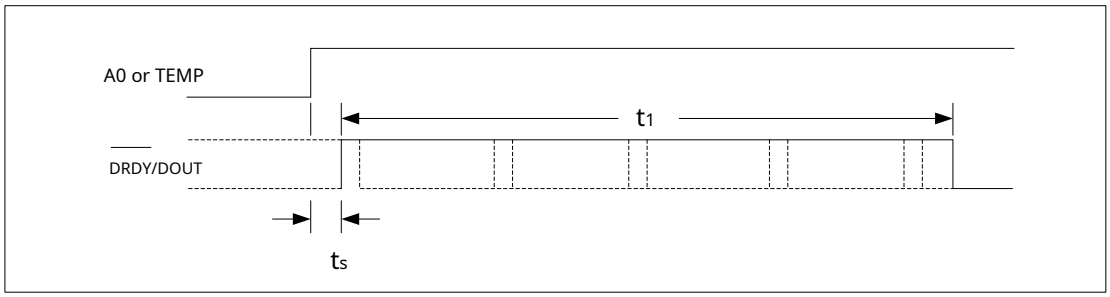
CS1232use2WireSPIserial communication, viaSCLKand*DRDY/DOUT*Data can be received. CS1232can continuously convert the analog input signal, when the*DRDY/DOUT*After being pulled low, it indicates that the data is ready, the first inputSCLKyou can puttwenty fourbitADThe MSB of the value is read, attwenty fourindivualSCLKAfter that, put all thetwenty fourbitDOUTdata read, after*DRDY/DOUT*Will keep the last bit of data until the next data is ready to pull high, after that when*DRDY/DOUT*It is pulled low again, indicating that the new data has been converted and the next data read can be performed. After receiving a set of data, it should keepSCLKlevel is low, preventingSCLK high level for too long, so thatCS1232mistakenlyStandbymodel. Each data read may not need to be read24bitdata, read all24bitThe data has no effect on the next analog-to-digital conversion.

2.6.1 Build time

The digital part needs four data conversion cycles to meet the settling time requirements of the analog input signal and the filter. core

The chip switches from an external differential input signal to a temperature sensor, from a temperature sensor to an external differential input signal, or via

It takes four data conversion cycles to switch between tracks until new correct data arrives. The whole establishment process is shown in the following figure:



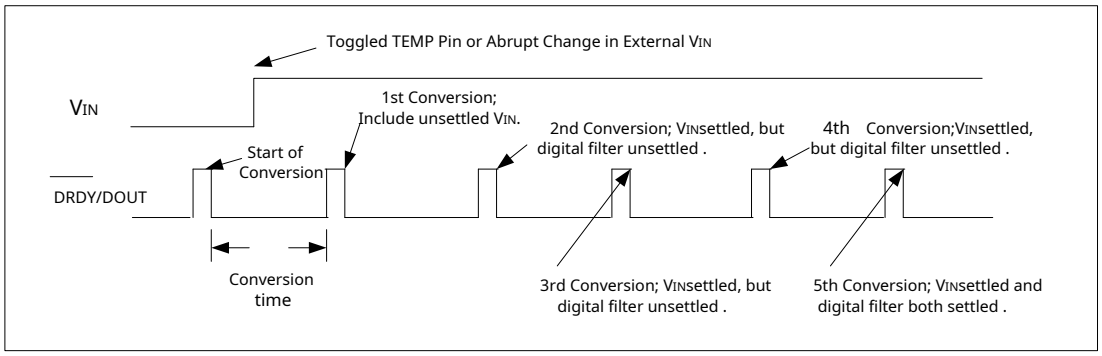
picture6ChangeA0orTEMPSettling time graph after pin input

surface7Setup Time Timing Diagram

parameter	describe(1)		minimum	maximum value	unit
ts	ChangeA0orTEMPpost build time		40	50	us
t1	build time (*DRDY/DOUT*keep high flat)	SPEED = 1	57	57	ms
		SPEED = 0	407	407	ms

(1)value is infclk=4.9152MHzWhen the corresponding value, differentfclkFrequency, value and other proportional changes.

CS1232During the continuous conversion process, if the external differential input signal changes suddenly, the settling time is also required. mutation signal needs4conversion cycles are established, the first5conversion cycles to get the finalADvalue. picture7Describing Mutation Letters number creation process. If the signal mutates again during the establishment process, the previous establishment is ignored and a new4indivual conversion cycle is established, followed by the first5conversion cycles to get the finalADvalue.



picture7 CS1232Settling time in continuous conversion mode

2.6.2 output rate

CS1232The output rate can be passed throughSPEEDpin settings. whenSPEEDWhen low, the output rate is 10Hz, the output rate has minimal noise, and50Hz/60HzNoise has a good suppression effect; whenSPEED When high, the output rate is80Hz.

surface8Output rate setting

SPEEDpin	output rate	
	clock for4.9152MHz	external clock
0	10Hz	f_{CLK}/491,520
1	80Hz	f_{CLK}/61,440

2.6.3 Data Format

CS1232The output data istwenty fourbit2Two's complement, MSB (MSB) is output first. least significant bit (LSB)for(0.5V_{REF}/Gain)/($2^{twenty\ three}$-1). A positive full-scale output code is7FFFFFH, the negative full-scale output code is 800000H. The table below shows the ideal output codes for different analog input signals.

surface9Ideal output code and input signal(1)

input signalV_{IN}(AINP-AINN)	ideal output
≥+0.5V_{REF}/Gain	7FFFFFH
(+0.5V_{REF}/Gain)/($2^{twenty\ three}$-1)	000001H
0	000000H
(-0.5V_{REF}/Gain)/($2^{twenty\ three}$-1)	FFFFFFH
≤+0.5V_{REF}/Gain	800000H

(1) regardless of noise,INL, the effects of offset error and gain error

2.6.4 Data preparation / data input and output (*DRDY/ DOUT*)

*DRDY/ DOUT*pins have2a use. First, when the output is low, it means that the new data has been converted; the third

Second, as a data output pin, when the data is ready, in the first1indivualSCLKAfter the rising edge of ,*DRDY/ DOUT*

Output the most significant bit of the converted data (MSB). in eachSCLKthe rising edge of , the data will automatically shift1bit. existtwenty fourindivual

SCLKAfter that, put all thetwenty fourbitDOUTdata read, after*DRDY/ DOUT*will keep the last digit

According to the data, it will be pulled high until the next data is ready, after that when the*DRDY/ DOUT*is pulled low again, indicating new data

The conversion has been completed, and the next data read can be performed.

2.6.5 Serial clock input (SCLK)

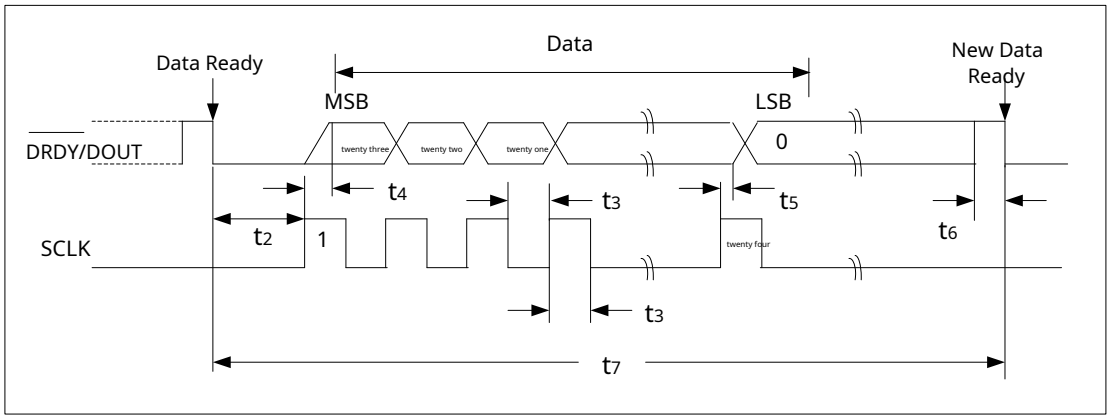
The serial clock input is a digital pin. This signal should be guaranteed to be a clean signal, glitch or slow rising edge

may result in reading incorrect data or erroneously entering an incorrect state. Therefore, it should be guaranteedSCLKThe rise and fall times are small

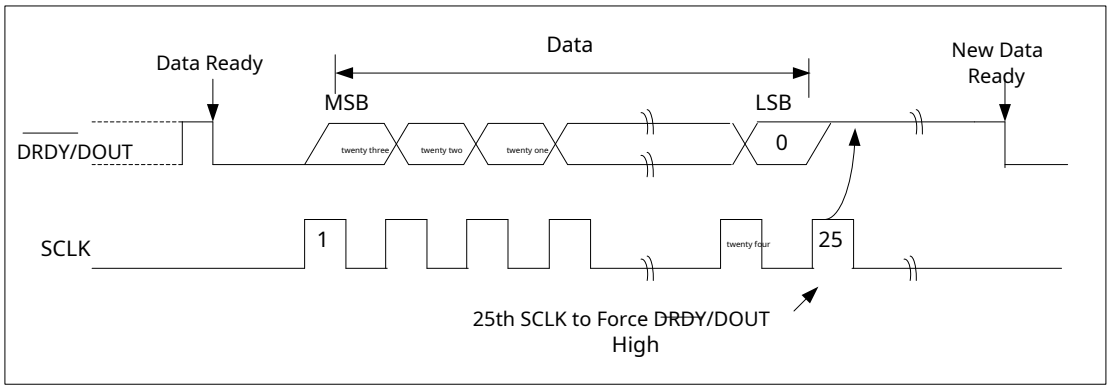
At50ns.

2.6.6 data reception

CS1232can continuously convert the analog input signal, when theDRDY/DOUTAfter pulling low, it indicates that the data is ready accept, the first enteredSCLKThe highest bit of the output can be read out, and thetwenty fourindivualSCLKAfter that, put all the twenty fourbitDOUTdata read, afterDRDY/DOUTwill hold the last bit of data until it is pulled high, pass pass25indivualSCLKcanDRDY/DOUTpulled high, then whenDRDY/DOUTis pulled low again, indicating a new The data is ready to be accepted for the next data transformation. Its basic timing is shown in the figure:



picture8 CS1232Read data timing diagram



picture9 CS1232read data timing and will*DRDY/DOUT*pull-up timing

surface10Read data timing table

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t2	*DRDY/DOUT*After going low to the firstSCLKrising edge		0			ns
t3	SCLKHigh-level or low-level pulse width		250			ns
t4	SCLKRising edge to new data bit valid (propagation delay)				200	ns
t5	SCLKRising edge to old data bit valid (hold time)		0			ns
t6	Data update, do not allow to read previous data		39			us
t7	Conversion time (1/data rate)	SPEED = 1		12.5		ms
		SPEED = 0		100		ms

2.6.7 Standbymodel

Standbymode reduces power consumption by shutting down most circuits. existstandbymode, the entire analog circuit is turned off, only

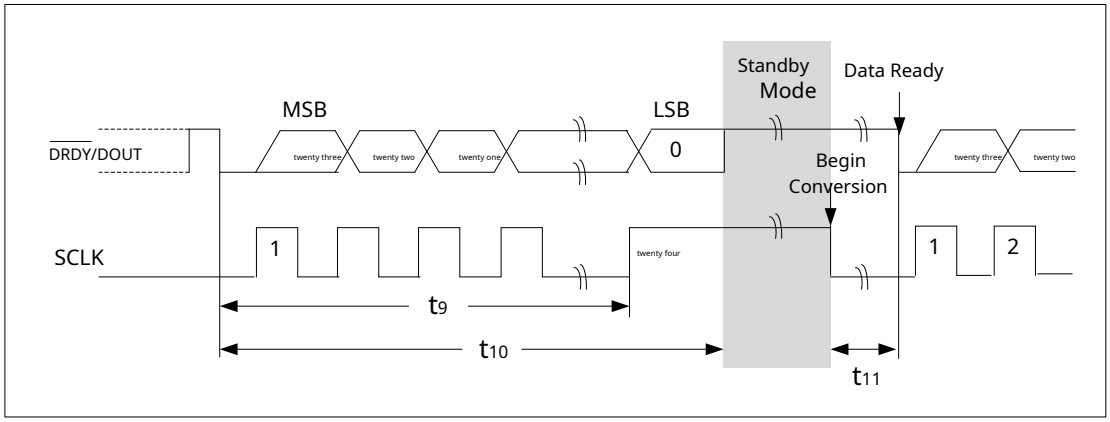
There is a clock circuit working. EnterstandbyThe way the pattern is,*DRDY/DOUT*After going low (data ready),

keepSCLKhigh level to enterstandbymodel. Enterstandbymode is the way to read data in any

in the process. whenSCLKkeep high to satisfyt10,Standbymode will be activated. Enterstandbymodel,

*DRDY/DOUT*will remain high. existstandbymodel,SCLKMust be held high at all times. whenSCLK

When going low, the chip exitsstandbyThe schema starts a new data transformation.



picture10 StandbyMode Timing Diagram

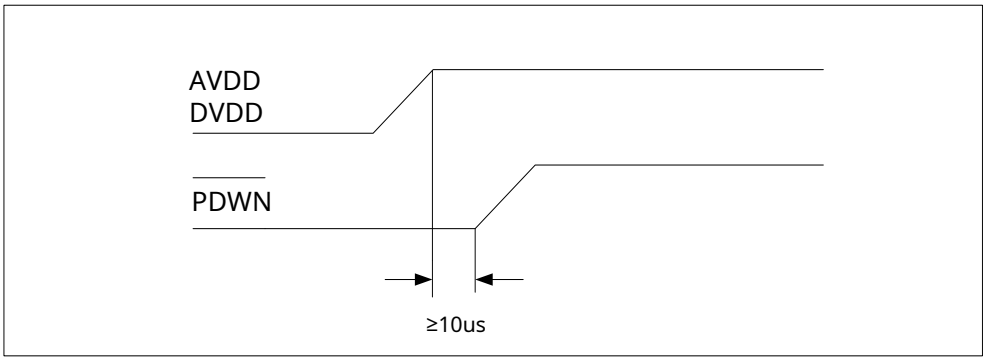
surface11 StandbyMode Timing Table

parameter	describe		minimum	maximum value	unit
t9(1)	exist*DRDY/DOUT*After going low, SCLKPull up to enterstandbymodel	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
t10(1)	standbyMode activation time	SPEED = 1	12.46		ms
		SPEED = 0	99.96		ms
t11(1)	quitstandbyAfter the data is ready	SPEED = 1	57	57	ms
		SPEED = 0	407	407	ms

(1)value is infclk=4.9152MHzWhen the corresponding value, differentfclkFrequency, value proportional change

2.6.8 Power up sequence

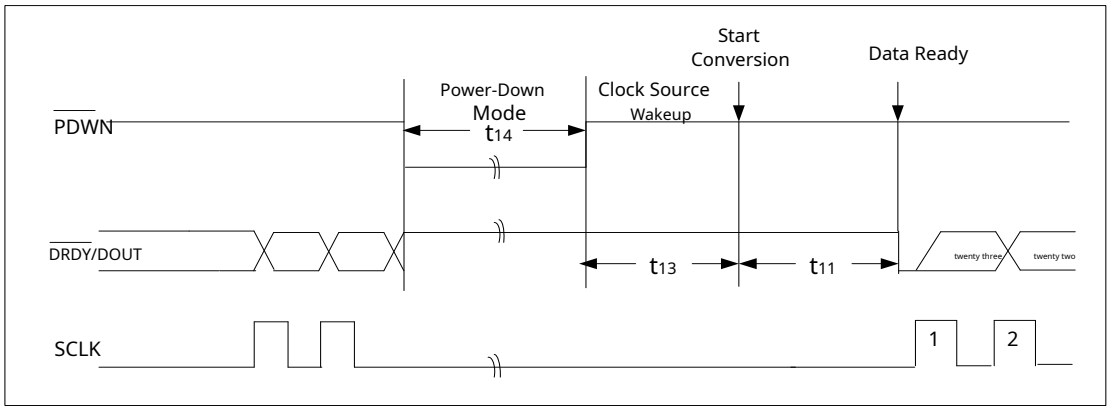
AVDDandDVDDgotta be*PDWN*Power up before the signal goes high.



picture11 CS1232Power-on sequence diagram

2.6.9 Power downmodel

*PDWN*When the signal is valid, all circuits of the chip are turned off, and the power consumption is less than1.6uA. just put*PDWN* pin is held low to enterPower downmodel.



picture12 Power DownMode Timing Diagram

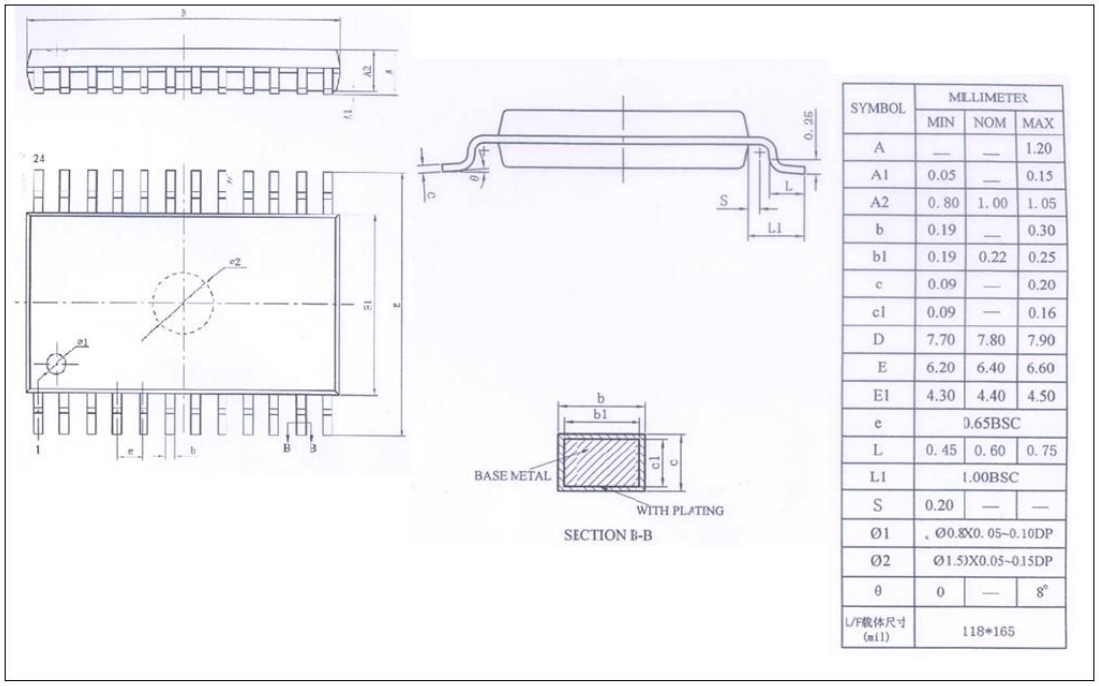
surface12 Power DownMode Timing Table

parameter	describe		Typical value	unit
t13(1)	existPOWER DOWNWake-up time in mode	internal time	7.95	us
		external time	0.16	us
		crystal oscillator	5.6	ms
t14(1)	*PDWN*pulse width		26 (min)	us

(1)value is infclk=4.9152MHzWhen the corresponding value, differentfclkFrequency, value proportional change

3 Chip packaging

useTSSOP-24package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
S	0.20	—	—
Ø1	，Ø0.8X0.05~0.10DP		
Ø2	Ø1.5)X0.05~0.15DP		
θ	0	—	8°
L/F载体尺寸 (mil)	118*165		

picture13chipTSSOP-24Package Size Information