芯海科技
CHIPSEA

CS1237User Manual

24-bit Sigma-Delta ADC

Rev 1.1

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Version history

historic version	Modify the content	version date
REV 1.0	initial version	2014-3-26
REV 1.1	1.Correct the format 2.Modify Differential Input Impedance Parameters 3.RevisePPNoise parameters 4.Modify Common Mode Input Range Parameters	2014-10-17

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1Chip function description

CS1237It is a high-precision, low-power analog-to-digital conversion chip, one differential input channel, built-in temperature sensor and High precision oscillator.

CS1237ofPGAOptional:1,2,64,128,The default is128.

CS1237in normal modeADCData output rate optional:10Hz,40Hz,640Hz,1.28kHz,default for10Hz;

MCUable to pass2linearSPIinterfaceSCLK,$\overline{DRDY}$/DOUTandCS1237to communicate, to row configuration, such as channel selection,PGAselection, output rate selection, etc.

1.1The main functional characteristics of the chip

- Built-in crystal oscillator
- Integrated temperature sensor
- bringPower downFunction
- 2WireSPIinterface, the fastest speed is1.1MHz

ADCFeatures:

- twenty fourNo missing codes
- PGAOptional magnification:1,2,64,128
- 1roadtwenty fourdifferential input with no missing codes, thePGA=128TimeENOBfor20bit (5V)\19.5bit (3.3V)
- PPnoise:PGA=128,10Hz:180nV;
- INLless than0.0015%
- Output rate optional:10Hz,40Hz,640Hz,1.28kHz
- In-band short function

1.2Chip applications

- Industrial Process Control
- electronic scale
- Liquid/Gas Chemical Analysis
- blood meter
- Smart Converter
- portable device

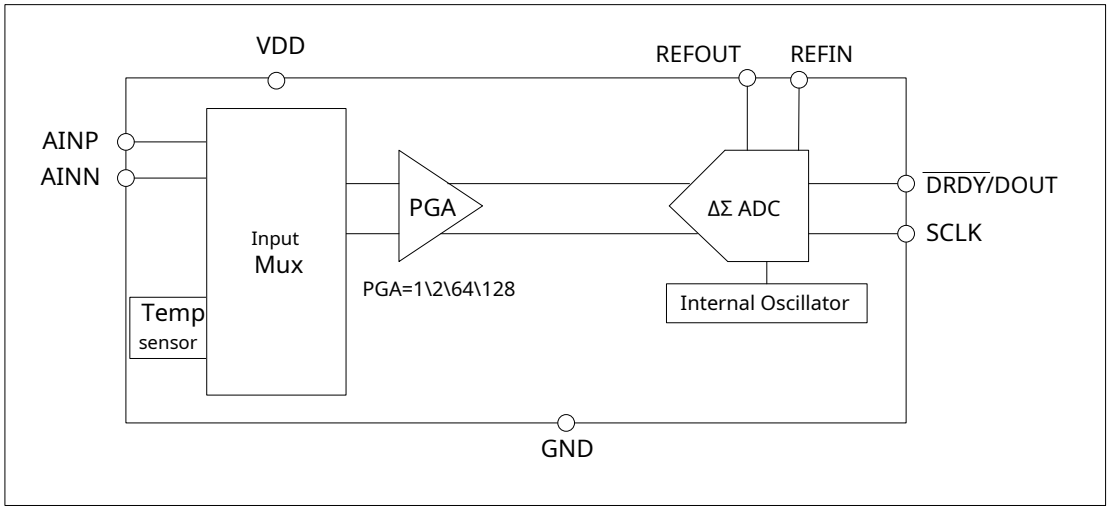
1.3Chip basic structure and function description

CS1237It is a high precision, low power consumptionSigma-DeltaAnalog-to-digital conversion chip, built-in one channelSigma-Delta ADC, one differential input channel and one temperature sensor,ADCtwo-stagesigma deltamodulator, via low noise The realization of the amplifier structure for sound instrumentPGAMagnification, the magnification is optional:1,2,64,128. existPGA=128when valid Resolution up to20bit (works in5V).

CS1237built-inRCOscillator, no external crystal is required.

CS1237able to pass*DRDY/DOUT*andSCLKConfiguration of various functional modes, e.g. as temperature detection,PGAchoose,ADCData output rate selection, etc.

CS1237havePower downmodel.



picture1 CS1237Schematic diagram

1.4Chip Absolute Maximum Limit

surface1 CS1237limit value

name	symbol	minimum	maximum	unit
voltage	VDD	- 0.3	6	V
Power instantaneous current			100	mA
Power constant current			10	mA
Digital pin input voltage		- 0.3	DVDD+0.3	V
Digital output pin voltage		- 0.3	DVDD+0.3	V
Festival temperature			150	°C
Operating temperature		- 40	85	°C
Storage temperature		- 60	150	°C
Chip pin soldering temperature			240	°C

1.5 CS1237digital logic characteristics

surface2 CS1237digital logic characteristics

parameter	minimum	typical	maximum	unit	Condition Description
VIH	0.7×DVDD		DVDD+0.1	V	
VIL	DGND		0.3×DVDD	V	
VOH	DVDD-0.4		DVDD	V	Ioh=1mA
VOL	DGND		0.2×DVDD	V	IoL=1mA
IIH			10	μA	VI=DVDD
IIL	- 10			μA	VI=DGND
serial clockSCLKworking frequency			1.1	MHz	

1.6 CS1237Electrical Characteristics

All parameters tested at ambient temperature-40~85℃ and built-in benchmark conditions, unless otherwise noted.

surface3 CS1237Electrical Characteristics (VDD = 5V,3.3V)

parameter	condition	minimum	Typical value	maximum value	unit
analog input					
Full-scale input voltage (AINP-AINN)			±0.5VREF/PGA		V
Common Mode Input Voltage	PGA=1,2	AGND-0.1		AVDD+0.1	V
	PGA=64,128	AGND+0.75		AVDD-0.75	V
Differential input impedance	PGA=1,2		190		MΩ
	PGA=64,128		28		MΩ
System performance					
Resolution	No missing codes		twenty four		Bits
ADrate			10	1280	Hz
Build time	full build	3: ADC output rate is 10\40Hz, 4: ADC output rate is 640\1280Hz			conversion cycle
PPnoise	PGA=128,10Hz		180		nv
Effective precision	PGA=128,10Hz		20(5V) 19.5(3.3V)		Bit
Integral linearity	PGA=128		±15		ppm
offset error	PGA=128		±1.4		μV
offset error drift	PGA=128		20		nv/°C
gain error	PGA=128		±0.5		%
Gain Error Drift	PGA=128		8		ppm/°C
Reference voltage input					
Reference voltage input	REFIN	1.5	VDD	VDD+0.1	V
Reference voltage output					
Reference voltage output	REFOUT		VDD		V
clock					
Internal oscillator frequency			5.2		MHz
Built-in clock temperature drift			250		ppm/°C
Temperature Sensor					
Temperature measurement error	TempError		±3		°C

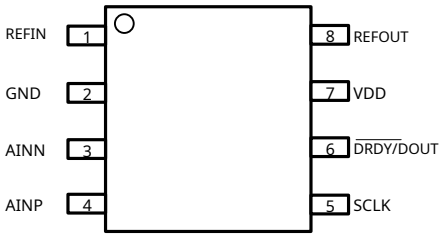
surface4 CS1237Power supply electrical characteristics (VDD = 5V)

parameter	condition		minimum	Typical value	maximum value	unit
voltage	VDD		4.5	5	5.5	V
Working current	normal model	PGA=1,2		1.57		mA
		PGA=64,128		2.34		mA
	Power down			0.1	0.1	μA

surface5 CS1237Power supply electrical characteristics (VDD = 3.3V)

parameter	condition		minimum	Typical value	maximum value	unit
voltage	VDD		3	3.3	3.6	V
Working current	normal model	PGA=1,2		1.26		mA
		PGA=64,128		2.11		mA
	Power down			0.1		μA

1.7chip pin



picture2 CS1237Chip Pin Diagram

surface6 PINfoot description

serial number	pin name	input Output	illustrate
1	REFIN	AI	Reference source input
2	GND	P	chip ground
3	AINN	AI	Channel Negative Input
4	AINP	AI	Channel positive input
5	SCLK	DI	SPIinput interface
6	$\overline{DRDY}$/DOUT	DI/DO	SPIData input\output interface
7	VDD	P	power supply
8	REFOUT	AO	Reference source output

Note:REFOUTThat is, the sensor excitation source output (the output value isVDD).

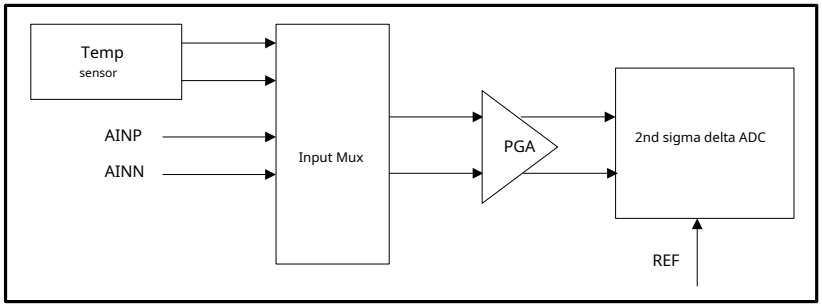
2Chip function module description

2.1Analog input front end

CS1237have1roadADC,Integrated1Differential input, the signal input can be a differential input signalAINP,

AINN, it can also be the output signal of the temperature sensor, the switching of the input signal is controlled by the register (ch_sel[1:0])control, its

The basic structure is shown in the following figure:



picture3Analog Input Block Diagram

CS1237ofPGAAvailable with:1,2,64,128, by register (pga_sel[1:0])control;

The reference voltage can be input externally or output internally. If you want to use an external reference voltage, you must first turn off the internal reference voltage.

reference, the internal reference is controlled by a register (refo_off)control.

2.2Temperature Sensor

The temperature measurement function is provided inside the chip. whench_sel[1:0]=2'b10hour,ADCThe analog signal input is connected to the internal temperature transmitter

sensor, other analog input signals are invalid.ADCThe actual voltage is derived by measuring the voltage difference output by the internal temperature sensor

actual temperature value. whench_sel[1:0]=2'b10hour,ADConly supportPGA=1.**The temperature sensor needs to be calibrated at one point**

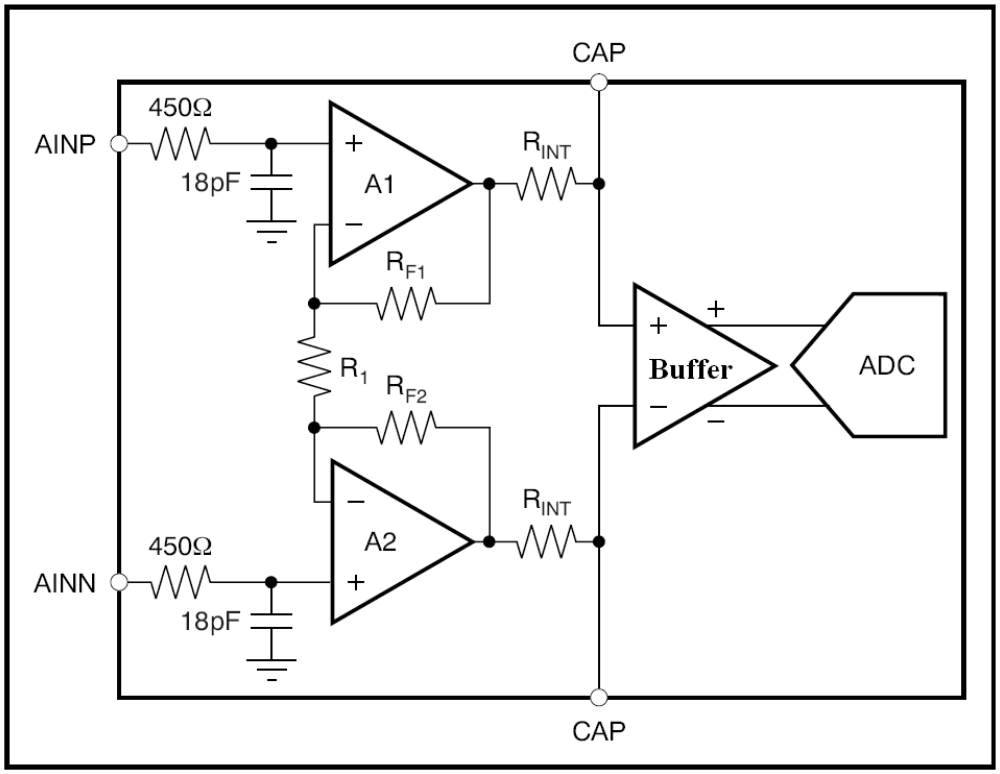
just. Correction method: at a certain temperature pointA, use the temperature sensor to measure to get the code valueYa.

Then other temperature pointsBcorresponding temperature =Yb*(273.15+A)/Ya-273.15

AThe unit of temperature is Celsius.YaYesAThe point corresponds to the temperature code value.YbYesBThe point corresponds to the temperature code value.

2.3low noisePGAamplifier

CS1237provides a low noise, low driftPGAThe amplifier is connected to the differential output of the bridge sensor, whose base The structure diagram is shown in the following figure, the pre-resistanceEMIfilter circuitR=450Ω,C=18pFaccomplish20MHigh frequency filtering. Low noisePGAAmplifier throughRF1,R1,RF2accomplish64multiplier, and switch capacitors with the post-stagePGAcomposition64and 128ofPGAenlarge. passpga_sel[1:0]to configure1,2,64,128etc. differentPGA. when using PGA=1,2hour,64twice as low noisePGAThe amplifier is turned off to save power. When using low noisePGAamplifier , the input range isGND+0.75VarriveVDD-0.75VIn between, beyond this range, will lead to actual performance degradation. existCAPa built-in port45pFcapacitor, with built-in2kresistanceRINTform a low-pass filter for low-noise VoicePGAhigh-frequency filtering of the output signal of the amplifier, while the low-pass filter can also be used asADCanti-aliasing filter device.



picture4 PGAsStructure diagram

CS1237built-inBuffer,whenPGA=1,2hour,CS1237useBufferto reduce due toADCDifferential input Problems caused by low impedance, such as insufficient settling time, large gain error, etc., whenPGA=64,128hour, CS1237also useBufferto reduce noise due to lowPGAgo throughRINT=2K,CINT=0.1μFAfter low pass filtering of The resulting set-up error, gain error and internal code drift.

2.4clock source

CS1237Use the built-in crystal oscillator to provide the clock frequency required by the system, the typical value is5.2MHz.

2.5reset and power down (POR&power down)

When the chip is powered on, the built-in power-on reset circuit will generate a reset signal to automatically reset the chip.

whenSCLKgo from low to high and stay high for more than100μs,CS1237i.e. enterPowerDwon mode, the power consumption is lower than0.1μA. whenSCLKWhen it returns to the low level, the chip will re-enter the normal working state state.

when the system isPower downWhen re-entering the normal working mode, all functions are configured asPowerDownOf In the previous state, no functional configuration is required.

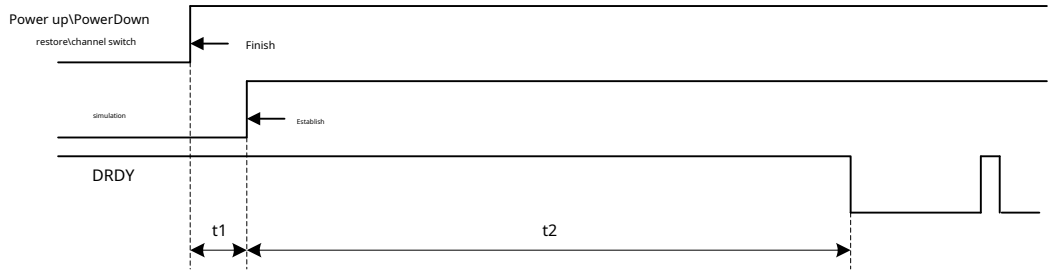
2.6 SPISerial communication

CS1237adopted in2WireSPIserial communication, viaSCLKand$\overline{DRDY/DOUT}$Data reception and function configuration can be realized.

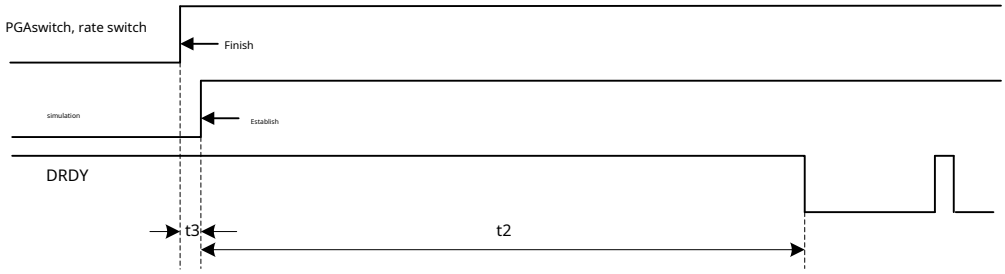
2.6.1 Build time

existADCThe data output rate is10Hzor40Hz, the digital part needs to have3The data conversion cycle satisfies the modulo Settling time requirements of the proposed input signal and filter;ADCThe data output rate is640Hzor1280Hzhour, The digital part needs to have4The data conversion cycle meets the settling time requirements of the analog input signal and the filter.

CS1237The whole establishment process is shown in the following figure:



picture5 CS1237data creation process1



picture6 CS1237data creation process2

parameter	describe(1)		minimum	Typical value	maximum value	unit
t1	Power up\PowerDownSettling time required for simulation after recovery\channel switching			2		ms
t3	PGASettling time required for simulation after switch\rate switch			0.8		μs
t2	build time ($\overline{DRDY/DOUT}$keep high flat)	10\40Hz		300\75		ms
		640\1280Hz		6.25\3.125		ms

2.6.2 ADCsData output rate

CS1237The data output rate can be set via the registerspeed_sel[1:0]configuration.

surface7Output rate setting

SPEED_SEL[1:0]	ADCoutput rate (Hz)
00	10
01	40
10	640
11	1280

2.6.3 Data Format

CS1237The output data istwenty fourbit2Two's complement, MSB (MSB) is output first. least significant bit (LSB)for($0.5V_{REF}$/Gain)/($2^{twenty\ three}$-1). A positive full-scale output code is7FFFFFH, the negative full-scale output code is 800000H. The table below shows the ideal output codes for different analog input signals.

surface8Ideal output code and input signal(1)

input signalV_{IN}(AINP-AINN)	**ideal output**
≥+$0.5V_{REF}$/Gain	7FFFFFH
(+$0.5V_{REF}$/Gain)/($2^{twenty\ three}$-1)	000001H
0	000000H
(-$0.5V_{REF}$/Gain)/($2^{twenty\ three}$-1)	FFFFFFH
≤+$0.5V_{REF}$/Gain	800000H

(1) regardless of noise,INL, the effects of offset error and gain error

2.6.4 Data preparation / data input and output (*DRDY/DOUT*)

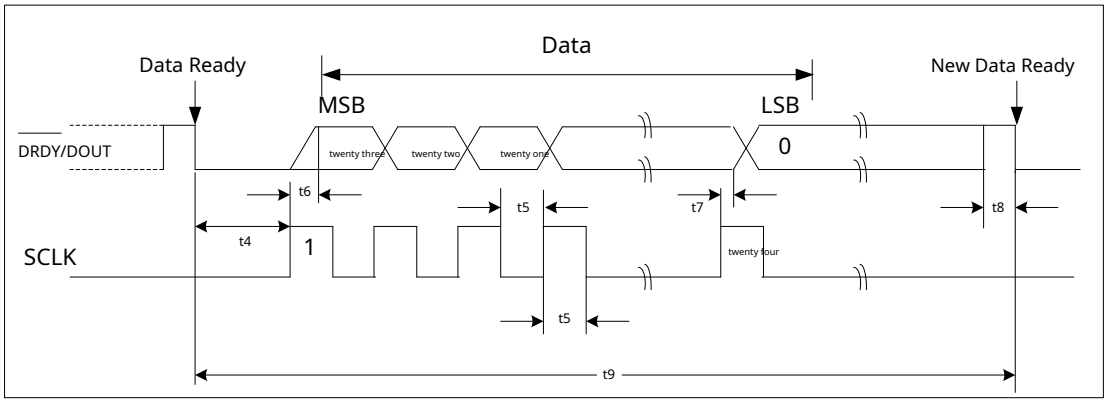
*DRDY/DOUT*pins have4a use. First, when the output is low, it means that the new data has been converted; the third Second, as a data output pin, when the data is ready, in the first1indivualSCLKAfter the rising edge of ,*DRDY/DOUT* Output the most significant bit of the converted data (MSB). in eachSCLKthe rising edge of , the data will automatically shift1bit. existtwenty fourindivual SCLKafter alltwenty fourbit data readout, if paused at this timeSCLKof sending,*DRDY/DOUT*will keep The last bit of data is pulled high until the next data is ready, after that when the*DRDY/DOUT*pulled again Low, indicating that the new data has been converted, and the next data reading can be performed; third, in the first25,26indivualSCLK When the register status update flag is output; fourth, as the register data write or read pin, when it is necessary to configure the register device or when reading register values,SPIneed to send46indivualSCLK,according to*DRDY/DOUT*Enter the command word, judge Whether it is a write register operation or a read register operation.

2.6.5 Serial clock input (SCLK)

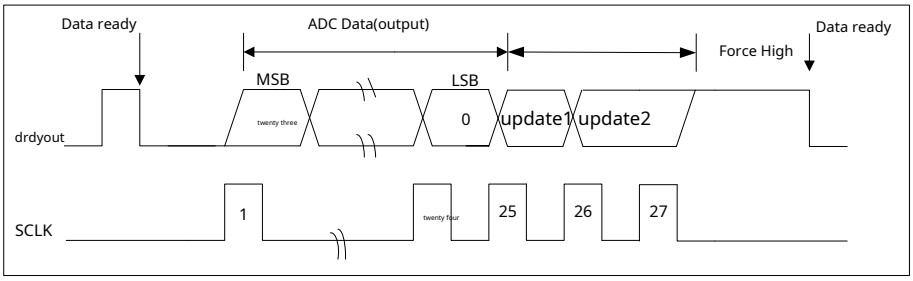
Serial clock inputSCLKis a digital pin. This signal should be guaranteed to be a clean signal, glitchy or slow A rising edge can cause incorrect data to be read or an incorrect state to be entered. Therefore, it should be guaranteedSCLKthe rise and fall of room is less than50ns.

2.6.6 data sending

CS1237can continuously convert the analog input signal, when the*DRDY/ DOUT*After being pulled low, it indicates that the data has ready to accept, the first enteredSCLKThe highest bit of the output can be read out, and thetwenty fourindivualSCLKafter all oftwenty fourbit data readout, if paused at this timeSCLKof sending,*DRDY/ DOUT*will keep the last digit According to, until it is pulled high, the first25and26indivualSCLKWhether the output configuration register has a write operation flag, the first25indivual SCLKcorresponding*DRDY/ DOUT*for1indicates the configuration registerConfigis written with a new value, the first26indivual SCLKcorresponding*DRDY/ DOUT*Reserved for chip expansion, the current output has always been0, through the27indivualSCLK can*DRDY/ DOUT*pulled high, then when*DRDY/ DOUT*is pulled low again, indicating that the new data has been accurate Ready to accept for the next data transformation. Its basic timing is shown in the figure:



picture7 CS1237Read data timing diagram1



picture8 CS1237Read data timing diagram2

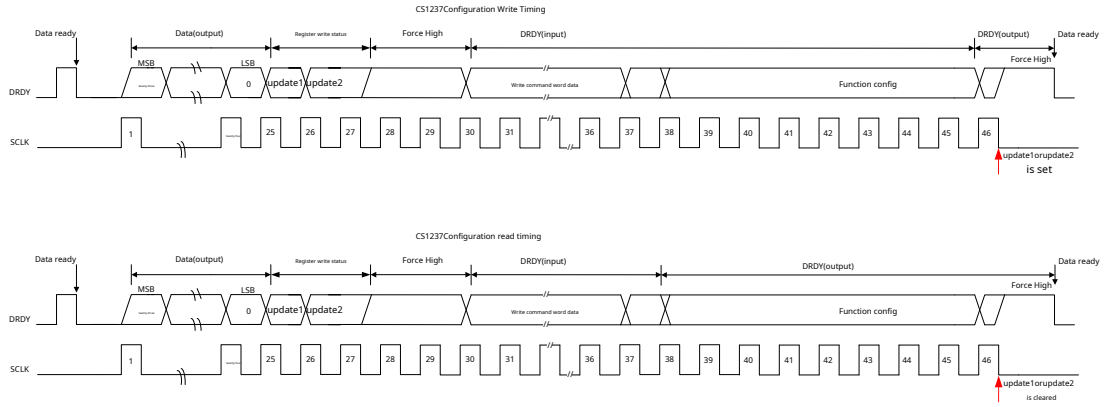
surface9Read data timing table

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
t4	*DRDY/ DOUT*After going low to the firstSCLKrising edge		0			ns
t5	SCLKHigh-level or low-level pulse width		455			ns
t6	SCLKRising edge to new data bit valid (propagation delay)		455			ns
t7	SCLKRising edge to old data bit valid (hold time)		227.5		455	ns
t8	Data update, do not allow to read previous data			26.13		μs
t9	Conversion time (1/data rate)	10Hz		100		ms
		40Hz		25		ms
		640Hz		1.5625		ms
		1280Hz		0.78125		ms

2.6.7 Functional configuration

CS1237able to pass SCLK and $\overline{DRDY/DOUT}$ Different functions can be configured, function configuration timing

The figure is shown in the following figure:



picture9Functional Configuration Timing Diagram

A brief description of the function configuration process, in $\overline{DRDY/DOUT}$ After changing from high to low:

1.the first1to thetwenty fourindivualSCLK, readADCdata. If no configuration register or read memory, you can omit the following steps.

2.the first25to the26indivualSCLK, read the register write status.

3.the first27indivualSCLK,Bundle $\overline{DRDY/DOUT}$ The output is pulled high.

4.the first28to the29indivualSCLK, toggle $\overline{DRDY/DOUT}$ for input.

5.the first30to the36indivualSCLK, input register write or read command word data (high order input first).

6.the first37indivualSCLK, toggle $\overline{DRDY/DOUT}$ direction (if writing a register, $\overline{DRDY/DOUT}$ is an input; if it is a read register, $\overline{DRDY/DOUT}$ for output).

7.the first38to the45indivualSCLK, input register configuration data or output register configuration data (high order input/ output first).

8.the first46indivualSCLK, toggle $\overline{DRDY/DOUT}$ for output, and put $\overline{DRDY/DOUT}$ Pull high. update1/ update2is set or cleared.

2.6.7.1 SPICommand word

CS1237Have2command word, the length of the command word is7bits, the command word description is as follows:

surface10 CS1237Command word description table

command name	command byte	describe
write configuration register	0x65	write configuration registerConfig
read configuration register	0x56	read configuration registerConfig

2.6.7.2 SPIregister

CS1237has a set of registersConfig.

Configregister

register	R/W	describe	reset value
describe	reserved bit	configuration register	0x0C

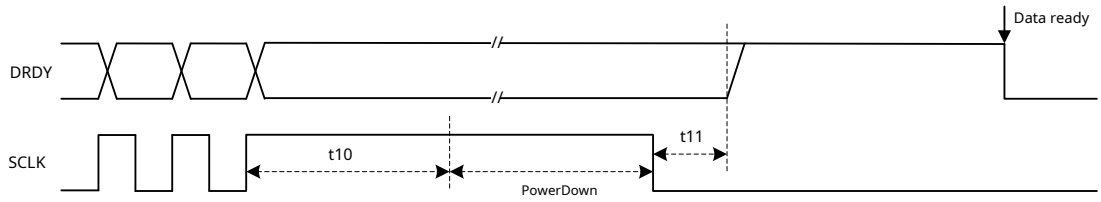
configuration bits	B7	B6	B5	B4
describe	reserved bit	REFoutput switch	ADCOutput rate selection	
configuration bits	B3	B2	B1	B0
describe	PGAchoose		Channel selection	

surface11 ConfigRegister Description Table

Bits	describe	
[7]	-	The chip reserves the used bits.**The default is0, write while writing0, do not write1**
[6]	REFO_OFF	**REFOutput switch:**defaultREFoutput on 1=closureREFoutput. 0=REFnormal output.
[5:4]	SPEED_SEL	**ADCOutput rate selection:**The default is10Hz SPEED_SEL[1:0] / describe 00 / ADCThe output rate is10Hz 01 / ADCThe output rate is40Hz 10 / ADCThe output rate is640Hz 11 / ADCThe output rate is1280Hz
[3:2]	PGA_SEL	**PGAchoose:**defaultPGAfor128, in temperature measurement modePGA_SEL=00 PGA_SEL[1:0] / describe 00 / 1 01 / 2 10 / 64 11 / 128
[1:0]	CH_SEL[1:0]	**Channel selection**: The default channel is the channelA CH_SEL[1:0] / describe 00 / aisleA 01 / Chip retention use bit 10 / temperature 11 / inner short

2.6.8 Power downmodel

whenSCLKgo from low to high and stay high for more than100μs,CS1237i.e. enterPowerDwon mode, all circuits of the chip will be turned off at this time, and the power consumption will be close to0. whenSCLKWhen it returns to the low level, the chip will re-enter the normal working state.



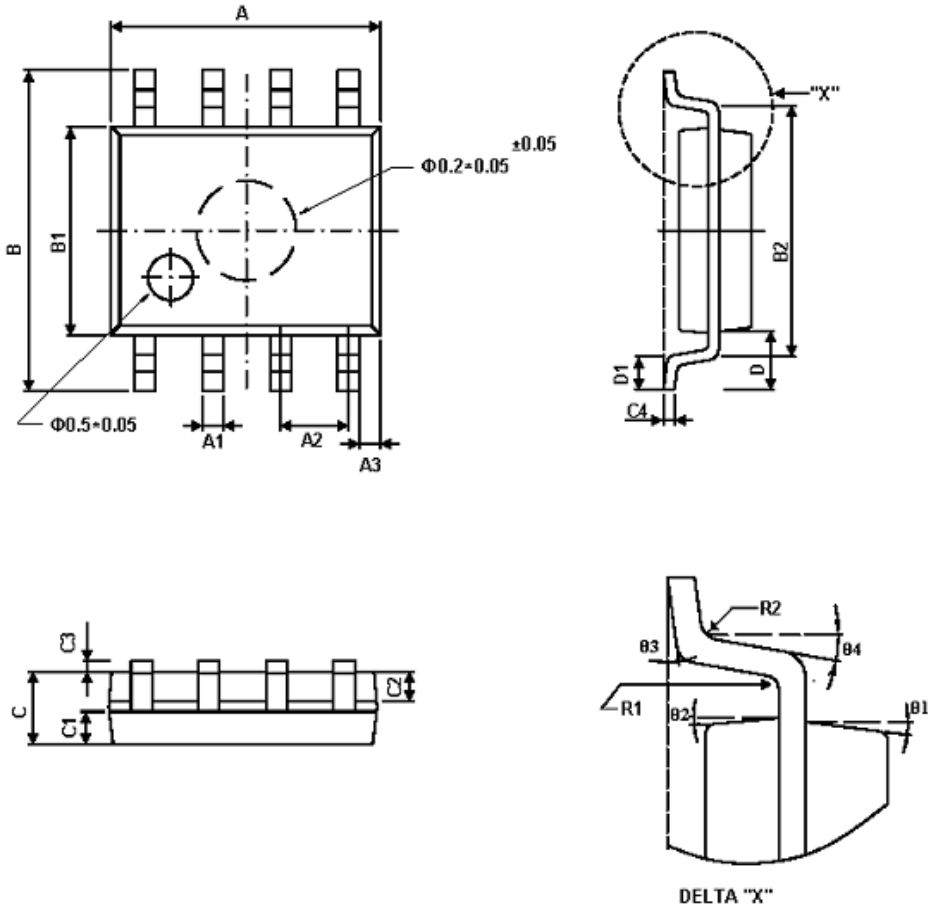
picture10 CS1237 PowerDownMode diagram

symbol	describe	minimum	Typical value	maximum value
t10	SCLKHigh level hold time	100μs		
t11	SCLKLow level hold time after falling	10μs		

3 Chip packaging

CS1237useSOP8package.

尺寸 / 标注	最小 （mm）	最大 （mm）	尺寸 / 标注	最小 （mm）	最大 （mm）
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20TYP	
A2	1.27TYP		D	1.05TYP	
A3	0.41TYP		D1	0.40	0.60
B	5.80	6.20	R1	0.07TYP	
B1	3.80	4.00	R2	0.07TYP	
B2	5.0TYP		θ1	17°TYP	
C	1.30	1.50	θ2	13°TYP	
C1	0.55	0.65	θ3	4°TYP	
C2	0.55	0.65	θ4	12°TYP	



picture11chipSOP8Package Size Information