芯海科技
CHIPSEA

CS1243User Manual

24-bit Sigma-Delta ADC

Rev 1.0

Mailing address: 9th Floor, Block A, Garden City Digital Building, No. 1079 Nanhai Avenue, Shekou, Nanshan District, Shenzhen

Postal Code: 518067

Company Tel: +(86 755)86169257

Fax: +(86 755)86169057

Company website: www.chipsea.com

WeChat ID: Chipsea Technology

Wechat QR code:

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Figure Catalog

table directory

1Function Description

CS1243It is a high-precision, low-power analog-to-digital conversion chip. Its resolution is24bit, the effective resolution can reachtwenty twobit. can be widely Widely used in process control, weight, liquid/gas chemical analysis, blood analysis, smart transmitters, portable measuring instruments area.

1.1 CS1243Main functional features

- twenty fourNo missing codes,twenty twoBit effective precision analog-to-digital converter
- integrated50Hz,60HzNotch (up to -90dB)
- INLless than0.0015%
- Programmable gain (1~128)
- Single clock cycle ready
- Programmable analog-to-digital conversion (ADC) data rate output
- The external reference voltage range can be0.1V~5V
- chip with calibration
- Integration CompatibleSPIbus interface
- Low power consumption, minimum0.6mW
- 8analog input channels

1.2Application

- Industrial Process Control
- weight meter
- Liquid/Gas Chemical Analysis
- blood meter
- Smart Converter
- portable device

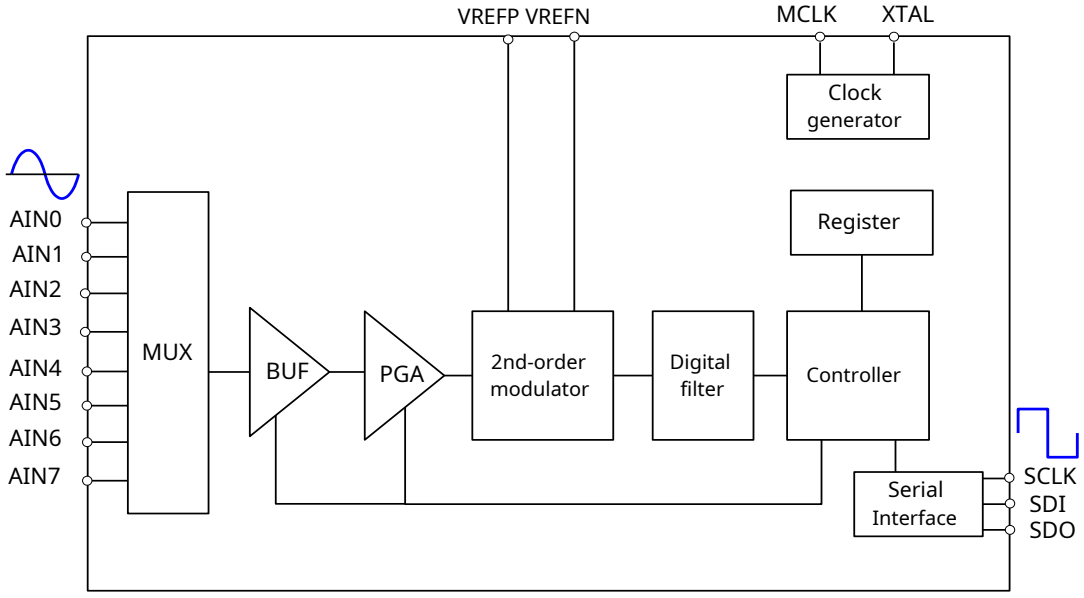
1.3Function description

CS1243Yestwenty fourBit high precision, low power consumptionSigma-DeltaAnalog-to-digital conversion chip, effective resolution up totwenty twobit. allowable 2.7V~5.5VOperates under supply voltage conditions.

CS1243Have8analog input channels. Input channel analog buffers can be selected (Buffer) or directly input the signal to the digital converter (ADC), the analog buffer can effectively improve the input impedance of the chip.

CS1243which provided1~128times programmable gain amplifier, the128times,CS1243Effective resolution up to18bit. tune The controller is a second-orderSigma-Deltamodulator, chipFIRfilter provided50Hzand60HzNotch filter, effectively improve High chip anti-interference performance.

CS1243supplySPICompatible serial interface bus.



picture1 CS1243Schematic diagram

2Feature Description

2.1Chip Absolute Maximum Limit

surface1 CS1243limit value

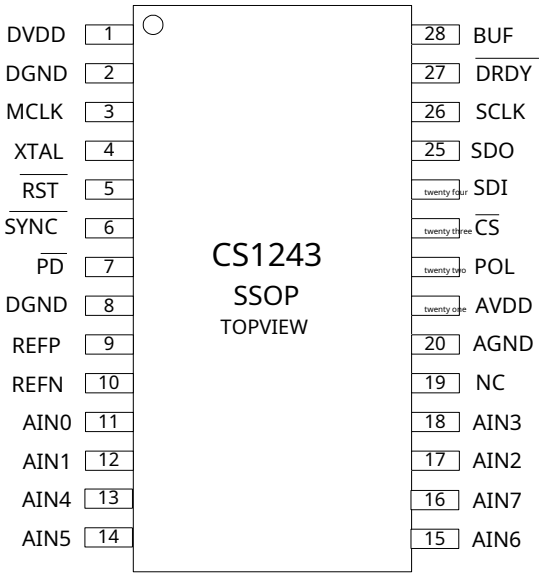
name	symbol	minimum	maximum	unit	illustrate
Analog supply voltage	AVDD	- 0.3	6	V	AVDD to AGND
Digital supply voltage	DVDD	- 0.3	6	V	DVDD to DGND
pressure difference between ground	DVGND	- 0.3	0.3	V	DGND to AGND
Power instantaneous current			100	mA	Input Current momentary
Power constant current			10	mA	Input Current continuous
Digital pin input voltage		- 0.3	DVDD+0.3	V	Digital Output Voltage to DGND
Digital output pin voltage		- 0.3	DVDD+0.3	V	
Festival temperature			150	oC	Max. Junction Temperature
Operating temperature		- 40	85	oC	Operating Temperature
Storage temperature		- 60	150	oC	Storage Temperature
Chip pin soldering temperature			300	oC	Lead Temperature (Soldering, 10s)

2.2digital logic characteristics

surface2 CS1243digital logic characteristics

parameter	minimum	typical	maximum	unit	Condition Description
VIH	0.8×DVDD		DVDD	V	
VIL	DGND		0.2×DVDD	V	
VOH	DVDD-0.4		DVDD+0.4	V	Ioh=1mA
VOL	DGND		DGND+0.4	V	IoL=1mA
IIH			10	uA	VI=DVDD
IIL	- 10			uA	VI=DGND
fosc	1		5	MHz	
tosc	200		1000	ns	
illustrate: 1,CS1243The digital interface isCMOSlogical interface.					

2.3chip pin



picture2 CS1243Pin Diagram

surface3 CS1243Pin description

pin number	symbol	Pin description	Remark
1	DVDD	digital supply voltage,2.7~5.25V	
2	DGND	digitally	
3	MCLK	master clock input,1~10MHz	
4	XTAL	Crystal drive pin2	
5	$\overline{RST}$	Chip reset pin, active low	
6	$\overline{SYNC}$	Synchronous control signal, active low	
7	$\overline{PD}$	Power-down control signal, active low	
8	DGND	digitally	
9	REFP	Analog (positive) reference voltage input	
10	REFN	Analog (negative) reference voltage input	
11	AIN0	analog input0	
12	AIN1	analog input1	
13	AIN4	analog input4	
14	AIN5	analog input5	
15	AIN6	analog input6	
16	AIN7	analog input7	
17	AIN2	analog input2	
18	AIN3	analog input3	
19	NC	dead end	
20	AGND	Analogously	
twenty one	AVDD	Analog supply voltage2.7V~5.25V	
twenty two	POL	Serial Clock Polarity	
twenty three	$\overline{CS}$	Chip select signal, active low	
twenty four	SDI	Serial input data	

pin number	symbol	Pin description	Remark
25	SDO	Serial output data	
26	SCLK	Serial port working clock, usingSchmitttrigger	
27	$\overline{\text{DRDY}}$	Data ready indication signal, active low	
28	BUF	Analog input buffer enable signal, active high	

2.4Electrical Characteristics

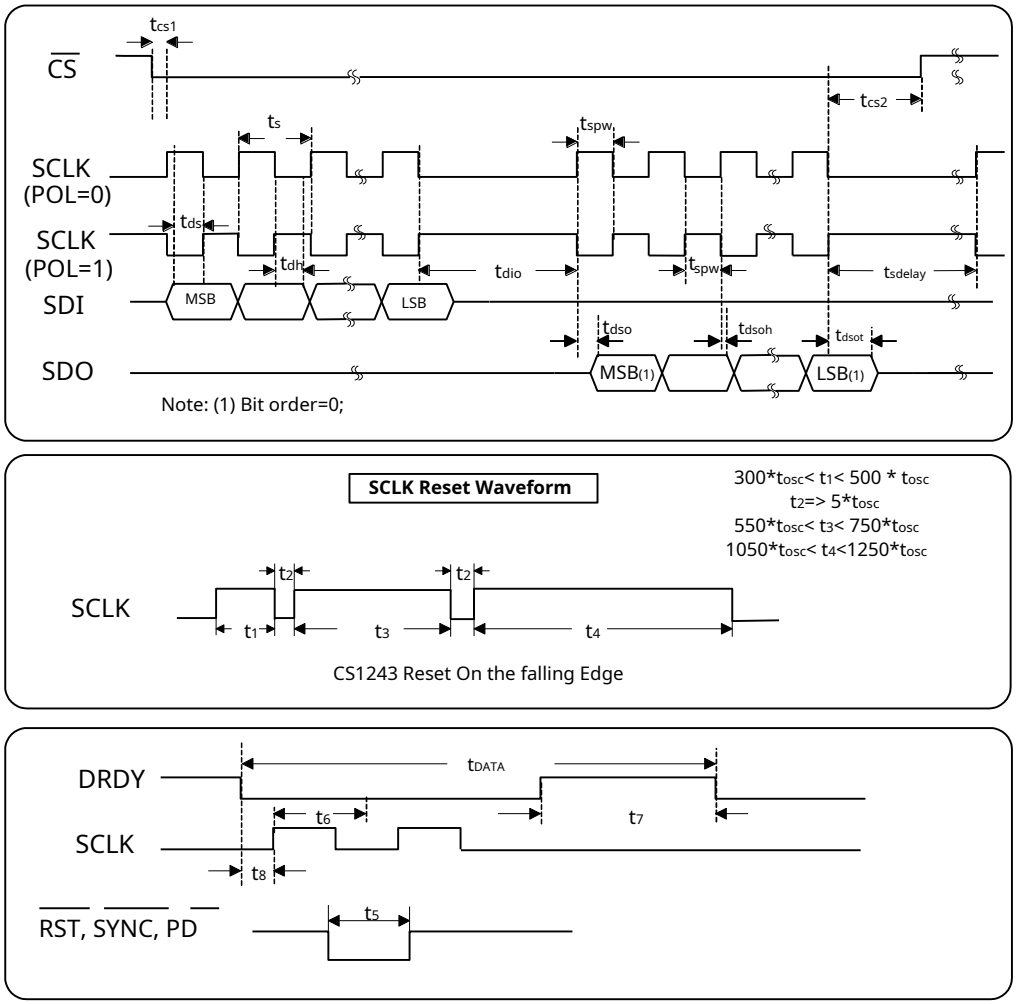
surface4 AVDD=5VTimeCS1243Electrical Characteristics

parameter		condition	minimum	Typical value	maximum value	unit
analog input	Analog input range	Bufferclosure	AGND-0.1		AVDD+0.1	V
		BufferOpen	AGND+0.4		AVDD-1.5	V
	Full-scale input voltage (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2×PGA)	V
	Differential input impedance	Bufferclosure		5/PGA		MΩ
		BufferOpen		5		GΩ
	bandwidth(-3dB)	f_{DATA}= 3.75Hz		1.65		Hz
		f_{DATA}= 7.50Hz		3.44		Hz
		f_{DATA}= 15.0Hz		3.7		Hz
	PGA	Selectable Gain Range	1		128	
	input capacitance			9		pF
	Input leakage current	modulator off,T = 25°C		5		pA
	Test current source			2		2uA
System performance	Resolution	No missing codes		twenty four		Bits
	Integral linearity				±0.0015	% of FS
	offset error			8		ppm of FS
	offset error drift			0.02		ppm of FS/°C
	gain error			0.005		%
	Gain Error Drift			0.5		ppm/°C
	Common Mode Rejection Ratio	DC	100			dB
		f_{CM}= 60Hz, f_{DATA}= 15Hz		130		dB
		f_{CM}= 50Hz, f_{DATA}= 15Hz		120		dB
	Notch rejection ratio	f_{CM}= 60Hz, f_{DATA}= 15Hz		100		dB
		f_{SIG}= 50Hz, f_{DATA}= 15Hz		100		dB
	power supply rejection ratio	DC	80	95		dB
reference voltage enter	VREF≡REFP - REFN	RAN = 0	0.1	2.5	2.6	V
		RAN=1	0	2.5	AVDD	V
	REFP,REFN input range	RAN = 0	0		AVDD	V
		RAN=1	0.1		AVDD	V
	Common Mode Rejection Ratio	DC		120		dB
		f_{VREFCM}= 60Hz		120		dB
	Bias current			1.3		uA
power supply	voltage	AVDD	4.75		5.25	V
	Analog partial current	$\overline{PD}$ = 0		1		nA
		PGA = 1,Bufferclosure		120		uA
		PGA = 1,BufferOpen		160		uA
		PGA = 128,Bufferclosure		400		uA
		PGA = 128,BufferOpen		760		uA
	Digital part current (DVDD = 5V)	normal mode		2		mA
		Continuous read data mode		2.2		mA
		$\overline{PD}$ = 0		0.5		nA

surface5 AVDD=3VTimeCS1243Electrical Characteristics

parameter		condition	minimum	Typical value	maximum value	unit
analog input	Analog input range	Bufferclosure	AGND-0.1		AVDD+0.1	V
		BufferOpen	AGND+0.3		AVDD-1.5	V
	Full-scale input voltage (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2×PGA)	V
	Differential input impedance	Bufferclosure		5/PGA		MΩ
		BufferOpen		5		GΩ
	bandwidth(-3dB)	f_{DATA}= 3.75Hz		1.65		Hz
		f_{DATA}= 7.50Hz		3.44		Hz
		f_{DATA}= 15.0Hz		14.6		Hz
	PGA	Selectable Gain Range	1		128	
	input capacitance			9		pF
	Input leakage current	modulator off,T = 25°C		5		pA
	Test current source			2		2uA
System performance	Resolution	No missing codes		twenty four		Bits
	Integral linearity				±0.0015	% of FS
	offset error			15		ppm of FS
	offset error drift			0.04		ppm of FS/°C
	gain error			0.01		%
	Gain Error Drift			1.0		ppm/°C
	Common Mode Rejection Ratio	DC	100			dB
		f_{CM}= 60Hz, f_{DATA}= 15Hz		130		dB
		f_{CM}= 50Hz, f_{DATA}= 15Hz		120		dB
	Notch rejection ratio	f_{CM}= 60Hz, f_{DATA}= 15Hz		100		dB
		f_{SIG}= 50Hz, f_{DATA}= 15Hz		100		dB
	power supply rejection ratio	DC	75	90		dB
reference voltage enter	VREF≡REFP - REFN	RAN = 0	0.1	1.25	1.30	V
		RAN=1	0	2.5	2.6	V
	REFP,REFN input range	RAN = 0	0		AVDD	V
		RAN=1	0.1		AVDD	V
	Common Mode Rejection Ratio	DC		120		dB
		f_{VREFCM}= 60Hz		120		dB
	Bias current			0.65		uA
power supply	voltage	AVDD	2.7		3.3	V
	Analog partial current	$\overline{PD}$ = 0		1		nA
		PGA = 1,Bufferclosure		107		uA
		PGA = 1,BufferOpen		118		uA
		PGA = 128,Bufferclosure		360		uA
		PGA = 128,BufferOpen		500		uA
	Digital part current (DVDD = 3V)	normal mode		2		mA
		Continuous read data mode		2.2		mA
		$\overline{PD}$ = 0		0.5		nA

2.5Communication timing



picture3 CS1243Timing diagram

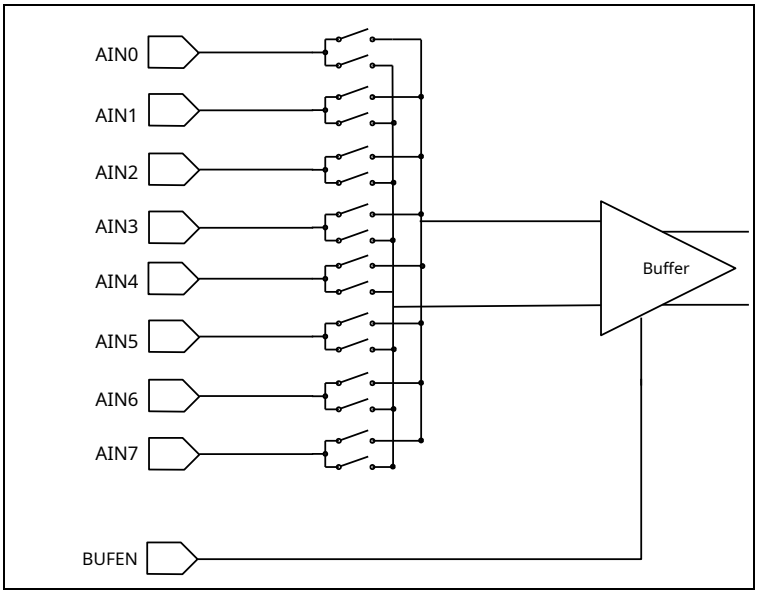
surface6 CS1243Timetable

parameter	describe		minimum	maximum value	unit
t_s	SCLKclock cycle		4		tosccycle
t_{spw}	SCLKPulse width, high level and low level		200		ns
t_{cs1}	Chip select signalCSfalling edge with the firstSCLKedge setup time		0		ns
t_{ds}	SDIData creation time (withSCLKDelay)		50		ns
t_{dsh}	efficientSDIdata retention time		50		ns
t_{dio}	When issuing the following commandSDIthe last ofSCLKclock edge withSDO the firstSCLKClock edge: RDATA, RDATAC, RREG, WREG		50		tosccycle
t_{dso}	SDOoutput data withSCLKdelay time			50	ns
t_{dsoh}	SDOdata retention time		0		
t_{dsot}	SDObecomes tri-stated withSCLKclock edge delay		6	10	tosccycle
t_{cs2}	Chip select signalCShold low time with the lastSCLKclock edge		0		ns
t_{sdelay}	the last of the current command indivualSCLKclock edge to the first of the next instruction indivualSCLKClock edge:	RREG, WREG, SYNC, SLEEP, RDATA, RDATAC, STOPC	4		tosccycle
		GCALSELF, SELFOCA, OCALSYS, GCALSYS	8		DRDYcycle
		CALSELF	15		DRDYcycle
		RESET(or viaSCLKor RSTpin out $\overline{\text{RESE}}$Tinstruction)	16		tosccycle
t_5	Pulse Width		4		tosccycle
t_6	Allowable analog input signal change to the next valid conversion			5000	tosccycle
t_7	DORrenew,DORinvalid		4		tosccycle
t_8	DRDYAfter the signal goes low the firstSCLKclock	RDATACmodel	10		tosccycle
		other modes	0		tosccycle

3Function Module Description

3.1Input multiplexer (Input Multiplexer)

CS1243The input signal channels can be combined arbitrarily, and the schematic diagram of multi-input selection is shown in the figure.4shown.



picture4Block diagram of multiple input selection

CS1243Can be configured up to4for differential inputs or7single-ended input. For example, if you chooseAIN1is differential positive (negative) signal

One input terminal of the number, and any other input terminal can be selected as the negative (positive) terminal input.

CS1243It can realize the selection and switching of the input signal and the stable output of the internal digital filter within a single clock cycle. for

To reduce switching error, it is required toDRDYConfigured as soon as the signal goes lowMUXregister.

3.2Input analog buffer (Buffer)

When the analog input buffer is not enabled (Buffer), the input impedance is approximately6M--PGA. When the system requires higher input impedance

, the analog input buffer can be enabled, and the input impedance can be increased to about5G-.

The buffer enable signal can be set byBUFpin or internal registerACRcontrol. When the input pinBUFis high orACRsend

storedBUFWhen high, the input buffer is enabled, effectively increasing the input impedance.

If the buffer is enabled, the chip adds additional power consumption. The size of the power consumption andPGAis related to the gain,PGA=1

, increase by approx.50uAcurrent, whilePGA=128, the increased current is150uA.

When the buffer is turned on, the range of the input signal is required. At this time, the range of the input signal is required to beAGND+0.3V~

AVDD-1.5V.

3.3Programmable Gain Amplifier (PGA)

The internal voltage gain amplifier can be programmed with a gain of1,2,4,8,16,32,64,128. by usingPGA

The effective conversion precision can be improved. E.g,PGA=1,5VFull-scale analog-to-digital conversion, the effective identification voltage is1uV,but if

PGA=128,39mVDuring full-scale analog-to-digital conversion, the minimum can be identified75nVInput voltage.

3.4Modulator(Modulator)

CS1243The modulator is a single loopback,2Order --- Modulator, the sampling frequency of the modulator can be passed throughSPEED(ACRregisterbit 5

) control, as shown in the following table:

surface7Modulator Sampling Frequency Table

Crystal frequency (MHz)	SPEED	ADCSampling frequency (KHz)	Data output rate (Hz)			Notch frequency (Hz)
			DR=00	DR=01	DR=10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

3.5Error correction (Calibration)

Chip calibration is divided into self-calibration and external system calibration. The calibration includes analog-to-digital converter offset error correction (OCAL), analog-to-digital conversion

Converter gain correction (GCAL). While calibrating,DRDYmaintained high, indicating that nowADThe result of the conversion is not available.

After the chip is powered on again, the external ambient temperature changes, the gain (PGA) is changed to perform error correction to ensure that the analog-to-digital conversion is correct.

Exactly. After calibrationDRDYpin goes low, i.e.DRDYWhen the output is low, it means that the chip has completed the calibration.Calibration completed

After the first output data is incorrect due to the delay of the internal circuit operation, it cannot be used as normal analog-to-digital conversion data.. second

The conversion output data is normal and can be used.

3.5.1 self-calibration (Self Calibration)

CS1243self-calibration throughCALSELF,GCALSELF,OCALSELFThree instructions to control completion. implement

CALSELFcommand, offset error correction can be done simultaneously (Offset Calibration) and gain error correction (Gain

Calibration).GCALSELFThe command only controls the chip to complete the gain correction, whileOCALSELFThen the control chip completes the bias

shift correction. Gain correction, offset correction are in8indivualTDATAcycle(ADcycle) is completed,TDATAperiod is output

The inverse of the data rate. If you executeSEFLCALcommand, you need15indivualTDATAcycle.

During self-calibration,CS1243Automatically disconnect the external input signal and connect the internal voltage. When performing gain error correction,CS1243

automatic firstPGAset as1, after performing gain error correctionCS1243willPGAThe value reverts to the user-set

value. However, during the execution of offset error correction,PGAsettings have not changed.(Note that if calibration is done externally

reference voltage higher thanAVDD-1.5V, the input analog buffer must be turned off.)

3.5.2 System calibration (System Calibration)

System calibration can correct the offset error and gain error inside the chip and the system, and the calibration must require the correct input signal carried out later. System calibration instructions includeOCALSYS,GCALSYS,inOCALSYSPerform offset error correction, GCALSYSPerform gain error correction, offset error correction and gain error correction respectively in8indivualTDADAwithin the data cycle Finish.

During offset error correction (OCALSYS)Time,must require the input to be a differential voltage of0,CS1243calculated for the system offset error value and writeOCCregister,CS1243This is offset by internal calculations during normal conversions.

While performing gain error correction (SYSGCAL)Time,Positive full-scale voltage must be entered,CS1243Calculate the gain of the system error and writeGCCregister,CS1243This is offset by internal calculations during normal conversions.

3.6External reference voltage (External Voltage Reference)

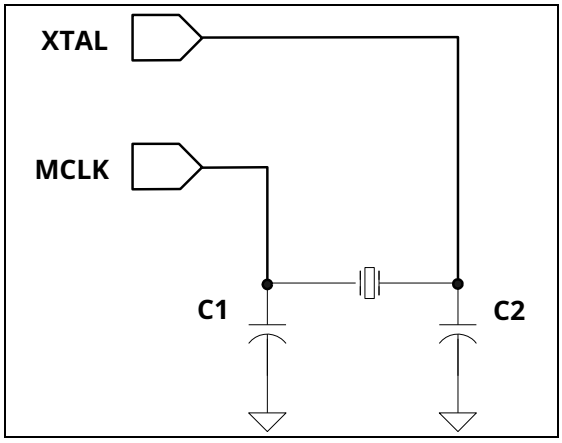
CS1243An external reference voltage is required, and the specific value is passed throughACRregister configuration. The reference voltage is connected toREFPandREFNOn the pins, the voltage cannot exceed the power supply voltage of the chip. The specific voltage values are as follows:

surface8external reference voltage andRANrelation table

RAN(ACR.2)	voltage(V)	Reference differential voltage (V)	Remark
0	5	<=2.5	
1	5	<=5	
0	3.0	<=1.25	
1	3.0	<=2.5	

3.7clock unit (Clock Unit)

CS1243An external crystal, oscillator or clock can be connected. If connected to an external clock, thenMCLKpin input, this timeXTAL dangling. If an external crystal is connected, the circuit requirements are as follows: (required inMCLKandXTALconnected to the pins at the same time10~20pFof capacitance)



picture5External crystal oscillator connection diagram

3.8digital filter (FIR)

CS1243with a programmableFIRfilter.FIRFilters can be configured for different output rates. when using 2.4576Mthe clock,CS1243The rate of output data can be configured as15Hz,7.5Hzor3.75Hz. this hour,FIRThe filter can simultaneously50Hzand60HzThe clutter signal is notch filtered.

If other output data rates are desired, other clock frequencies must be used. At this time, the notch frequency is also changed at the same time. changed. For example, when using the default register configuration, the clock frequency is3.6864Mwhen:

The output data frequency is:

(3.6864MHz/2.4576MHz) × 15Hz = 22.5Hz

The notch frequency is:

(3.6864MHz/2.4576MHz) × (50Hzand60Hz)= (75Hzand90Hz)

3.9Serial bus interface (SPI)

SCLKis a Schmitt trigger, used toSDIandSDOThe signal is sampled. To prevent wrong sampling data,SCLKmust Must be very clean. if in3indivualDRDYno periodSCLKthe clock appears, then in the nextSCLKadvent hour,SPIThe bus will be reset and the next communication cycle will begin.SCLKon a specific waveform can reset the entire chip. For specific information, please refer to**RESET**chapter

3.9.1 Chip select signal (CS)

in withCS1243Before communication, the external controller must sendCSChip select signal. During the entire communication period,CSThe signal must be held low. whenCSAfter the signal goes high, the entireSPIThe bus will be reset.CSThe signal can also be tied normally low. when CSsignal is pulled normally low,SPIThe bus can work in three-wire mode.

3.9.2 serial clock (SCLK)

SCLKis a Schmitt trigger, used toSDIandSDOThe signal is sampled. To prevent wrong sampling data,SCLKMust be very clean. if in3indivualDRDYno periodSCLKthe clock appears, then in the nextSCLKwhen it comes,SPIThe bus will be reset and the next communication cycle will begin.SCLKA specific waveform on can reset the entire chip. For specific information, please refer to**RESET**chapter

3.9.3 Clock Polarity Control (POL)

POLcontrolled serial clockSCLKpolarity. whenPOLis low, the data is inSCLKThe falling edge of is sampled. if not There is a clock pulse, thenSCLKshould be kept low. whenPOLWhen high, the data is inSCLKThe rising edge of is sampled as If there is no clock pulse,SCLKshould remain high.

3.9.4 data input(SDI)and data output (SDO)

SDIandSDOThe pins are used to input and output data, respectively. When not in use,SDOis high impedance, which allows the SDIandSDOconnected together and drive it through a bidirectional bus. It should be noted that this case is not suitable for TowardsCS1243issueRDATACinstruction. becauseRDATACcommand needs to useSTOPCinstruction orRESETcommand to end end. while inRDATACIn mode, this bidirectional bus will always be occupied to send data to the outside, so it cannot be used at this time. via the bus toCS1243sendSTOPCinstruction orRESETinstruction, so it cannot be terminatedRDATACstatus, except not at this timeSDOThe data sent containsSTOPCorRESETinstruction. at this timeSDIwill detectSTOPCor RESETinstruction, which terminatesRDATACstate.

3.10data ready (DRDY)

DRDYSignals are used to indicate the state of the internal data registers. When the internal data registerDORReady for new data within hour,DRDYThe signal will go low. When executing a slave internal data registerDORAfter a read operation to read data,DRDY

The signal will go high. existDORWhen register data is ready to be updatedDRDYThe signal will also go high, indicating that at this timeDORregister data within is not available, preventing theDORregisters are updated fromDORRead data in the register.

DRDYThe signal can also be obtained fromACRregisterbit 7to obtain.

3.11data synchronization(SYNC)

CS1243able to passSYNCpin orSYNCcommand to synchronize data. when usingSYNCpin for data with step, the digital circuit will be inSYNCreset on the falling edge. whenSYNCAfter going low, the serial interface is in an inactive state. whenSYNCAfter going high, the digital circuit will change fromRESETout of state, on the subsequent rising edge of the system clock, the data will be synchronized.

when usingSYNCWhen the instruction performs data synchronization, the digital filter isSYNClast commandSCLKedge of the clock is reset, the modulator will be inRESETstate until the nextSCLKThe clock edge is detected. existSYNCafter the first OneSCLKWithin the rising edge of the system clock, the data will be synchronized.

3.12Power-on reset and chip reset (RESET)

There are three ways toCS1243To reset: put$\overline{RST}$pin is pulled low, sending$\overline{RESET}$instruction, inSCLKsend on specific waveform (SCLK $\overline{RESET}$waveform, referenceCS1243timing diagram).

4 CS1243register description

CS1243The working mode is configured through a series of control registers, which include data format, multiplexing signal output input, analog-to-digital conversion data output rate, correction control, etc.

4.1register list

surface9Detailed List of Internal Registers

address(h)	register	the first7bit	the first6bit	the first5bit	the first4bit	the first3bit	the first2bit	the first1bit	the first0bit
00	SETUP	ID3	ID2	ID1	ID0	reserve	PGA2	PGA1	PGA0
01	MUX	PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0
02	ACR	$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUF	BITOR	RAN	DR1	DR0
03	ODAC	reserve	reserve	ISET1	ISET0	reserve	reserve	reserve	reserve
04	reserve								
05	reserve								
06	reserve								
07	OCC0	OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
08	OCC1	OCC17	OCC16	OCC15	OCC14	OCC13	OCC12	OCC11	OCC10
09	OCC2	OCC27	OCC26	OCC25	OCC24	OCC23	OCC22	OCC21	OCC20
0A	GCC0	GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
0B	GCC1	GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
0C	GCC2	GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
0D	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0E	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0F	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

4.2Register Details

SETUPregister(address=00H, reset value =xxxx0000)PGAcontrol(SETUP REGISTER)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	reserve	PGA2	PGA1	PGA0

SETUP. 7-4 :chipIDnumber, for manufacturer use

SETUP.3 :reserve

SETU.2-0 :PGA2/PGA1/PGA0, programmable gain amplifier gain selection (Programmable Gain Amplifier Gain Selection)

000=1(Defaults);
001=2
010=4
011=8
100=16
101=32
110=64
111=128

MUXregister(address=01H, reset value =01H) input channel selection (Multiplerxer Control Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS3	PS2	PS1	PS0	NS3	NS2	NS1	NS0

SETUP. 7-4 : PS3~0, positive input channel selection (Positive Channel Selection)

0000=ADIN0(Defaults)
0001=ADIN1
0010=ADIN2
0011=ADIN3
0100=ADIN4
0101=ADIN5
0110=ADIN6
0111=ADIN7
rest = reserved (Reserved)

SETUP.3-0 : NS3~0, negative input channel selection (Negative Channel Selection)

0000=ADIN0
0001=ADIN1(Defaults)
0010=ADIN2
0011=ADIN3
0100=ADIN4
0101=ADIN5
0110=ADIN6
0111=ADIN7
rest = reserved (Reserved)

ACRregister(address=02H, reset value =x0H) analog circuit control (Analog Control Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{DRDY}$	U/$\overline{B}$	SPEED	BUF	BITOR	RAN	DR1	DR0

SETUP.7 : $\overline{DRDY}$, the data is ready (Data Ready, read only), with output pins$\overline{DRDY}$the same value;

SETUP.6 : U/$\overline{B}$,Data Format(Data Format)
0= bipolar (default);
+FSRoutput0x7FFFFFH,ZERO=0x00000H, -FSR=0x800000H; 1= unipolar;
+FSRoutput0xFFFFFFH,ZERO=0x00000H, -FSR=0x000000H;

SETUP.5 : SPEED, the analog-to-digital converter sampling frequency control (Modulator Clock Speed)
0=fosc/128(Defaults); 1= fosc/256;

SETUP.4 : BUF, the input buffer is enabled (Buffer Enable)
0= disable (default);
1= enable;

SETUP.3 : BITOR,Output Databitorder
0 =Big order first (default)
1 =low first

SETUP.2 : RAN, conversion range selection (Select)
0= full scale input (Full Scale) is +/-V_{REF}(Defaults); 1= full scale input (Full Scale) is +/-V_{REF}/2;

SETUP.1-0 : DR1/DR0, the data output rate (Data Rate)
00=15Hz(Defaults); 01= 7.5Hz;
10=3.75Hz;
11=reserve(Reserved)

ODACregister(address=03H, reset value =00H)Offset DACset up

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
invalid	invalid	ISEL1	ISET0	invalid	invalid	invalid	reserve

ISET11-0: Analog circuit bias current selection,
00= Bias current is10uA(Defaults) 01or10= Bias current increases25%, 11= Bias current increases50%, when using higher clock frequencies, increasing the analog circuit bias current helps to increase theCS1243performance.

OCC0register(address=07H, reset value =00H), the offset error coefficient (Offset Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23Yes MSB, OCC00YesLSB) to correct the offset error.							

OCC1register(address=08H, reset value =00H) offset error positive coefficient (Offset Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23Yes MSB, OCC00YesLSB) to correct the offset error.							

OCC2register(address=09H, reset value =00H) offset error correction factor (Offset Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16
OCC0andOCC1andOCC2Composition offset error correction factorOCC23~0(commontwenty fourbit,OCC23Yes MSB, OCC00YesLSB) to correct the offset error.							

GCC0register(address=0AH, reset value =00H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23 YesMSB, GCC00YesLSB) to correct the gain error.							

GCC1register(address=0BH, reset value =00H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23 YesMSB, GCC00YesLSB) to correct the gain error.							

GCC2register(address=0CH, reset value =00H) gain error correction coefficient (Gain Calibration Coefficient)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
GCC0andGCC1andGCC2Composition offset error correction factorGCC23~0(commontwenty fourbit,GCC23 YesMSB, GCC00YesLSB) to correct the gain error.							

DOR2register(address=0D$_H$, reset value =00$_H$) analog-to-digital data (Data Output Register)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR 23	DOR22	DOR 21	DOR 20	DOR 19	DOR 18	DOR 17	DOR 16
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB, DOR00 YesLSB).							

DOR1register(address=0E$_H$, reset value =00$_H$) analog-to-digital data (Data Output Register)

MSB							**LSB**
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB, DOR00 YesLSB).							

DOR0register(address=0F$_H$, reset value =00$_H$) analog-to-digital data (Data Output Register)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00
DOR 0andDOR 1andDOR 2Compose analog-to-digital dataDOR23~0(commontwenty fourbit,DOR23YesMSB, DOR00 YesLSB).							

5 CS1243Instruction description

CS1243The working mode is configured through a series of control registers, which include data format, multiplexing signal output input, analog-to-digital conversion data output rate, correction control, etc.

Operands:

n =quantity(0arrive127)

r =register (0arrive15)

x =any value

5.1command list

surface10 CS1243Instruction description table

instruction	describe	opcode	operand
RDATA	fromDORread data from register	0000 0001 (01H)	- -
RDATAC	fromDORContinuously read data from registers	0000 0011 (03H)	- -
STOPC	stop fromDORContinuously read data from registers	0000 1111 (0FH)	- -
RREG	read register"rrrr”the value of	0001 rrrr (1XH)	xxxx_nnnn
WREG	write data to the register"rrrr”middle	0101 rrrr (5XH)	xxxx_nnnn
CALSELF	Corrects for chip offset and gain errors	1111 0000 (F0H)	
OCALSELF	Correct the offset error of the chip	1111 0001 (F1H)	
GCALSELF	Correct the gain error of the chip	1111 0010 (F2H)	
OCALSYS	Correct the offset error of the system	1111 0011 (F3H)	
GCALSYS	Correct the gain error of the system	1111 0100 (F4H)	
SYNC	rightDRDYto synchronize	1111 1100 (FCH)	
RESET	Reset the chip to the state after power up	1111 1110 (FEH)	
Note: When receiving data, the high-order bits are always first. The format of the sent data is given byACRregisterBITORDERbit to decide			

5.2Instruction details

RDATA- read data

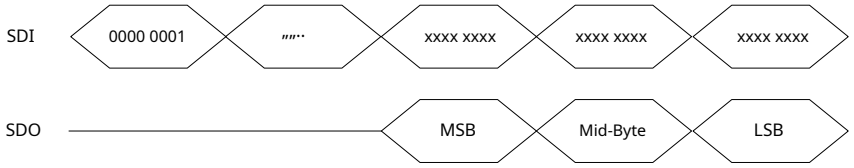
describe:fromDORThe latest read from the registerADThe converted value, this value is24bit

Operands:none

byte: 1

coding: 0000 0001

Data transfer sequence:



RDATAC- Continuous read data command

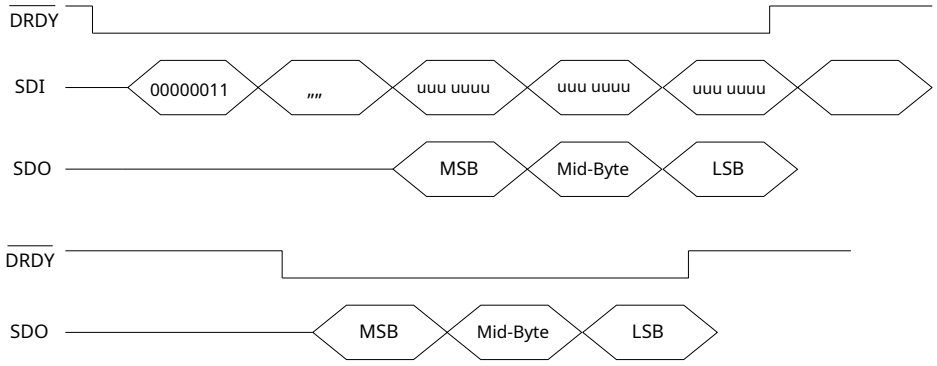
describe:RDATACallowed in eachDRDYContinuously from the signal periodDORThe register is read every timeADthe result of the conversion. This command does not need to be executed every timeDRDYSent when the signal goes lowRDATAinstruction. can be sent bySTOPCinstruction orRESET instruction to terminate the execution of this instruction. existDRDYAfter the signal goes low, wait at least until10indivualfosccycle to execute this instruction.

Operands:none

byte: 1

coding: 0000 0011

Data transfer sequence:



STOPC- Stop continuous read data command

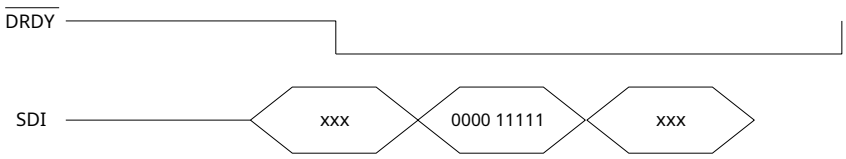
describe: Stop continuous read data mode. need inDRDYEmitted when the signal goes low.

Operands:none

byte: 1

coding: 0000 1111

Data transfer sequence:



RREG- read the value of the register

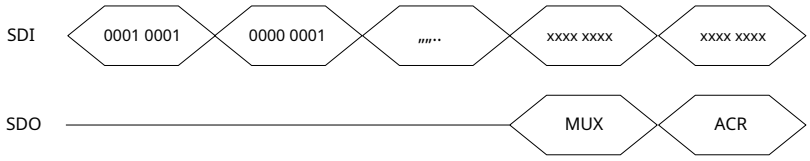
describe: output the most16value of a register. The address of the first register is determined by the first operand of the instruction. read sent The number of registers is added by the value of the second operand of the instruction1Decide. If this value exceeds the remaining register's number, the address of the register goes to the first register.

Operands:r, n

byte: 2

coding: 0001 rrrr xxxx nnnn

Data transfer sequence: Read the value of two registers, the address of the first register is01_H(MUX)



WREG- write data to the register

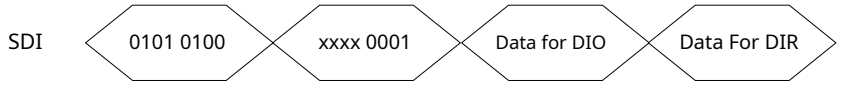
describe: Write data to multiple registers. The address of the first register is determined by the first operand of the instruction. read register The number of registers is added by the value of the second operand of the instruction1Decide.

Operands:r, n

byte: 2

coding: 0101 rrrr xxxx nnnn

Data transfer sequence: Write data into two registers, the address of the first register is04_H(DIO)



CALSELF- Self-correction of offset error and gain error

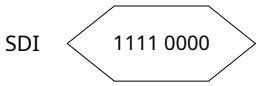
describe: Self-correct the chip. After doing this,OCCregister andGCCThe value of the register will be updated.

Operands:none

byte: 1

coding: 1111 0000

Data transfer sequence:



OCALSELF- Self-correction of offset errors

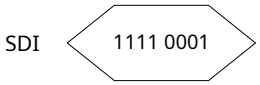
describe: Offset error self-correction for the chip. After doing this,OCCThe value of the register will be updated. **Operands:**

none

byte: 1

coding: 1111 0001

Data transfer sequence:



GCALSELF- Self-correction of gain error

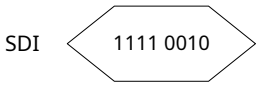
describe: Gain error self-correction for the chip. After doing this,GCCThe value of the register will be updated.

Operands:none

byte: 1

coding: 1111 0010

Data transfer sequence:



OCALSYS- Correct the offset error of the system

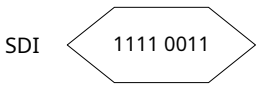
describe: Correct the offset error of the system. At this time, the input signal of the system should be0,CS1243Calculate OCCThe value of , compensates for the offset error. After doing this,OCCThe value of the register will be updated. use user must input the correct analog input0SignalOCCThe registers are automatically updated.

Operands:none

byte: 1

coding: 1111 0011

Data transfer sequence:



GCALSYS- Correct the gain error of the system

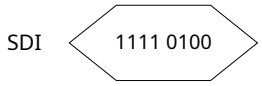
describe: Correct the gain error of the system. At this time, the input signal of the system should be a full-scale voltage,CS1243calculate outGCCThe value of , compensates for the gain error. After doing this,OCCThe value of the register will be updated. The user must input the full scale signal on the correct analog input.GCCThe registers are automatically updated.

Operands:none

byte: 1

coding: 1111 0100

Data transfer sequence:



SYNC-rightDRDYsignal to synchronize

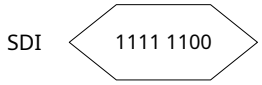
describe: SynchronizeCS1243The data

Operands:none

byte: 1

coding: 1111 1100

Data transfer sequence:



RESET- Reset the chip to the default state

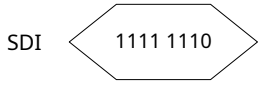
describe: Resets all register values to their state after power-up. This command can terminateRDATACinstruction

Operands:none

byte: 1

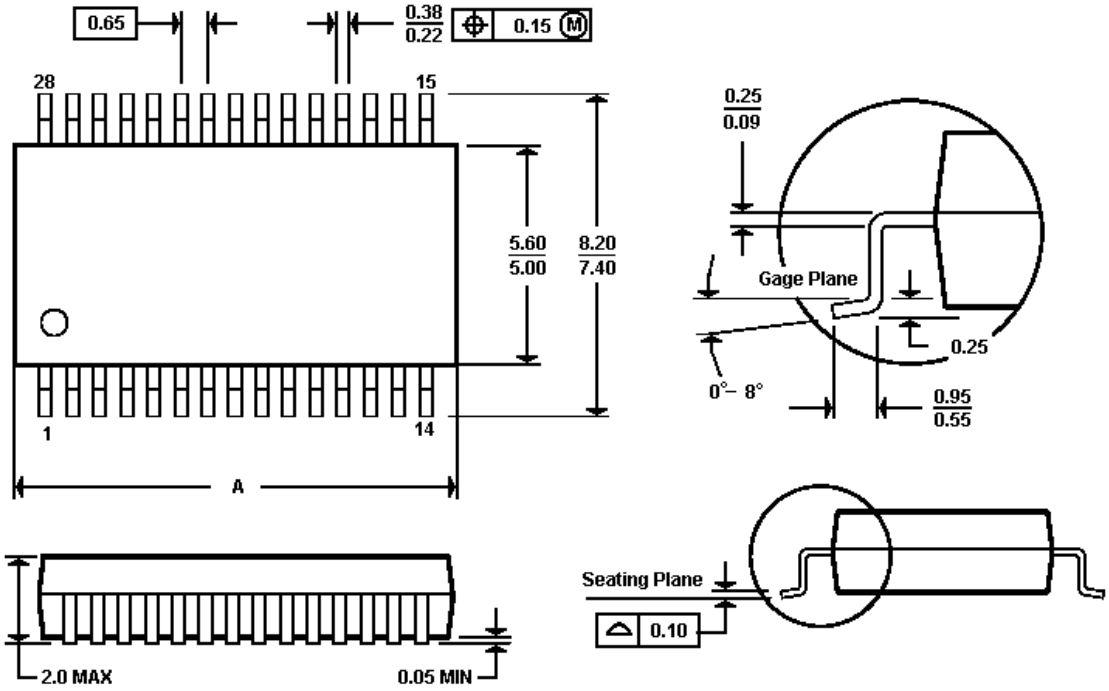
coding: 1111 1110

Data transfer sequence:



6 Chip packaging

CS1243useSSOP-28package as shown.



NOTES :

A. All linear dimensions are in millimeters
B. This drawing is subject to change without notice
C. Body demensions do not include mold flash or protrusion nont to exceed 0.15
D. Falls within JEDEC MO-150

A MAX	10.50
A MIN	9.90

picture6chipSSOP-28Size Information