High Frequency PWM Controller With Short Circuit Restart

Halogen Free

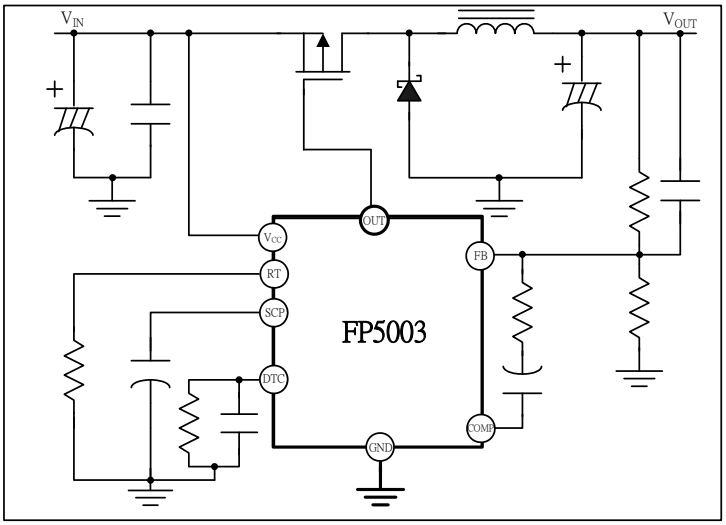
General Description

The FP5003, a high performance monolithic IC, includes adjustable frequency oscillator, error amplifier for pulse width modulation (PWM) control, 1.0V precision voltage reference, under-voltage lockout circuit (UVLO), variable pulse duty control (DTC) circuit and programmable auto-restart timer for short circuit shutdown protection (SCSAR). Built-in totem-pole transistors pair drives MOS directly at high frequency operation with high efficiency. It is very easy to design a DC-DC converter using a few external components. The typical application example is shown below:

Features

- Wide Operating Voltage Range:3.6~30V
- Reference Voltage Precision: ±2%
- Output Source / Sink Current up to 100mA
- Totem-Pole Output for MOS Drive
- Oscillator Frequency:Max.1.5MHz
- Variable Duty Control (DTC)
- Under Voltage Lockout Protection Function (UVLO)
- Short Circuit Shutdown Protection / Auto Re-start Function (SCSAR)
- Package:SOP-8L / MSOP-8L / SOP-8L (EP)

Typical Application Circuit



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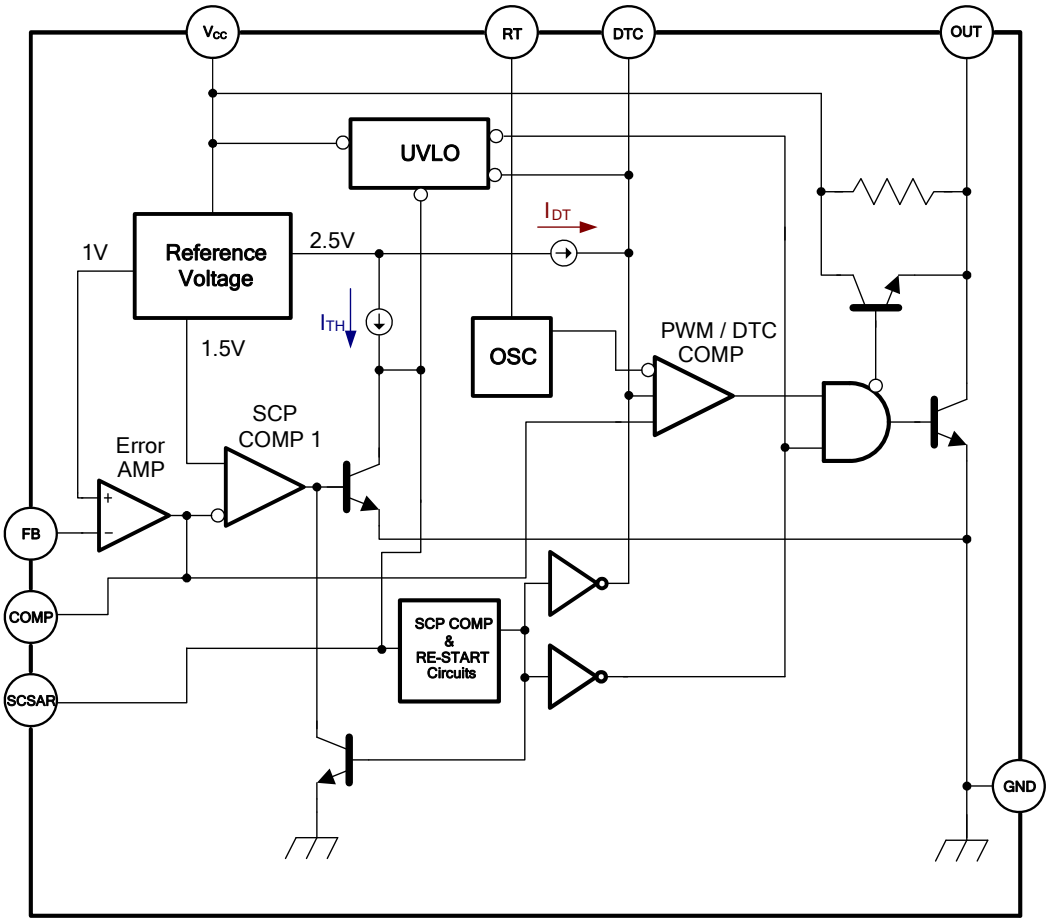
Function Block Diagram



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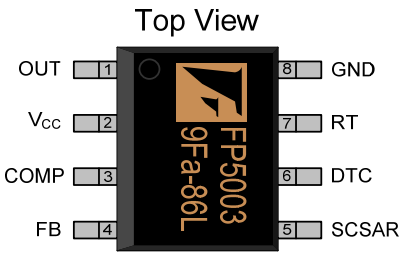
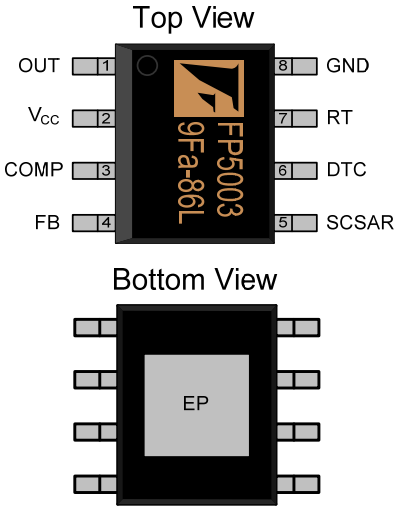
Pin Descriptions

SOP-8L



Name	No.	I / O	Description
OUT	1	O	Totem-pole Transistor Pair Output
V_{CC}	2	P	IC Power Supply
COMP	3	O	Error Amplifier Feedback Output
FB	4	I	Error Amplifier Inverting Input
SCSAR	5	I	Short Circuit Protection Input
DTC	6	I	Duty Control Input
RT	7	I	Frequency Adjustment. Connect a Resistor Between This Pin and GND to Adjust PWM Frequency
GND	8	P	IC Ground

SOP-8L (EP)



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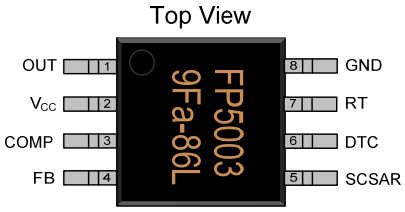
FB	4	I	Error Amplifier Inverting Input
SCSAR	5	I	Short Circuit Protection Input
DTC	6	I	Dead-Time Control Input
RT	7	I	Frequency Adjustment. Connect a Resistor Between This Pin and GND to Adjust PWM Frequency
GND	8	P	IC Ground
EP	9	P	Exposed PAD. Must connect to GND

MSOP-8L



Name	No.	I / O	Description
OUT	1	O	Totem-pole Transistor Pair Output
V_{CC}	2	P	IC Power Supply
COMP	3	O	Error Amplifier Feedback Output
FB	4	I	Error Amplifier Inverting Input
SCSAR	5	I	Short Circuit Protection Input
DTC	6	I	Dead-Time Control Input
RT	7	I	Frequency Adjustment. Connect a Resistor Between This Pin and GND to Adjust PWM Frequency
GND	8	P	IC Ground

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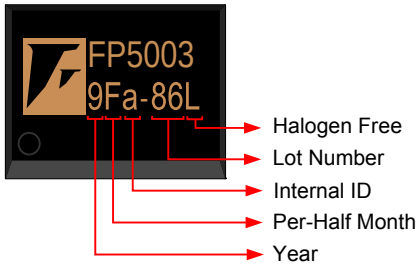
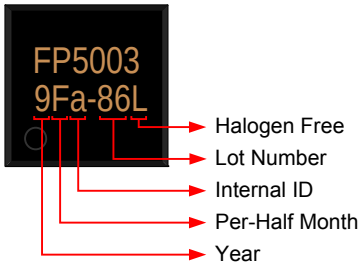
Marking Information

SOP-8L & SOP-8L (EP)



MSOP-8L



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code n

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D(Last Half Month)

Year: Production year's last digit

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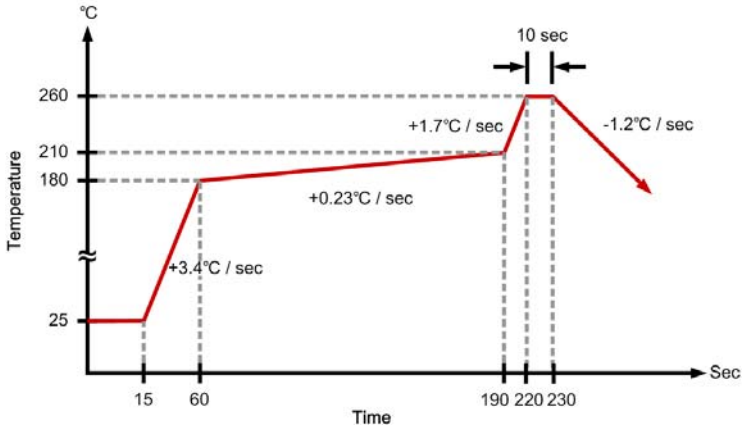
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5003DR-LF	-20°C ~ +105°C	SOP-8L	2500EA	Tape & Reel
FP5003XR-LF	-20°C ~ +105°C	SOP-8L (EP)	2500EA	Tape & Reel
FP5003TR-LF	-20°C ~ +105°C	MSOP-8L	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				30	V
Output Voltage	V_o				30	V
Source / Sink Output Current	I_O				±150	mA
Junction Temperature	T_j				+150	℃
Allowable Dissipation		SOP-8L ($T_A \leq 25℃$)			570	mW
		SOP-8L (EP) ($T_A \leq 25℃$)			600	mW
		MSOP-8L ($T_A \leq 25℃$)			400	mW
Thermal Resistance	T_{JA}	SOP-8L			+130	℃ / W
	T_{JC}				+38.8	℃ / W
Thermal Resistance	T_{JA}	SOP-8L (EP)			+120	℃ / W
	T_{JC}				+38.8	℃ / W
Thermal Resistance	T_{JA}	MSOP-8L			+260	℃ / W
	T_{JC}				+60	℃ / W
Operating Temperature Range			-20		+105	℃
Storage Temperature Range			-65		+150	℃
Lead Temperature (soldering, 10 sec)					+260	℃

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		3.6		30	V
Operating Temperature			-20		+105	°C

DC Electrical Characteristics (V_{CC}= 6V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference						
Output Voltage	V_{REF}	COMP Connected to FB	0.98	1	1.02	V
Input Regulation	$\triangle V_{REF}$	V_{CC} = 3.6 V to 30 V		2	12.5	mV
Output Voltage Change with Temperature	$\triangle V_{REF}$ / V_{REF}	T_A = -20°C to 25°C	-10	-1	15	mV / V
		T_A = 25°C to 85°C	-10	-2	10	mV / V
Under Voltage Lockout						
Upper Threshold Voltage	V_{UPPER}			3		V
Lower Threshold Voltage	V_{LOW}			2.8		V
Hysteresis	V_{HYS}		100	200		mV
Short-Circuit Protection						
SCP Standby Voltage	V_{SB}	V_{COMP} < 1.5V		0.2		V
SCP Threshold Voltage	V_{TH}	V_{COMP} > 1.5V		0.7		V
SCP re-start Charge Current	I_{RSC}	V_{COMP} > 1.5V		20		μA
SCP re-start / Hold Time	T_{RS} / T_{HOLD}	V_{COMP} > 1.5V		1 / 32		Ratio
SCP Comparator 1 Threshold Voltage	$V_{COMP\ (TH)}$			1.5		V
Oscillator						
Frequency	f	R_T = 100K		260		KHz
Standard Deviation of Frequency	$\triangle f$			15		KHz
Frequency Change with Voltage	$\triangle f$ / $\triangle V$	V_{CC} = 3.6V to 30V		1		KHz
Frequency Change with Temperature	$\triangle f$ / $\triangle T$	T_A = -20°C to 25°C		±1		%
		T_A = 25°C to 105°C		±1		%
Voltage at RT	V_{RT}			1		V

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DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Duty-time Control						
Output (Source) Current	I_{SOURCE}	$V_{(DT)}$=1.5V	0.9×I_{RT}		1.2×I_{RT}	V
Input Threshold Voltage	V_{TH}	Duty Cycle=0%	0.5	0.7		V
		Duty Cycle=100%		1.3	1.5	V
Error Amplifier						
Input Voltage	V_{IN}	V_{CC} = 3.6V to 30V	0		1.5	V
Input Bias Current	I_{BIAS}			-160	-500	nA
Output Voltage Swing Positive	V_{POS}		1.5	2.3		V
Output Voltage Swing Negative	V_{NEG}			0.3	0.4	V
Open-loop Voltage Amplification	A_{VO}			80		dB
Unity-Gain Bandwidth	BW_U			1.5		MHz
Output (Sink) Current	I_{SINK}	$V_{I(FB)}$ = 1.2V, COMP = 1V	600	800		µA
Output (Source) Current	I_{SOURCE}	$V_{I(FB)}$ = 0.8V, COMP = 1V	-100	-150		µA
Output						
Output Low Voltage	V_{OL}	Io=100mA		1.7		V
Output High Voltage	V_{OH}	Io=100mA		4.4		V
Total Device						
Standby Supply Current Off State	$I_{STANDBY}$			3.5	4.0	mA
Average Supply Current	I_{AVE}	R_T = 100k		3.8	5	mA

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Typical Characteristics

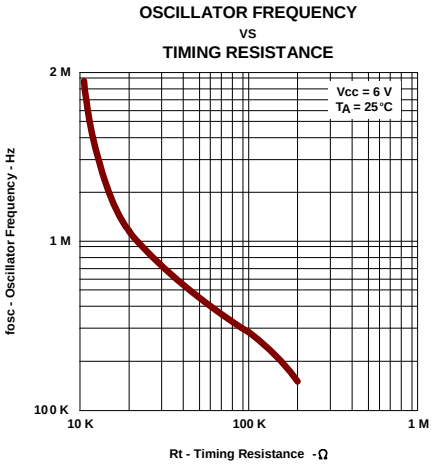

Figure 1

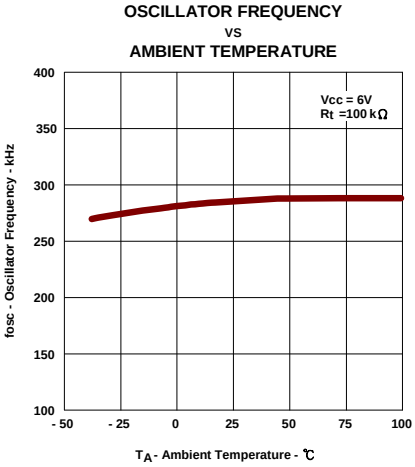

Figure 2

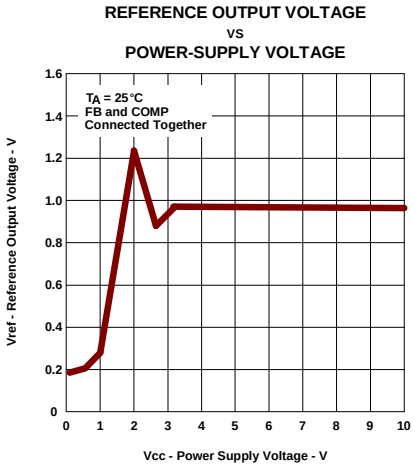

Figure 3

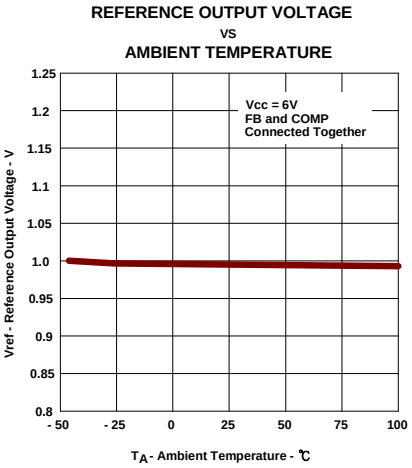

Figure 4

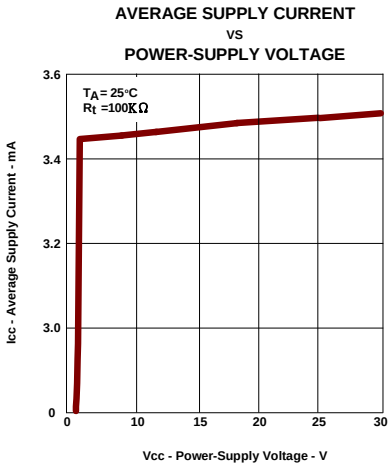

Figure 5

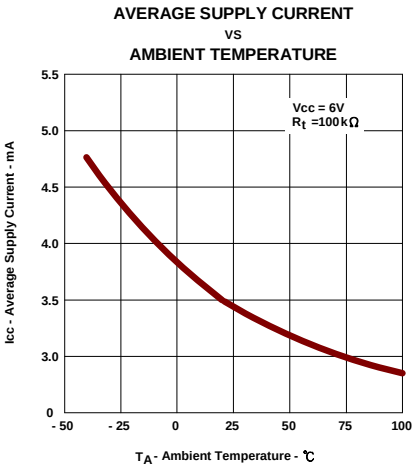

Figure 6

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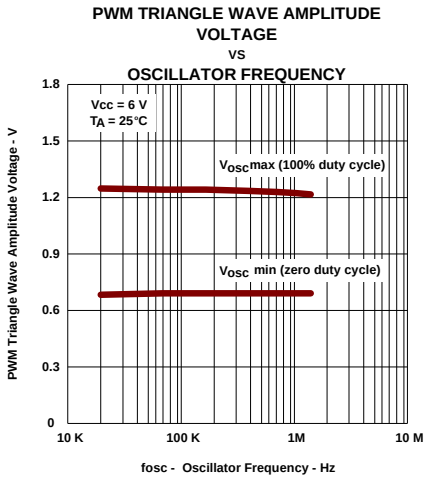

Figure 7

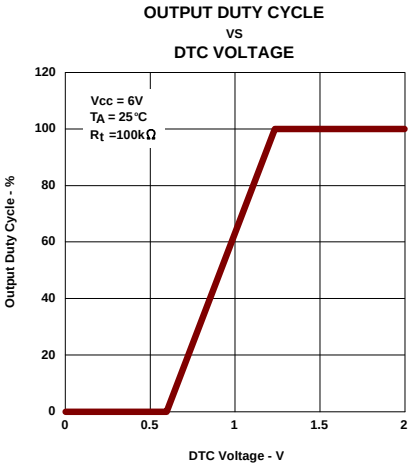

Figure 8

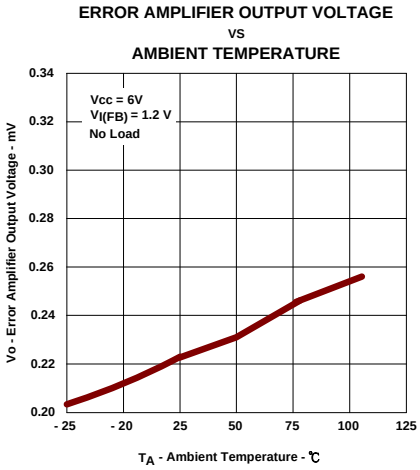

Figure 9

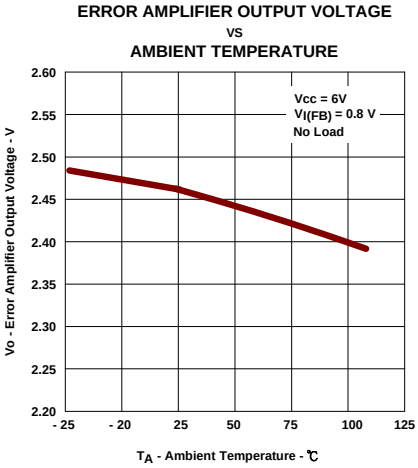

Figure 10

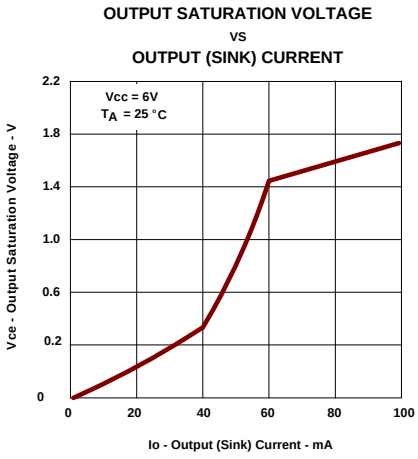

Figure 11

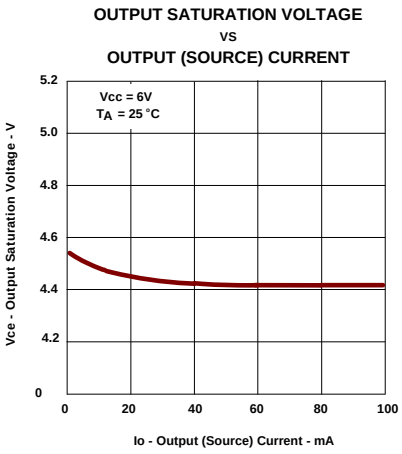

Figure 12

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Function Description

Voltage Reference

The FP5003 includes a 2.5V reference regulator to supply its own internal circuits. Also, a resistive divider is included to divide the 2.5V reference voltage to 1.0V as the precision reference voltage for the error amplifier's non-inverting terminal and SCP comparator's 1.0V threshold voltage.

Error Amplifier

The error amplifier compares the feedback voltage, divided from DC-DC converter output, with the 1.0V reference and generates the error signal for the PWM comparator. The relation between V_{OUT} and V_{REF} are shown below (see Figure 13).

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{REF}$$

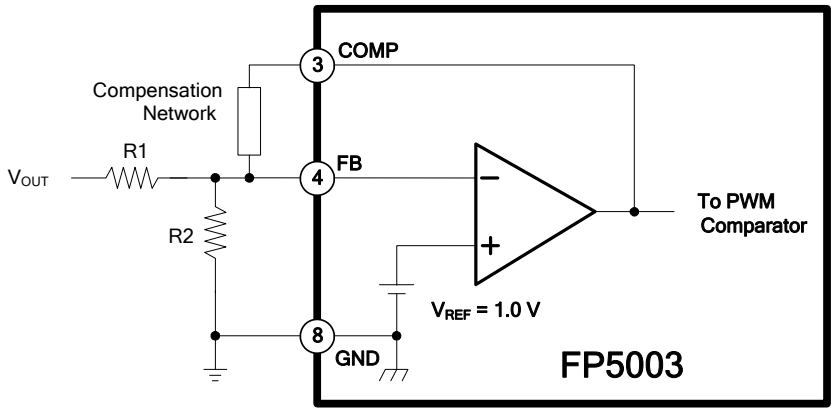

Figure 13. Error Amplifier with Converter Feedback Resistors

Note:

It is necessary to check the converter total open loop gain and phase shift from Bode plot before compensation network adjustment. Finally, let the system works stability.

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Oscillator / PWM Comparator

The oscillator frequency (fosc) can be adjusted from 20KHz to 1.5MHz by the resistor connected to R_T pin. The relation between the oscillator frequency and R_T value can be determined by the graph shown in Figure 1.

The internal oscillator output is a triangular waveform. Its minimum and maximum voltage levels are approximately 0.7V and 1.3V respectively (see Figure 14). The PWM comparator compares the triangular waveform with the signals from output voltage of error-amplifier and the DTC voltage. The PWM comparator output controls the output stage of totem-pole transistors pair off or on whenever the triangular wave is greater than the both input signals or less.

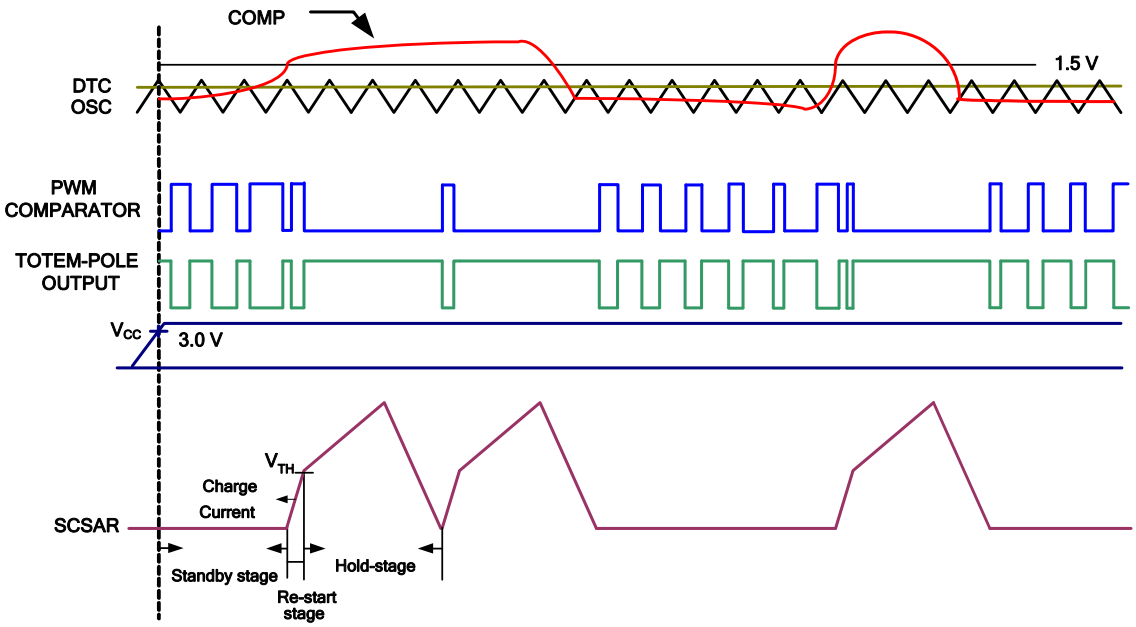

Figure 14. PWM Timing Diagram

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Duty Control (DTC)

DTC main function is to limit PWM duty cycle to less than 100%. The source current of duty control current I_{DT} at DTC pin is the same as the one of R_T. The source current I_{DT} flows through a resistor R_{DT}, connecting between DTC pin and GND, generating a bias voltage V_{DT}. This V_{DT} voltage is further compared with the output waveform of oscillator in the PWM comparator. The PWM duty cycle begins from 0% when V_{DT} sets at 0.7V or less, and 100% when V_{DT} sets at 1.3V or greater. Engineer can choose a resistor R_{DT} for a specific limitation of PWM duty cycle D. According to the following equation, we can choose a R_{DT} for a maximum duty cycle.

$$R_{DT} = (R_T + 1250) \times (0.6 \times D + 0.7)$$

For example:

R_T is 33KΩ for oscillator frequency, and we assume the allowable maximum duty cycle is 75%.

$$R_{DT} = (33K+1250) \times (0.6 \times 0.75 + 0.7) = 39.38K$$

When a 39.38KΩ resistor is used as R_{DT}, the maximum limitation of PWM duty cycle is 75%.

A capacitor (C_{DT}), parallel connecting with the resistor R_{DT} as shown in Figure 15, is used to implement the soft-start function during power on. The soft-start time equation is:

$$V_{DT} \approx I_{DT} \div R_{DT} \left(1 - e^{\frac{-t}{R_{DT} C_{DT}}} \right)$$

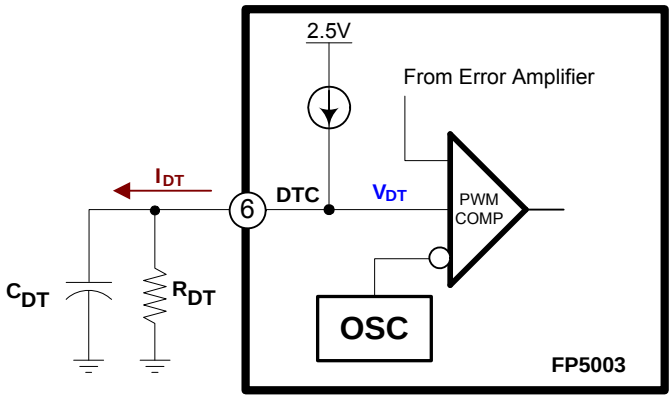

Figure 15. Soft-Start Circuit

Note:

C_{DT} is discharged by internal circuit every time when UVLO or SCP becomes active.

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Under Voltage Lock-out (UVLO) Protection

When the power supply turns off, the output of FP5003 also turns off and resets the SCP latch whenever the supply voltage drops under the UVLO off threshold voltage. It is a simple protection function when the supply voltage can not maintain at a stable operating condition. The UVLO hysteresis voltage avoids an internal false trigger whenever power noises or spikes appear.

Short-circuit Shutdown and Auto Re-start Protection (SCSAR)

FP5003 includes short-circuit shutdown and auto re-start protection function (see Figure 16), which turns the power MOS off to prevent damage when the converter output is over loading or short circuit.

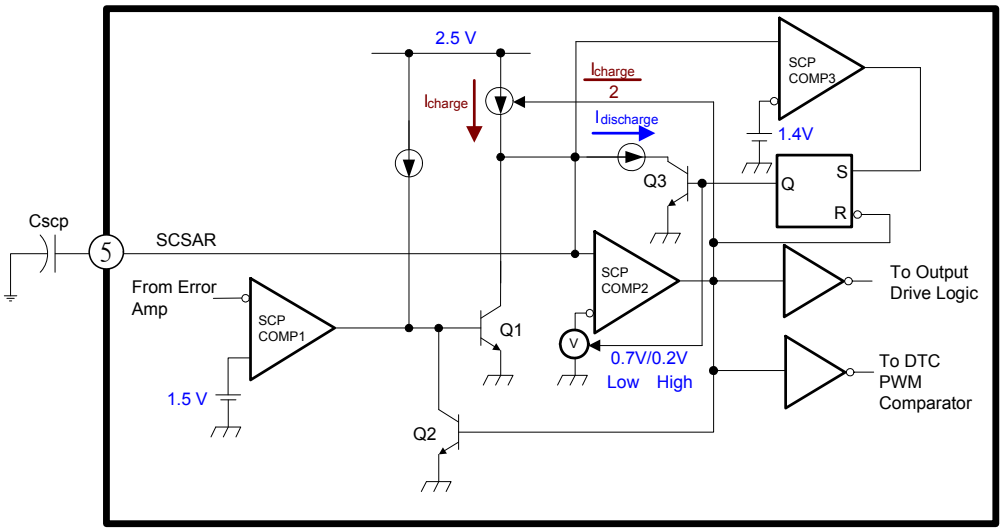

Figure 16. SCSAR Protection Circuit

When error amplifier output voltage is lower than 1.5V, SCP comparator 1 output will keep in high state, Q1 is turn-on, and C_{SCP} can not be charged. When short circuit occurs, the COMP pin of error-amplifier would rise to larger than 1.5V. SCP comparator 1 output changes to low state and C_{SCP} is charged by I_{CHARGE} current. Once C_{SCP} is charged to higher than 0.7V threshold, SCP comparator 2 output will change to high state and Q2 is turned-on to keep Q1 off in latch mode. Meanwhile, the source current of C_{SCP} would change to half of original current for the first shutdown phase that will turn FP5003's output off and pull DTC pin to low. The SCP function of FP5003 is released if short circuit condition is removed before SCP comparator 2 outputs and turning on Q2.

When C_{SCP} voltage is greater than 1.4V of SCP comparator 3, the output of S-R Latch would turn on Q3 and change SCP comparator 2's output from 0.7V to 0.2V. When SCP comparator 3 is active, C_{SCP} is discharged until SCP comparator 2 is released from the latch state, output of FP5003 is

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active and DTC pin is working in soft-start state or limitation of duty cycle. C_{SCP} discharging time from 1.4V to 0.2V is the second shutdown phase. After this phase, FP5003 would be released from shutdown state and re-start the normal operation. Figure 17 is a relation description about SCSAR pin and the other pins of FP5003.

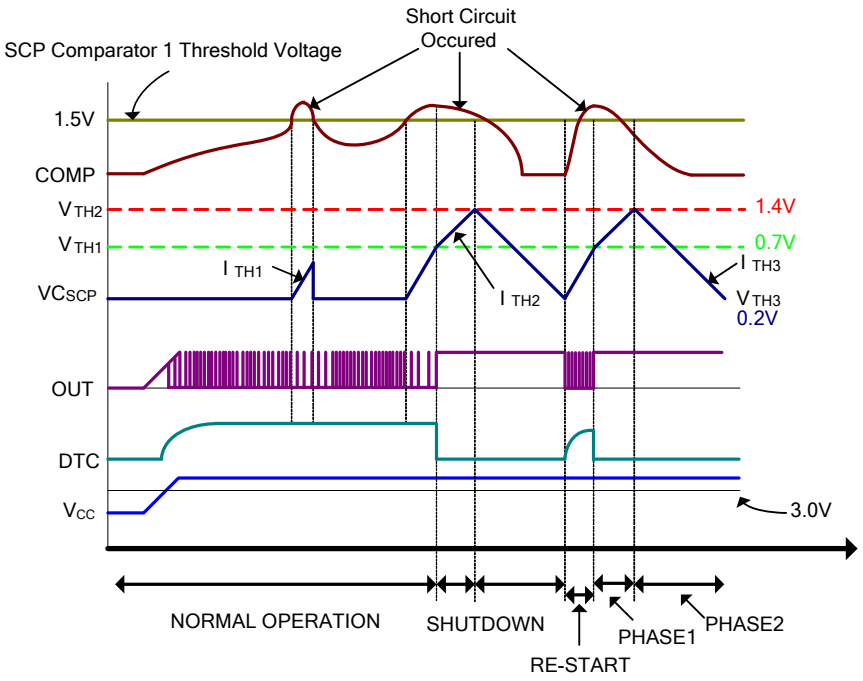

Figure 17. Shutdown and Re-start waveform

The equations are shown below for shutdown and re-start time calculation:

AUTO RE-START time equation:

$$t_{RE-START} = \frac{V_{TH1} \times C_{SCP}}{I_{TH1}}$$

SHUTDOWN time equation:

$$t_{SHUTDOWN} = t_{PHASE1} + t_{PHASE2} = \frac{(V_{TH2} - V_{TH1}) \times C_{SCP}}{I_{TH2}} + \frac{(V_{TH2} - V_{TH3}) \times C_{SCP}}{I_{TH3}}$$

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Output Transistors

The output of the FP5003 is a totem-pole transistor pair, which provides current source and sink capability for driving the external MOSFET directly. A basic drive method is shown in figure 18.

When PWM operation frequency is different, the both of on and off time of MOSFET also are different.

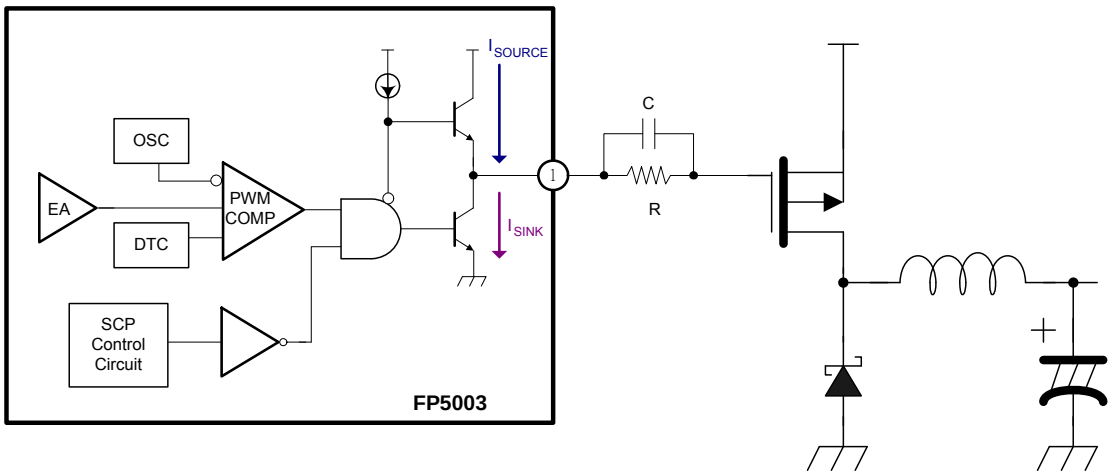

Figure 18. MOSFET Output Driving Cricuit

Note:

It is very important to choose a suitable MOSFET for high frequency operation. The larger capacitance between gate and source of MOSFET makes more switching loss under the same condition such as high frequency operation, supply voltage and driving current.

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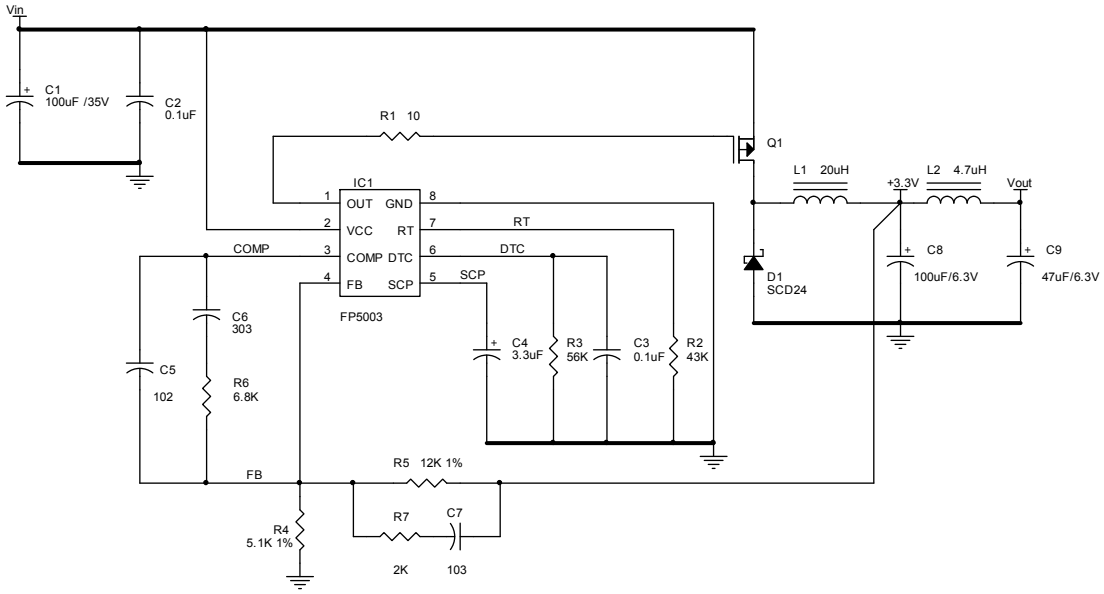
Typical Application

Application Example: V_{IN} = DC 5.0V~ 24.0V

V_{OUT} = DC 3.3V, I_{OUT} = 2.0A



Note:

This is a basic circuit of FP5003 example. C4 is a short circuit and re-start timing capacitor (C_{SCP}). The purpose of R3 and C3 is soft-start duty control (R_{DTC}*C_{DTC}). R2 is for adjustable oscillator frequency (R_T). R5 and R4 are feedback bias resistors for V_{OUT}. C5-R6-C6 establish compensation network for close loop stability.

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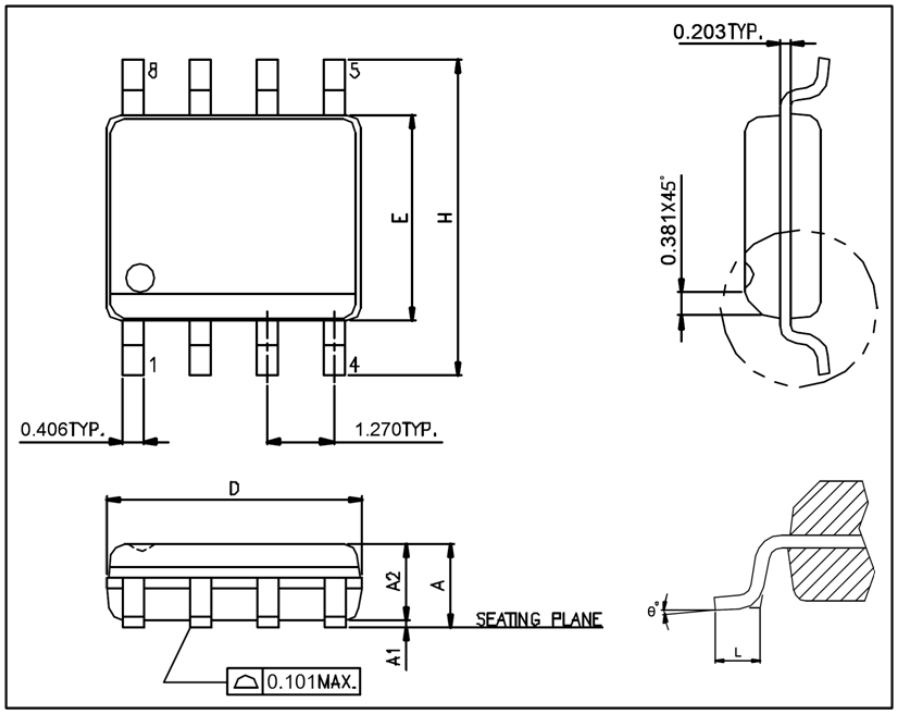
Package Outline

SOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.

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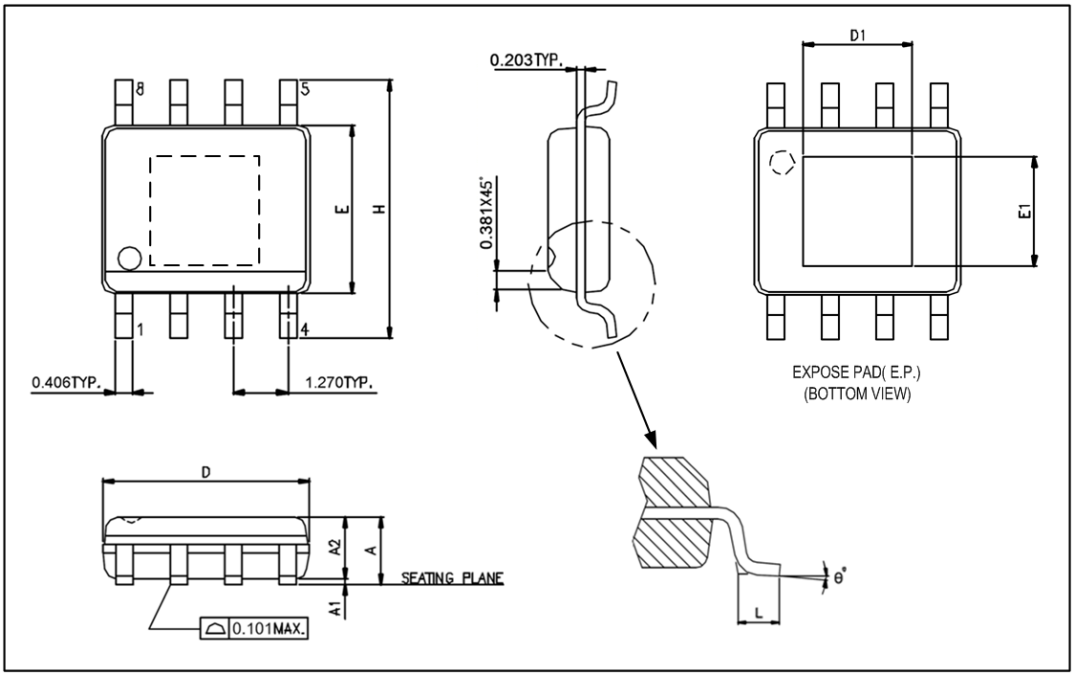
SOP-8L (EP)



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.050	0.152
A2		1.498
D	4.800	4.978
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E1	2.184 REF	
D1	2.971 REF	

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AA.
2. Dimension ”D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.

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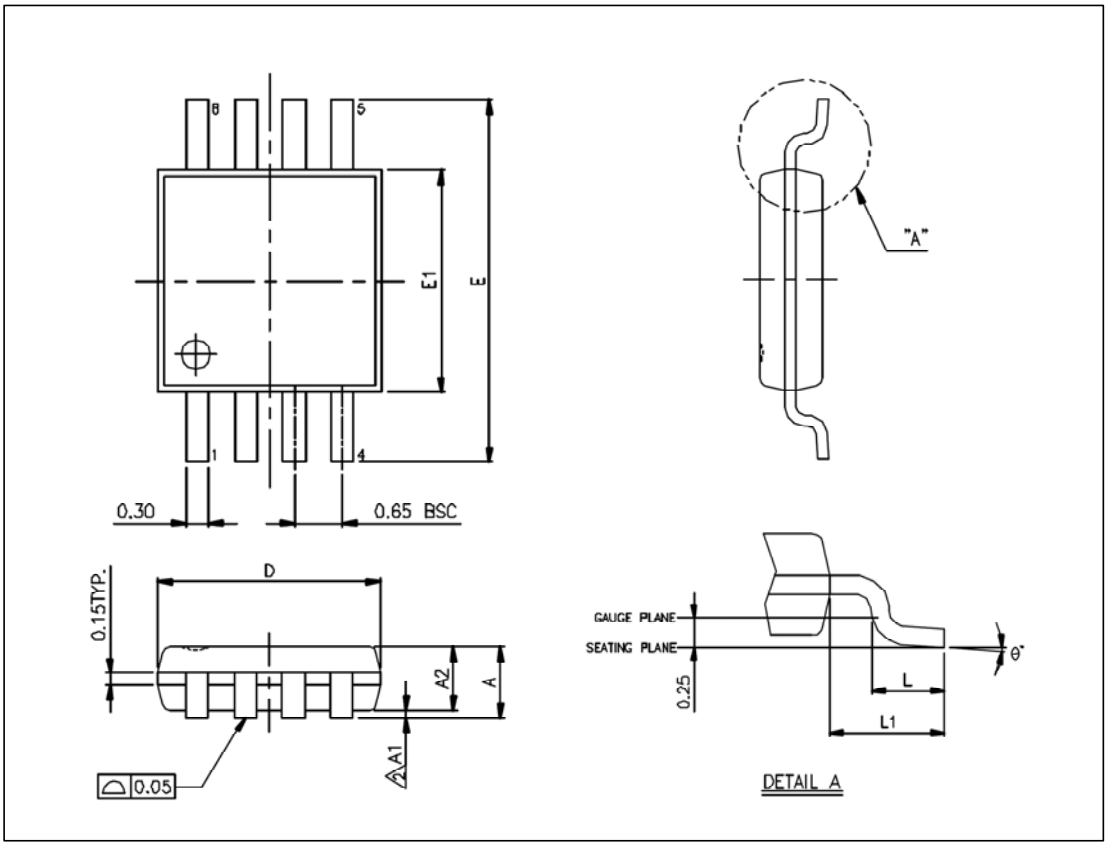
MSOP-8L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A		1.100
A1	0.000	0.150
A2	0.750	0.950
D	3.000 BSC	
E	4.900 BSC	
E1	3.000 BSC	
L	0.400	0.800
L1	0.950 REF	
θ°	0°	8°

Notes:

1. Package dimensions are in compliance with JEDEC outline: MO-187 AA.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E1” does not include inter-lead flash or protrusions.

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