Dual PWM Controller With SCP / DTC Function

Halogen Free

General Description

The FP5452 is a dual channel PWM buck controller with short circuit protection (SCP) and adjustable maximum duty control (DTC) function. It includes one 2.5V precision voltage reference regulator, two error amplifiers, PWM control circuits, totem-pole output stages and the under voltage lockout circuit (UVLO). It offers space and low cost solutions in many applications such as the DC / DC converters and backlight inverters.

Using FP5452, it is easy to complete a power conversion regulator design with few external components. The circuit diagram of the typical application example is as below.

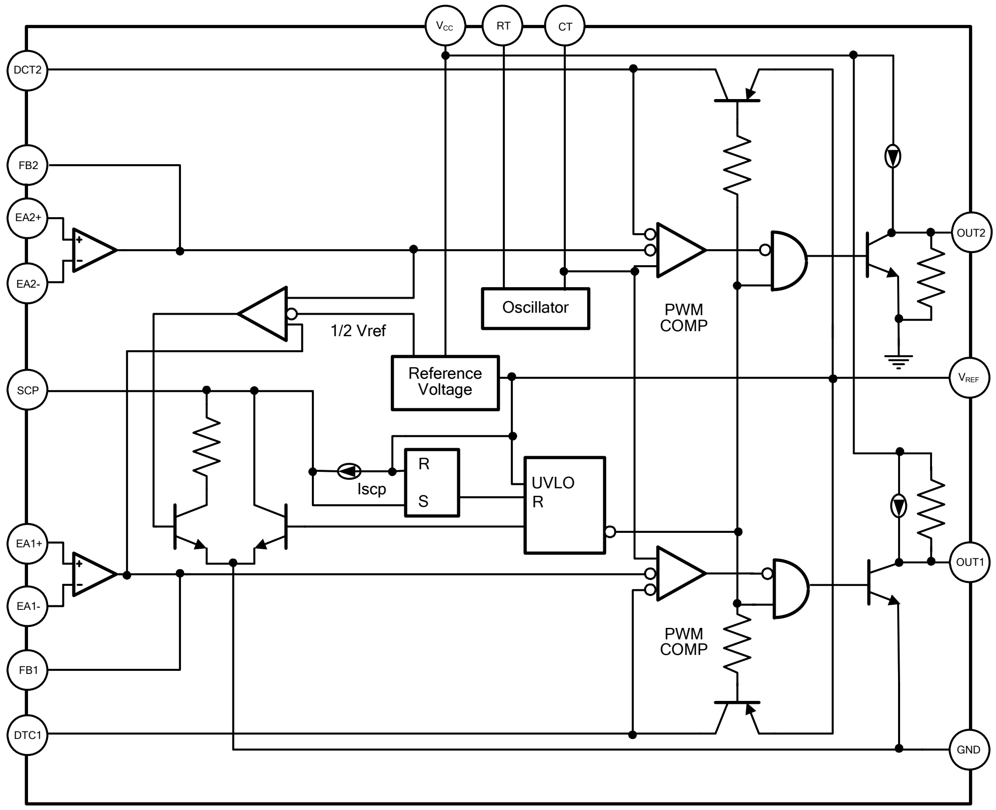
Features

- Wide Operating Voltage range: 3.6~40V
- Fixed Reference Voltage: 2.5V
- Reference Voltage Precision: 2%
- Oscillator Frequency: Max. 500KHz
- Totem-pole Output stage
- Low Quiescent Supply Current Under 3.5mA
- Variable dead-time Control (DTC)
- UVLO Protection Function
- SCP Protection Function (Threshold Voltage: 1.3V)
- Package: SOP-16L / SSOP-16L

Applications

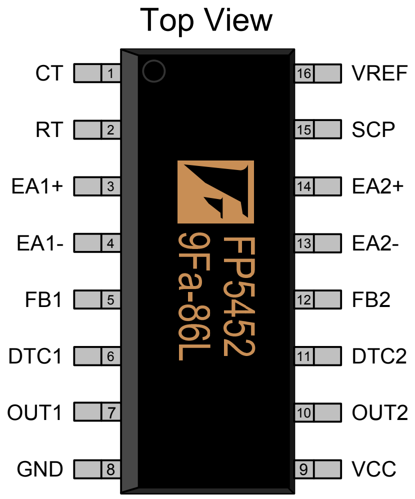
- DC / DC Converters for Video Camera
- TFT LCD Monitor
- Back Light CCFL Inverter

Function Block Diagram



Pin Descriptions

SOP-16L



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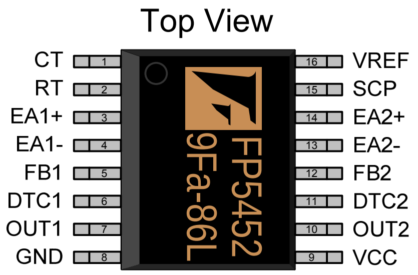
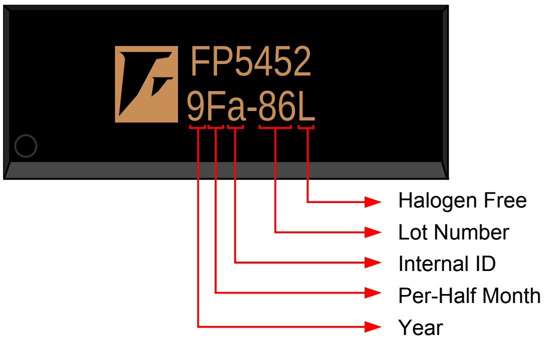


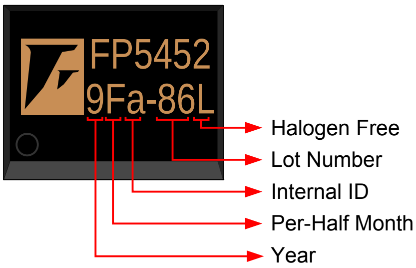
Name	No.	I / O	Description
CT	1	I	Connect a Capacitor for Oscillator Frequency Adjustment
RT	2	I	Connect a Resistor for Oscillator Frequency Adjustment
EA1+	3	I	Output 1 Error Amplifier Non-inverting Input
EA1-	4	I	Output 1 Error Amplifier Inverting Input
FB1	5	O	Output 1 Error Amplifier Output
DTC1	6	I	Output 1 Maximum Duty Control Voltage
OUT1	7	O	Output 1 Totem-pole Output
GND	8	P	IC Ground
V_{CC}	9	P	IC Power Supply
OUT2	10	O	Output 2 Totem-pole Output
DTC2	11	I	Output 2 Maximum Duty Control Voltage
FB2	12	O	Output 2 Error Amplifier Output
EA2-	13	I	Output 2 Error Amplifier Inverting Input
EA2+	14	I	Output 2 Error Amplifier Non-inverting Input
SCP	15	I	Connect a Capacitor to Set Short Circuit Protection Timing
V_{REF}	16	O	2.5V Reference Voltage Output

Marking Information

SOP-16L



SSOP-16L



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Internal ID: Internal Identification Code

Per-Half Month: Production period indicated in half month time unit

For Example: January → A (Front Half Month), B (Last Half Month)

February → C (Front Half Month), D (Last Half Month)

Year: Production year's last digit

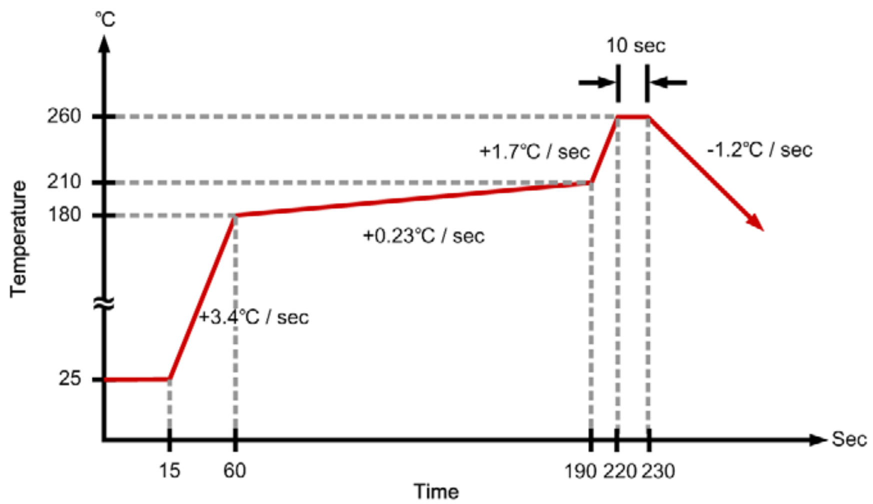
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5452DR-LF	-20°C ~ +85°C	SOP-16L	2500 EA	Tape & Reel
FP5452RR-LF	-20°C ~ +85°C	SSOP-16L	2500 EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}				40	V
Differential Input Voltage	V_{ID}				20	V
Output Sink Current	I_O				150	mA
Maximum Junction Temperature	T_J				+150	℃
Thermal Resistance Junction to Ambient	θ_{JA}	SOP-16L			+90	℃ / W
		SSOP-16L			+110	℃ / W
Thermal Resistance Junction to Case	θ_{JC}	SOP-16L			+45	℃ / W
		SSOP-16L			+55	℃ / W
Power Dissipation	P_D	SOP-16L, T_A= +25℃			830	mW
		SSOP-16L, T_A= +25℃			570	mW
Storage Temperature			-65		+150	℃
Lead Temperature, (soldering, 10 sec)					+260	℃

Suggested IR Re-flow Soldering Curve



Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage			3.6		40	V
Operating Temperature			-20		+85	℃

DC Electrical Characteristics (V_{CC}= 6V, f=200kHz, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Reference Section						
Output Voltage (pin16)	V_{REF}	I_O=1mA	2.45	2.5	2.55	V
Output Voltage Change with Temperature		T_A=-20℃ to 25℃		-0.1%	±1%	
		T_A=25℃ to 85℃		-0.2%	±1%	
Input Voltage Regulation	$\triangle V_{REF}$ / V_{REF}	V_{CC}=3.6V ~ 40V		2	12.5	mV
Output Voltage Regulation	$\triangle V_{REF}$ / V_{REF}	Io = 0.1mA to 1 mA		1	7.5	mV
Short-Circuit Output Current	I_{SHORT}	V_O=0	3	10	30	mA
Under Voltage Lockout Section						
Upper Threshold Voltage (V_{CC})	V_{UPPER}	$I_{O\ (REF)}$ = 0.1 mA, T_A=25℃		2.72		V
Lower Threshold Voltage (V_{CC})	V_{LOW}			2.6		V
Hysteresis (V_{CC})	V_{HYS}		80	120		mV
Reset Threshold Voltage (V_{CC})	V_{RESET}		1.0	1.3		V
Short-Circuit Protection Control Section						
Input Threshold Voltage (SCP)	V_{TH}	T_A= 25℃	1.2	1.3	1.5	V
Standby Voltage (SCP)	$V_{STANDBY}$	No pullup	60	80	100	mV
Latched Input Voltage (SCP)	V_{LATCH}	No pullup		40	60	mV
Input (Source) Current	I_{SOURCE}	V_I=0.7V, T_A=25℃	-1.	-2.0	-2.5	μA
Comparator Threshold Voltage (Feedback)	$V_{COMP\ (TH)}$			1.20		V
Oscillator Section						
Frequency	f	C_T=330pF, R_T=10K		220		KHz
Standard Deviation of Frequency	△f	C_T=330pF, R_T=10K		10		%
Frequency Change with Voltage	△f / △V	V_{CC}=3.6V to 40V		1		%
Frequency Change with Temperature	△f / △T	T_A=-20℃ to 25℃	-2	-0.4	+2	%
		T_A=25℃ to 85℃	-2	-0.2	+2	%
Duty Control Section						
Input Bias Current (DTC)	I_{BIAS}				1	μA
Latch Mode (Source) Current (DTC)	I_{SOURCE}	T_A=25℃	-80	-260		μA
Latched Input Voltage (DTC)	V_{LATCH}	I_O=40μA	2.2	2.3		V
Input Threshold Voltage at f=10kHz (DTC)	V_{TH}	Zero Duty Cycle		2.05	2.25	V
		Maximum Duty Cycle	1.2	1.35		V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Error Amplifier Section						
Input Offset Voltage	V_{IO}	Vo (Feedback)=1.25V	-6		+6	mV
Input Offset Current	I_{IO}	Vo (Feedback)=1.25V	-100		+100	nA
Input Bias Current	I_{BIAS}	Vo (Feedback)=1.25V		160	500	nA
Common-mode Input Voltage Range	V_{ICM}	V_{CC}=3.6V to 40 V	0.3		1.6	V
Open-Loop Voltage Gain	A_{VO}	R_F=200KΩ	70	80		dB
Unity Gain Bandwidth	BW			1.5		MH_Z
Common Mode Rejection Ratio	CMRR		60	80		dB
Positive Output Voltage Swing	V_{POS}		V_{REF}-0.3			V
Negative Output Voltage Swing	V_{NEG}				1	V
Output (Sink) Current (Feedback)	I_{SINK}	V_{ID}= -0.1V, VO=1.25V	1	4.0		mA
Output (Source) Current (Feedback)	I_{SOURCE}	V_{ID}=0.1V, V_O=1.25V	-45	-90		μA
Output Section						
V_{OUT} Low Voltage	V_{OL}	I_{SINK}=20mA		0.8	1.2	V
		I_{SINK} =130mA, Vcc=15V		1.2	1.8	V
V_{OUT} High Voltage	V_{OH}	I_{SOURCE}=20mA	4.0	4.5		V
		I_{SOURCE}=130mA, Vcc=15V	12.7	13.2		V
Rise Time	t_R	T_J=25℃, C_L=1nF		60	120	nS
Fall Time	t_F	T_J=25℃, C_L=1nF		30	60	nS
PWM Comparator Section						
Input Threshold Voltage at f=10kHz (Feedback)	V_{TH}	Zero Duty Cycle		2.05	2.25	V
		Maximum Duty Cycle	1.2	1.35		V
Total Device						
Standby Supply Current	$I_{STANDBY}$	Off-State		2.2	3.3	mA
Average Supply Current	I_{AVE}	R_T=10K		2.7	3.8	mA

Typical Operating Characteristics

(V_{CC}=5V, T_A= 25°C, unless otherwise noted)

TRIANGLE OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

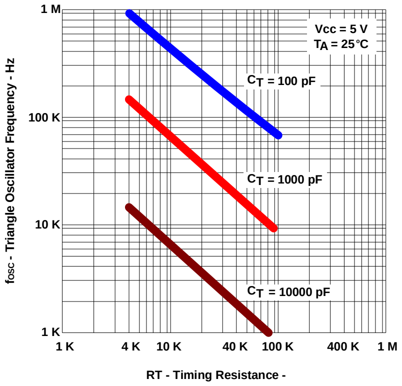


Figure 1

OSCILLATOR FREQUENCY VARIATION
vs
FREE-AIR TEMPERATURE

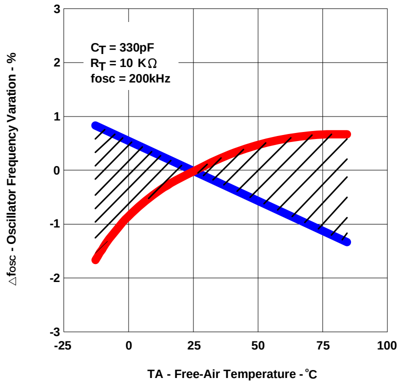


Figure 2

TRIANGLE WAVEFORM SWING VOLTAGE
vs
TIMING CAPACITANCE

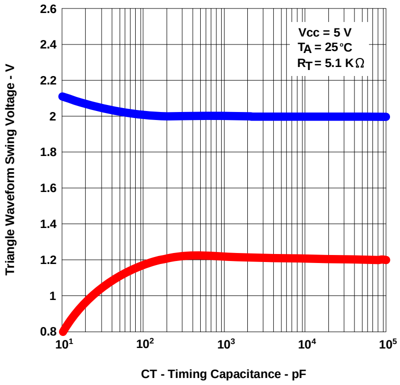


Figure 3

TRIANGLE WAVEFORM PERIOD
vs
TIMING CAPACITANCE

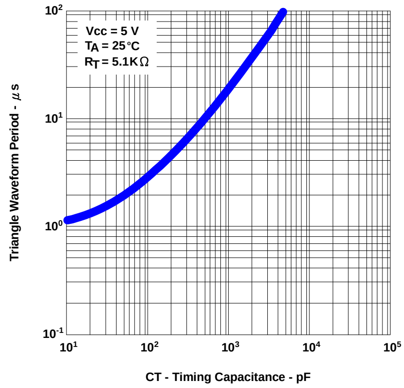


Figure 4

REFERENCE OUTPUT VOLTAGE VARIATION
vs
FREE-AIR TEMPERATURE

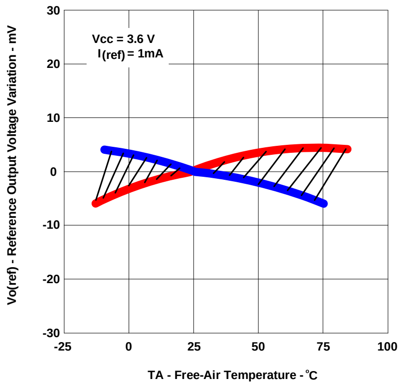


Figure 5

REFERENCE OUTPUT VOLTAGE VARIATION
vs
FREE-AIR TEMPERATURE

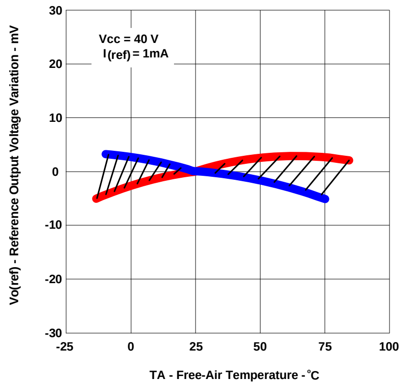


Figure 6

REFERENCE OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

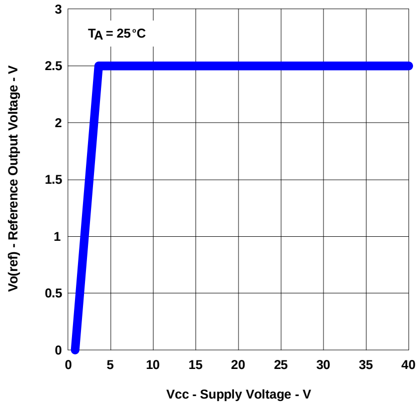


Figure 7

UNDERVOLTAGE LOCKOUT
CHARACTERISTIC

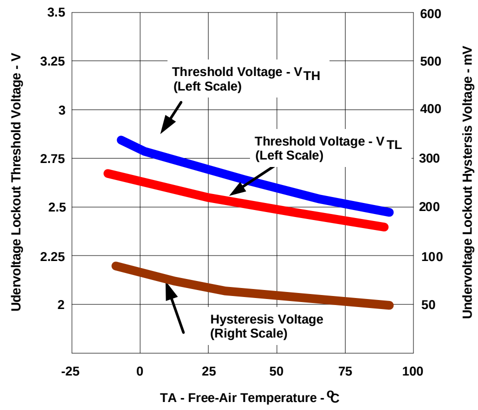


Figure 8

UNDERVOLTAGE LOCKOUT
HYSTERESIS CHARACTERISTICS

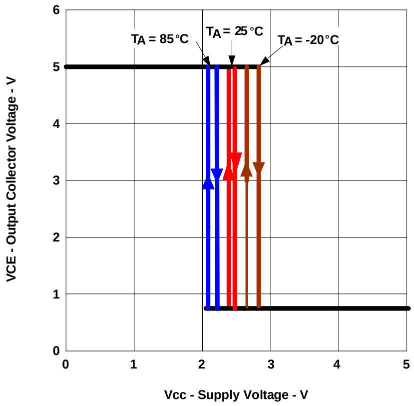


Figure 9

SHORT-CIRCUIT PROTECTION
CHARACTERISTICS

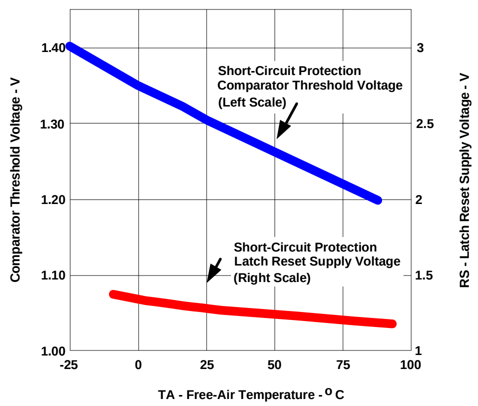


Figure 10

ERROR AMP MAXIMUM OUTPUT
VOLTAGE SWING
vs
FREQUENCY

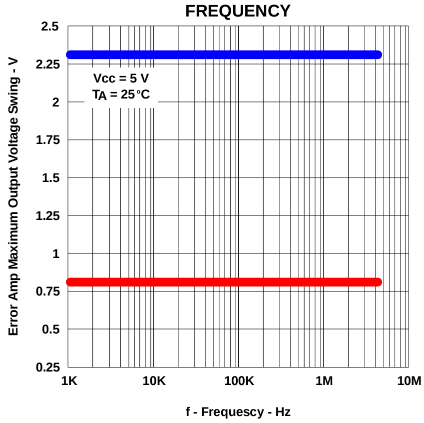
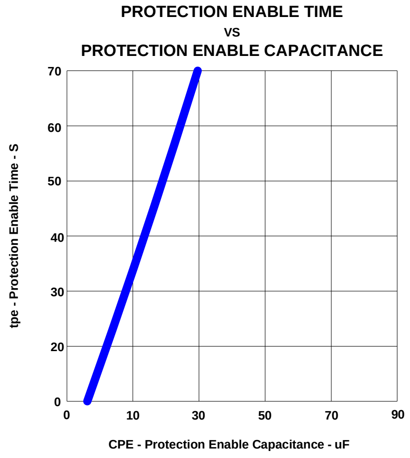


Figure 11


PROTECTION ENABLE TIME
vs
PROTECTION ENABLE CAPACITANCE
tpe - Protection Enable Time - S
CPE - Protection Enable Capacitance - uF
0
10
20
30
40
50
60
70
90

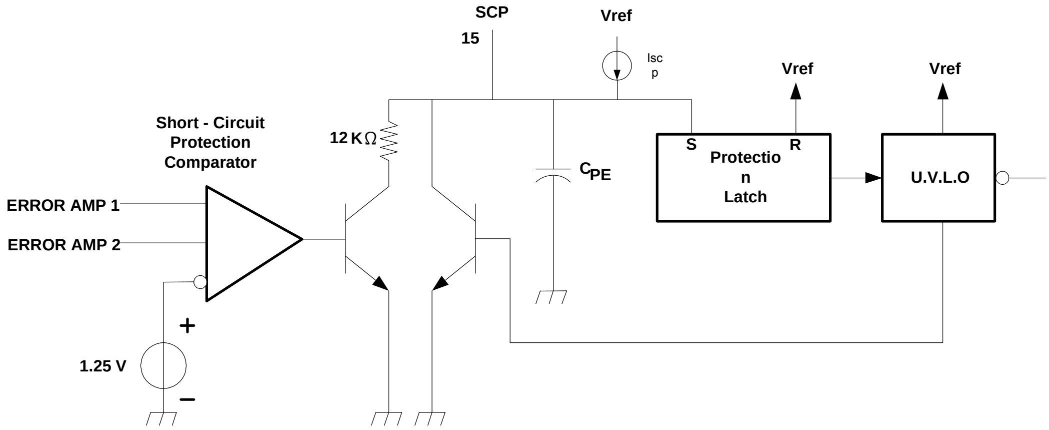

SCP
15
Vref
Isc
p
Vref
Vref
Short - Circuit
Protection
Comparator
12 KΩ
CPE
S
R
Protectio
n
Latch
U.V.L.O
ERROR AMP 1
ERROR AMP 2
1.25 V
+
−

Figure 12

OUTPUT TRANSISTOR ON DUTY CYCLE
VS
DEAD - TIME INPUT VOLTAGE

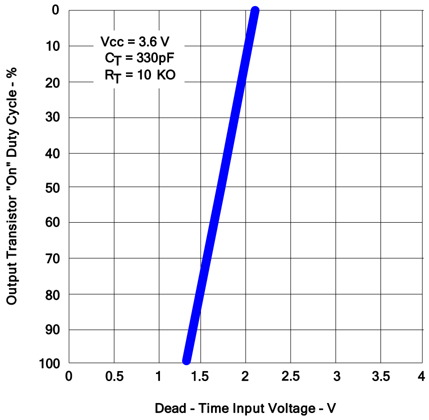


Figure 13

STANDBY CURRENT
VS
SUPPLY VOLTAGE

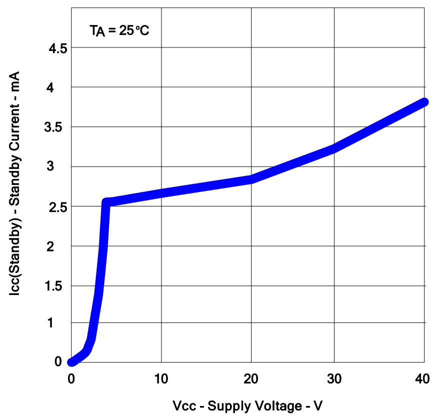


Figure 14

STANDBY CURRENT
VS
FREE - AIR TEMPERATURE

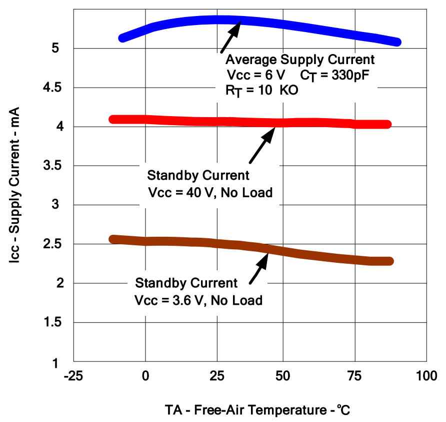


Figure 15

GAIN (AMPLIFIER IN UNITY-GAIN CONFIGURATION)
VS
FREQUENCY

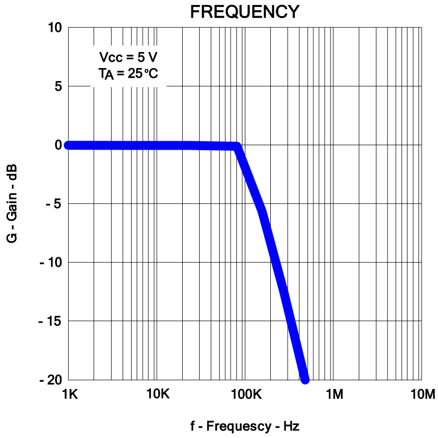


Figure 16

Timing Waveform

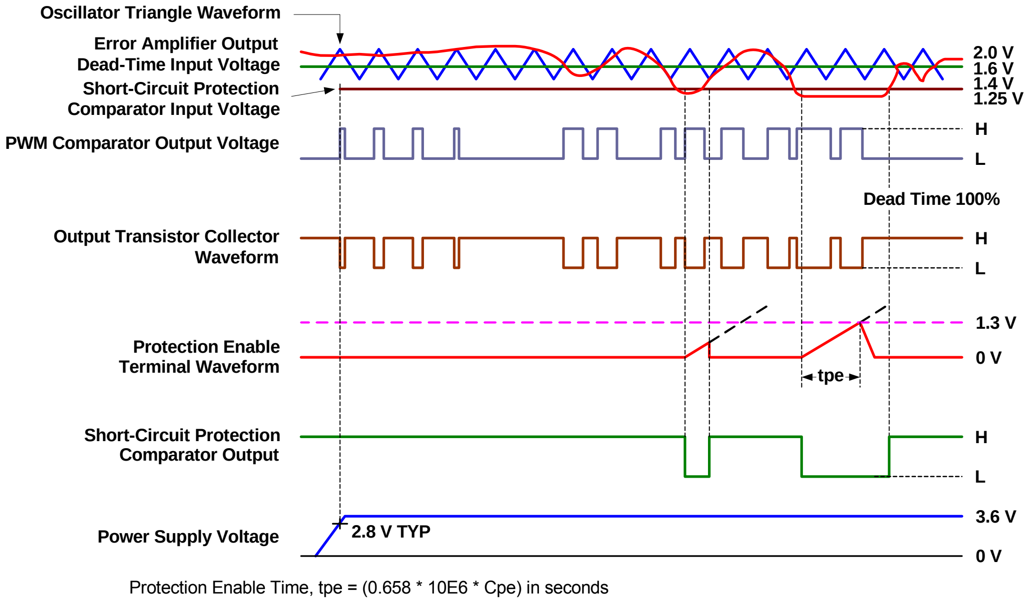


Figure 17 FP5452 CH1 / CH2 Timing Diagram

Function Description

Voltage Reference

FP5452 has an internal 2.5V reference regulator for its internal circuits' voltage bias. This reference voltage is also divided down by a resistive divider to provide error amplifiers as the inverting input reference voltage. (Figure 18)

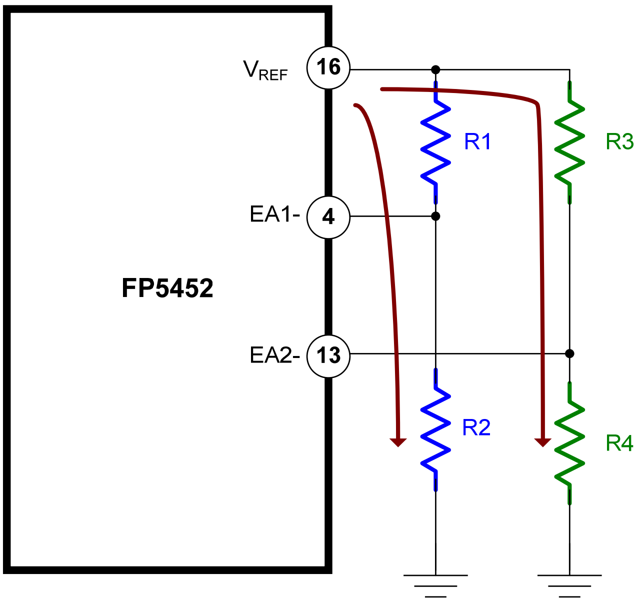


Figure 18 Error Amplifiers and Reference with Resistive Dividers

The error amplifier inverting input (EA1- or EA2-) reference voltage equations are shown as following:

$$V_{EA1-} = V_{REF}(2.5V) \times \frac{R2}{R1 + R2}$$

$$V_{EA2-} = V_{REF}(2.5V) \times \frac{R4}{R3 + R4}$$

Error Amplifier

The error amplifiers of FP5452 compare the feedback voltage from the resistive dividers of DC-DC converter output to the reference voltage (see Figure 19). They generate the error signal for the PWM comparator.

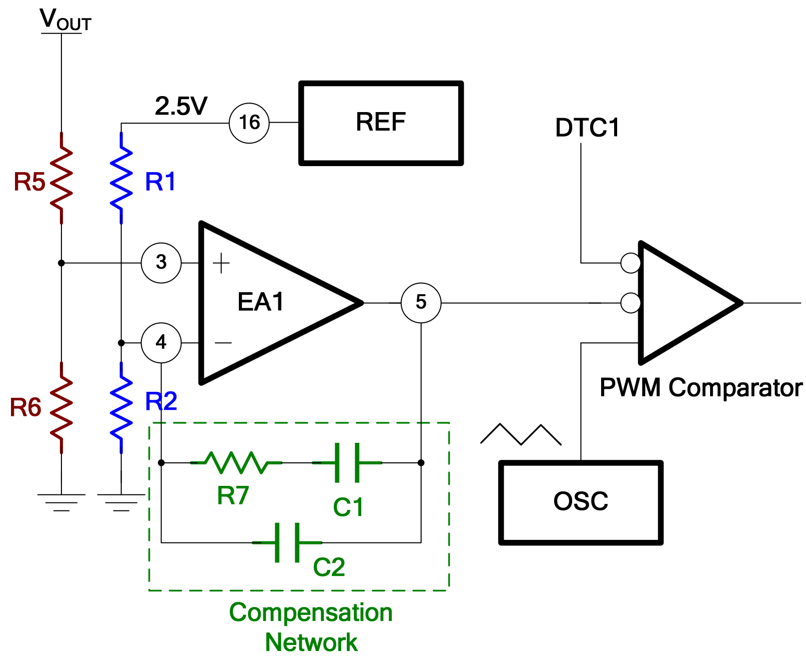


Figure 19 Error Amplifier with Feedback / Compensation Circuits

The Buck Converter Output Voltage:

$$V_{OUT} = \left(1 + \frac{R5}{R6}\right) \times \left(\frac{R2}{R1 + R2}\right) \times 2.5V$$

Error Amplifier Gain:

$$Av = 1 + \frac{1 + sR7C1}{sRi(C1 + C2)(1 + sR7C2)} \quad ,Ri=R1//R2$$

Error Amplifier Zero and Pole Frequency:

$$Fz = \frac{1}{2\pi R7C1} \quad , \quad Fp = \frac{1}{2\pi R7C2}$$

Oscillator / PWM Comparator

The oscillator frequency can be adjusted from 20KHz to 500KHz by the resistor (RT) and capacitor (CT) that are connected to pin1 and pin2 respectively. A sawtooth waveform would be compared with the error amplifier output signal and duty control voltage. Figure 20 shows the relationship of oscillator, error amplifier and PWM comparator. Figure 21 is their waveforms.

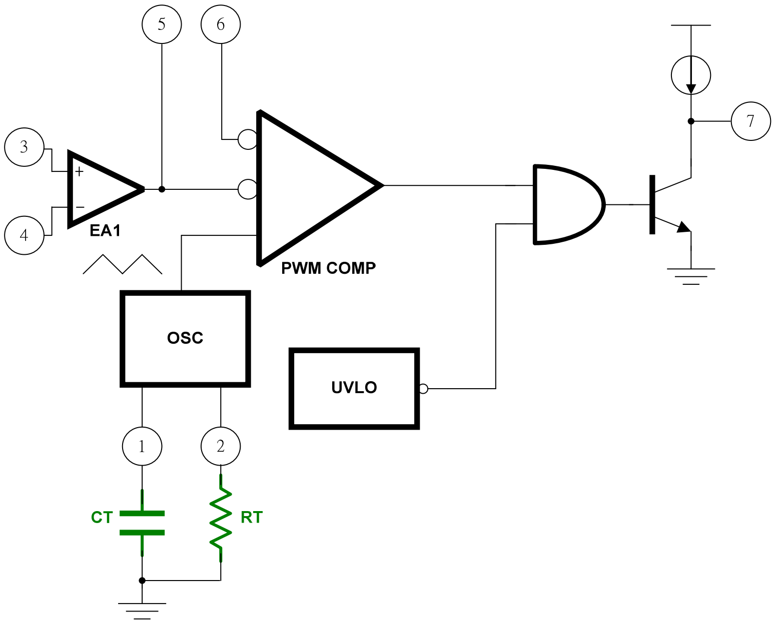


Figure 20 Oscillator / PWM Comparator with Frequency RC Circuits

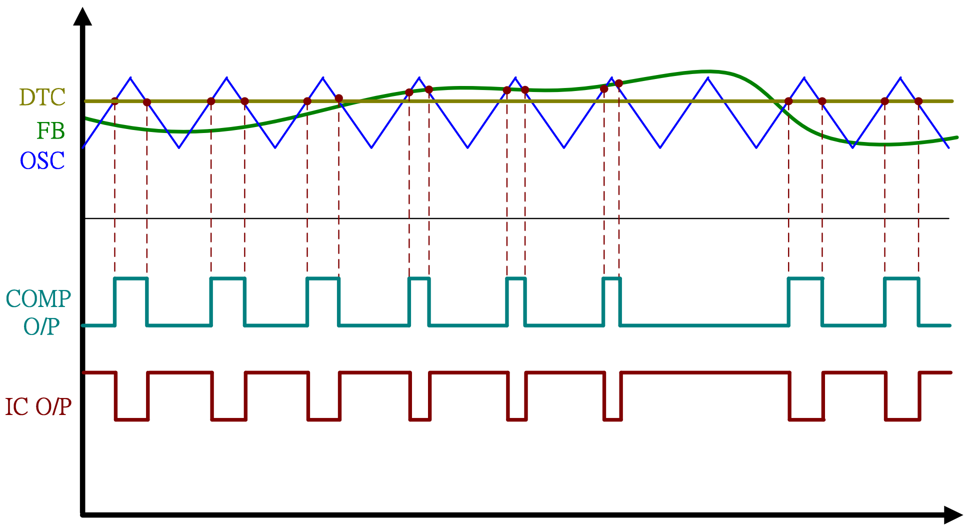


Figure 21 FP5452 Timing Waveforms

The relationship of oscillator waveform and duty voltage is shown below (Figure 22).

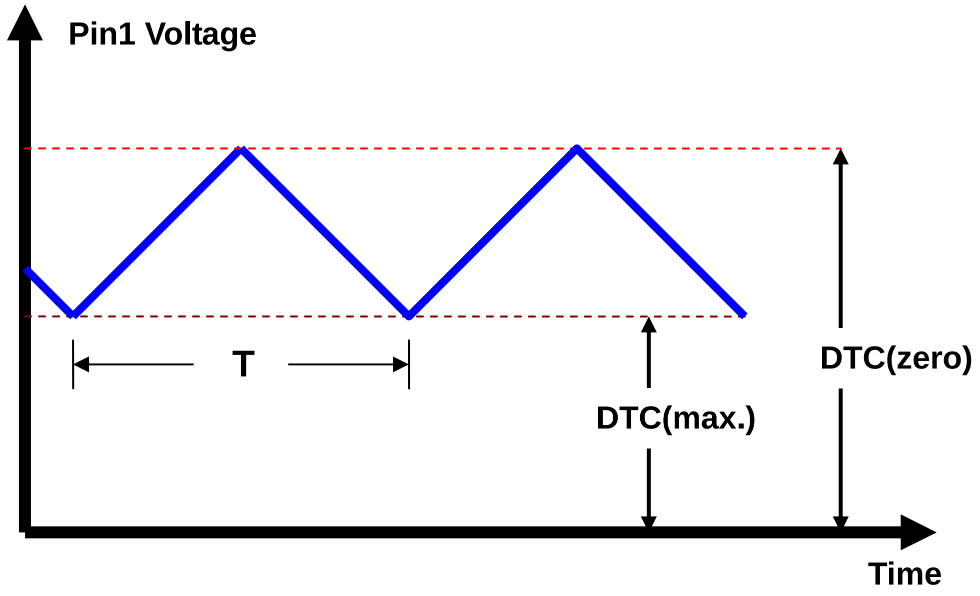


Figure 22 Oscillator Frequency and DTC voltage

The oscillator frequency calculation equation is shown as below:

$$f = \frac{VT}{2 \times CT \times RT \times (Vzero - Vmax.)}$$

Duty Control / Soft-Start

The duty control (DTC) is a function for the PWM duty cycle limitation. If the DTC voltage is lower than DTC maximum voltage (1.35V typically), the PWM duty cycle can be as large as 100% cycle. If the DTC voltage is higher than DTC zero voltage (2.05V typically), the PWM duty cycle will always be turned-off (zero duty).

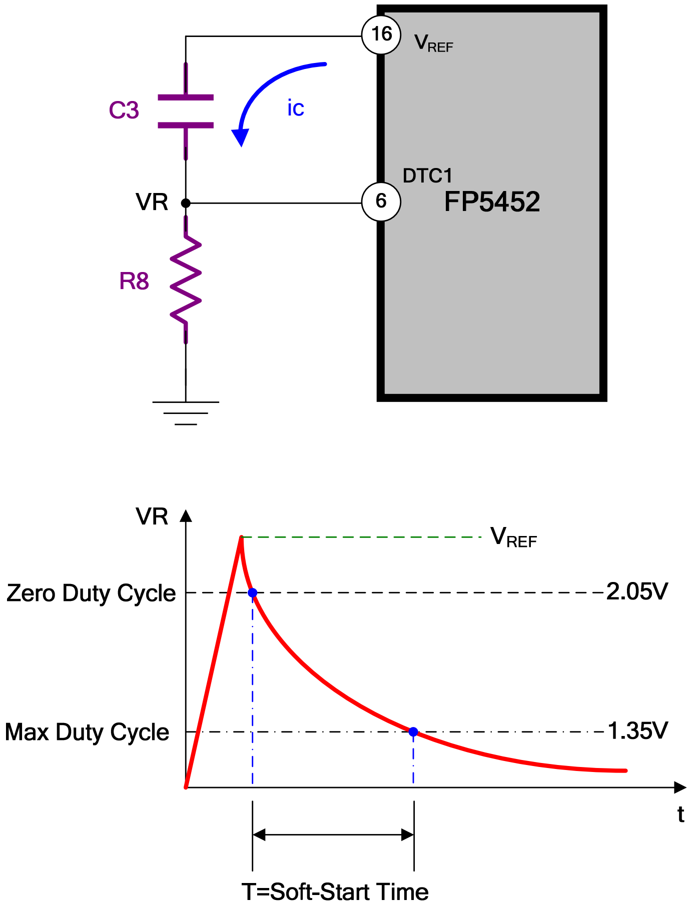


Figure 23 DTC Soft-start RC Circuit and Waveform

The soft-start time equation:

$$t = 0.616 \times R8C3$$

Short Circuit Protection

FP5452 has a protection function when short circuit is happened. When the DC-DC converter output voltage is drop to a very low voltage, the error amplifier IN+ pin would also have a low feedback voltage. The error amplifier will pull its output to a low voltage state. This output voltage is compared with a 1.25V reference by the SCP comparator. The SCP comparator then turns off transistor Q1 and SCP capacitor is charged up. When SCP voltage is higher than a threshold voltage (1.3V typically), this SCP state is latched. The DTC pins are charged up to disable PWM output (zero duty) and the SCP pin voltage is discharged by Q2 transistor.

Once SCP state is latched, the controller no longer output PWM control pulses. It can only be reset by reducing the input power supply voltage to below UVLO trigger point (2.6V) (see Figure 24).

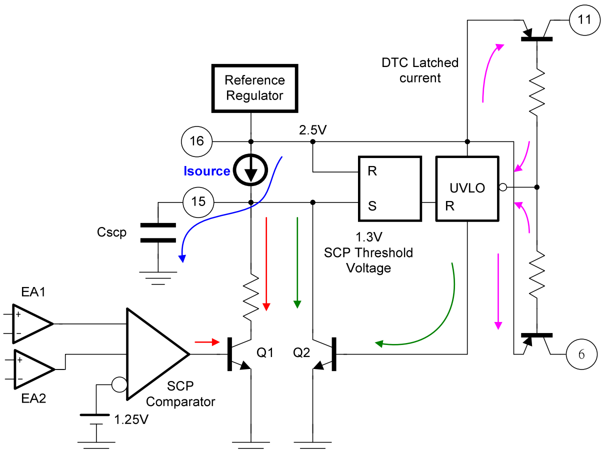


Figure 24 Internal SCP Detection / Control Circuits

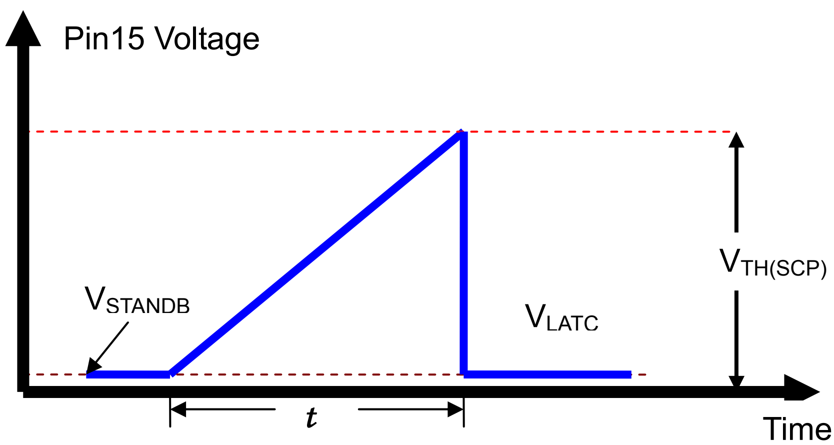


Figure 25 SCP Waveform (SCP active)

The SCP time equation is:

$$t = \frac{C_{SCP} \times \left(V_{th(scp)} - V_{sb}\right)}{I_{source}}$$

Application Information

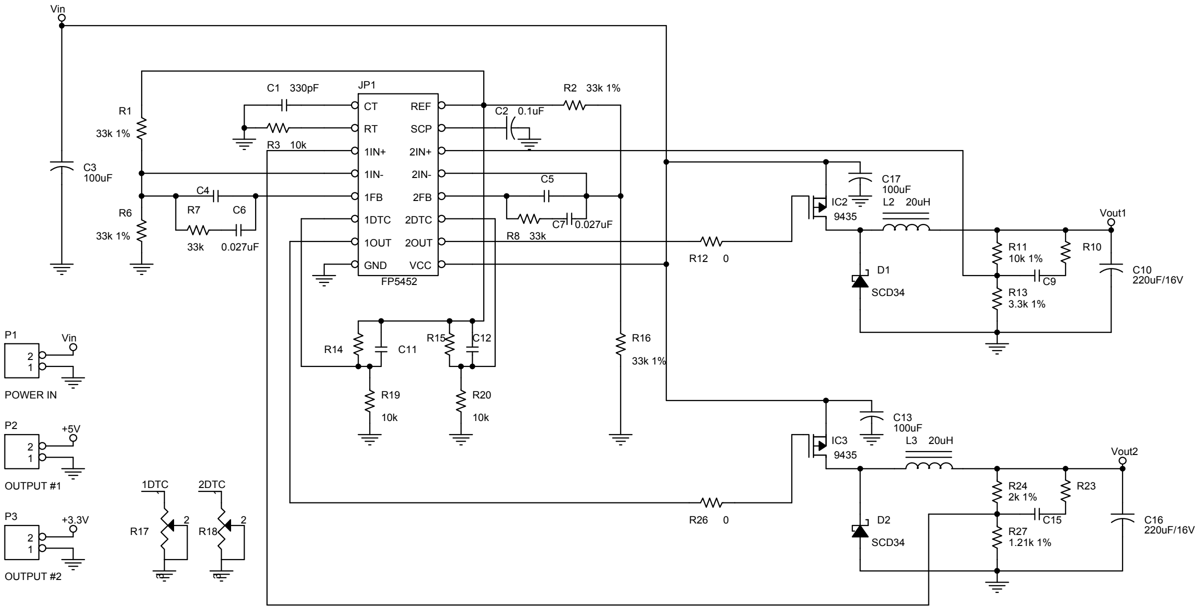


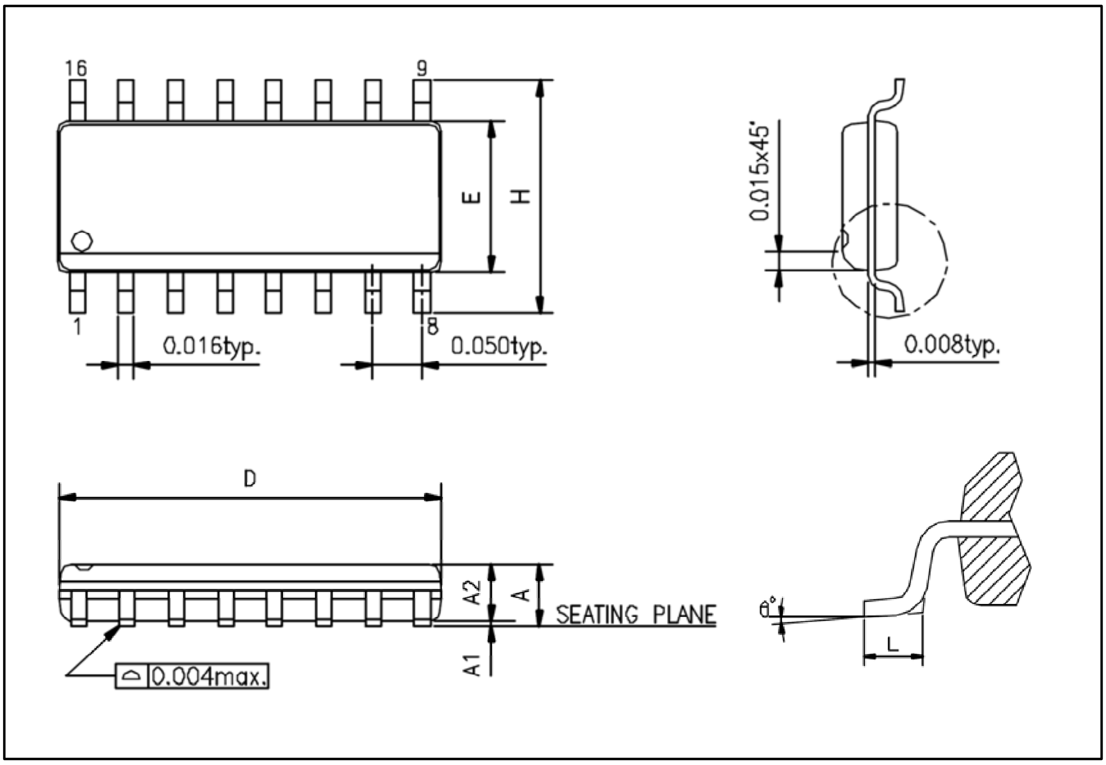
Figure 26 FP5452 2-channel Buck Regulators Application Circuits

Note:

1. The IN1- and IN2- voltage is 1.25V, half of V_{REF} voltage, because R1=R6 and R2=R16.
2. The R14-R19-C11 and R15-R20-C12 are DTC circuits for Buck Regulators power-on.
3. The R11-R13 and R24-R27 are the buck regulator output voltage feedback resistances.
4. The R7-C4-C6 is the compensation circuit for error amplifier 1.
5. The R8-C5-C7 is the compensation circuit for error amplifier 2.
6. The R3-C1 is used to decide FP5452 PWM frequency.
7. The C2 is the FP5452 short circuit protection delay time capacitor.

Package Outline

SOP-16L



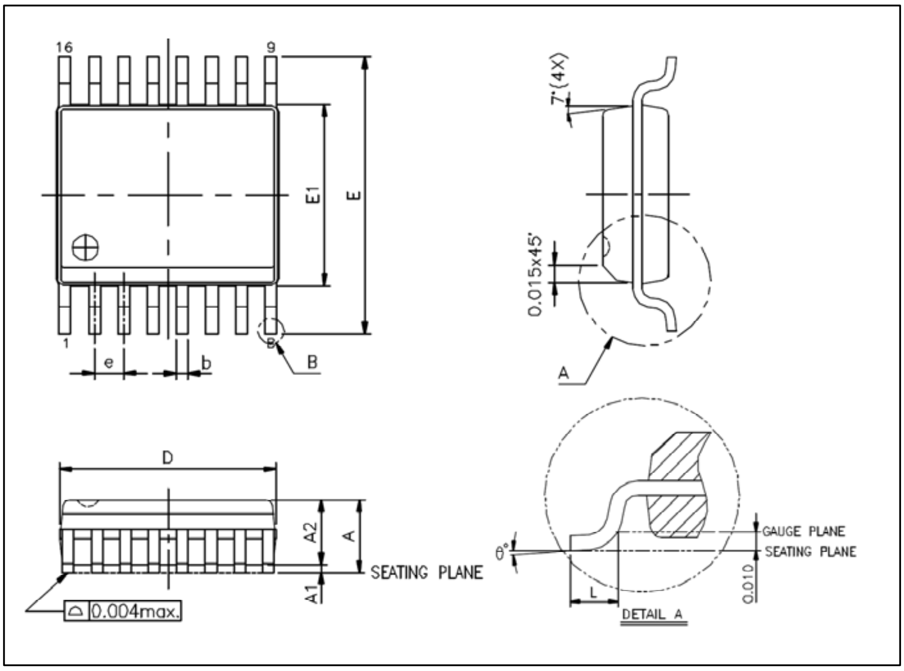
UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2	1.244	1.651
D	9.804	10.007
E	3.810	3.987
H	5.791	6.197
L	0.406	1.270
θ°	0°	8°

Note:

1. Package dimensions are in compliance with JEDEC outline: MS-012 AC.
2. Dimension “D” does not include molding flash, protrusions or gate burrs.
3. Dimension “E” does not include inter-lead flash or protrusions.

SSOP-16L



UNIT: mm

Symbols	Min. (mm)	Max. (mm)
A	1.346	1.752
A1	0.101	0.254
A2		1.498
b	0.203	0.304
b1	0.203	0.279
c	0.177	0.254
c1	0.177	0.228
D	4.800	5.003
E1	3.810	3.987
E	5.791	6.197
L	0.406	1.270
e	0.635 BASIC	
θ°	0°	8°

Note:

2. Package dimensions are in compliance with JEDEC outline: MO-137 AB.
3. Dimension “D” does not include molding flash, protrusions or gate burrs.
4. Dimension “E” does not include inter-lead flash or protrusions.